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Space Vector Techniques for a Binary-Cascaded Multilevel Inverter Operating Under Reduced Common-Mode Voltage With Reduced Commutations

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ABSTRACT This article presents a novel space vector pulsewidth modulation (SVPWM) for a three-phase binary-cascaded multilevel inverter (BCMLI). The SVPWM could become impractical in multilevel inverters (MLIs) because of its increasing complexity with a larger number of levels. The *gh* coordinate system can ease the digital implementation, but to generate the inverter's *abc* states from the nearest three vectors (NTVs), iterative computations are required every sampling instant. This article proposes a further reduction of computations by directly generating the *abc* state with minimum common-mode voltage (CMV) from a *gh* vector. Subsequently, only one vector among the NTVs is required for implementing the proposed SVPWM. The reduced CMV profile within the NTVs further permits the reduction of commutations by clamping one phase during a sampling period. The presented technique exhibits full dc bus utilization capability and can be implemented in the BCMLI and further applied to any *M*-level MLI. Also, if *M* is considerably large or if switching losses and electromagnetic interference emissions must be minimized, nearest vector modulation with reduced CMV along with the line-frequency operation of high-voltage cells can be implemented to reduce the switching losses. Experimental results of a BCMLI are presented to verify the effectiveness of the proposed technique.

INDEX TERMS Common-mode voltage (CMV), multilevel inverter (MLI), nearest vector modulation (NVM), space vector pulsewidth modulation (SVPWM), switching loss reduction.

I. INTRODUCTION

MULTILEVEL inverters (MLIs) exhibit improved power quality, reduced semiconductor stress, reduced electromagnetic interference (EMI) emissions, and reduced filtering requirements compared with two-level (2-L) inverters. For these reasons, MLIs have become attractive for a wide range of power applications from compressors and fans to marine propulsion and high-voltage direct-current transmission [1], [2].

With the same number of cells, a binary-cascaded multilevel inverter (BCMLI) substantially increases voltage levels as compared with an ordinary-cascaded MLI. Thus, the devices can switch under line frequency with staircase-type output while maintaining excellent output waveform quality [3], [4], [5]. To increase control response or further improve output waveform quality, a single-phase MLI can operate with the following two modulation schemes: sinusoidal pulsewidth modulation (SPWM) for improved output power quality and nearest-level modulation (NLM) for improved efficiency and reduced EMI emissions [6], [7]. Because of their relatively low computational burden, SPWM and NLM can be extended to operate three-phase MLIs. However, their inherent perphase operation requires proper synchronization and, thus, complicates the direct regulation of the common-mode voltage (CMV) present in three-phase systems [8], [9].

For three-phase MLIs, space vector pulsewidth modulation (SVPWM) operates every phase simultaneously, which provides control flexibility and facilitates its digital implementation. Thus, the regulation of the CMV and other objectives can be performed by the utilization of redundant *abc* states within vectors. Furthermore, compared with SPWM and NLM, SVPWM can increase the dc voltage utilization up to 15.5% in three-phase MLIs [10], [11], [12], [13]. SVPWM can be implemented by two-dimensional (2-D) or 3-D coordinate systems, where 2-D implementation exhibits lesser computational resources [14]. For an M-level MLI, there are $3M^2 - 3M + 1$ stationary or fundamental vectors distributed across the 2-D plane and a total number of M^3 states or possible space vectors generating those stationary vectors. Next, this scheme locates the stationary nearest three vectors (NTVs) to the rotary reference vector $\boldsymbol{v_{ref}}$ and distributes them by applying the volt-second-balancing principle. However, as M increases, the SVPWM implementation could become increasingly complex because of the M^3 available *abc* states. This problem would be exacerbated if these states were stored in lookup tables as it is typically done in 2-L inverters [13], [15]. In this regard, attempting to reduce the complexity of SVPWM implementation in MLIs, several works have been presented in recent years [15], [16], [17], [18], [19], [20], [21], [22], [23], [24].

The SVPWM of 2-L inverters based on the 2-D $\alpha\beta$ coordinate system is a mature technique that obtains the NTVs from a hexagon comprising seven vectors (from the vertexes and the zero vector). Likewise, the authors in [16], [17], [18], [19], and [20] have applied this 2-L hexagon structure to the MLIs space vector plane. As a result, the 2-L techniques to identify the NTVs and generate the switching sequences can simplify the SVPWM implementation in MLIs. Although these techniques can perform well for low M inverters, they become difficult to implement in larger Ms because of the lookup table requirement. In [21], the authors introduced a technique combining 2-D and 3-D coordinates to generate the inverter states of the NTVs without lookup tables. Yet, it does not optimize the *abc* state selection for objectives, such as CMV reduction, and requires consecutive iterations.

In [22], a transformation method from *abc* to 2-D *gh* coordinates was proposed. The method simplifies the multilevel SVPWM because the stationary vectors in the plane are represented by integer values. Thus, irrespective of the level M, identifying the NTVs can be carried out online by a digital signal processor (DSP) without lookup tables. However, Celanovic and Boroyevich [22] do not indicate how to obtain the inverter *abc* states after the NTVs are identified. Later, authors in [23] applied the *gh* coordinates to a diode clamped MLI and opted to iterate the *abc* states aiming to balance the capacitors. Similarly, Ahmed et al. [15] and Carnielutti et al. [24] iterated every possible *abc* state in NTVs to minimize switching transitions in MLIs. However, these iterative processes can burden the computational resources. In addition, a systematic approach to determine the *abc* states from the NTVs in *gh* coordinates is absent in the literature.

The CMV of a three-phase system is a crucial aspect that must be reduced to avoid deterioration of winding insulation and motor bearings and to minimize the EMI [25], [26]. Researchers in [27], [28], and [29] eliminated the CMV by employing zero CMV (ZCMV) vectors in SVPWM. However, the waveform quality and the dc voltage utilization are reduced in inverters when only ZCMV vectors are used. In [30], a reduced CMV approach that utilizes every vector in the plane was presented. It features reduced switching loss, reduced CMV, and capacitor voltage balancing capability for a T-type three-level inverter. Yet, this algorithm cannot be scaled up to larger M inverters and does not operate in the *gh* coordinate system. Nevertheless, it becomes evident that reduced CMV *abc* states throughout the sampling period could reduce the number of commutations in the inverter, improving its efficiency.

As the number of levels in a BCMLI is significantly higher than a conventional MLI given the same number of cells, its SVPWM computation needs to be efficient while maintaining the desired output waveform quality with reduced CMV. A technique operating in *gh* coordinates that can directly compute the *abc* states with reduced CMV within the NTVs is presented in this article. Thus, unnecessary iterations are avoided. In addition to the reduction in computational effort, only one vector among the NTVs is necessary for the implementation of the proposed SVPWM technique. Concurrently, analogous to NLM, nearest vector modulation (NVM) for reduced switching losses and EMI can be easily implemented. Key features of the proposed techniques are summarized as follows.

1) Reduced and constant computational burden irrespective of the number of levels M in the inverter.
2) Extensive utilization capability of the dc bus voltage to the output of the MLI.
3) Reduced CMV operation in SVPWM and NVM modes.
4) Reduced switching commutations during a sampling period for the SVPWM mode.
5) Simple identification of the nearest vector for the NVM mode, avoiding convoluted identification mechanisms [31], [32], [33].
6) Comprehensive technique suitable for both symmetrical and asymmetrical MLI topologies, eliminating the requirement of specific space vector strategies for asymmetrical structures [33], [34], [35].

The rest of this article is organized as follows. Section II introduces the CMVs that an MLI produces in the three-phase system. Section III explains the basic principles of the *gh* coordinate system. Section IV describes the proposed identification of reduced CMV *abc* states in any *gh* coordinate vector. Section V lays out the implementation procedure of the proposed method for SVPWM and NVM modes. Section VI presents the experimental validation of the technique with a BCMLI. Finally, Section VII concludes this article.

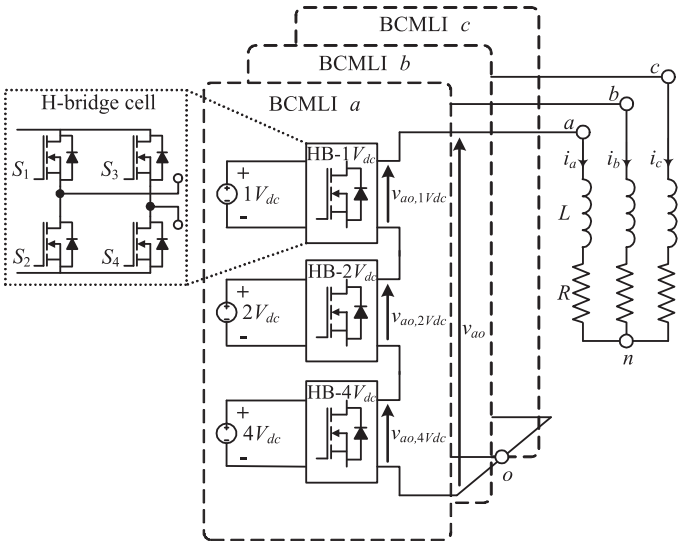

FIGURE 1. Circuit diagram of the three-phase BCMLI ($M = 15$, $p = 2$).

II. MLI AND ITS CMVS

The BCMLI portrayed, as shown in Fig. 1, is employed to verify the feasibility of the presented technique. To increase the number of output voltage levels while avoiding the added semiconductor count, the BCMLI features asymmetrical voltage sources at the H-bridges. Accordingly, a binary asymmetry implies that the H-bridges' dc voltages increase by powers of two, such as $2^0{:}2^1{:}2^2 \ldots{:}\ 2^p$, where p is defined as the binary factor of the inverter [5]. Thus, with $p = 2$, the maximum output voltage levels in the presented BCMLI are $M = 15$, which can be calculated as

$$M = 2^{p+2} - 1. \tag{1}$$

The inverter's phase output voltages must be regulated to track the *abc* reference voltages. For clarity, all voltage derivations are normalized by 1 V_{dc}, which is the base voltage of the MLI. Thus, the normalized reference voltages are given by

$$\begin{bmatrix} v_{a,ref} \\ v_{b,ref} \\ v_{c,ref} \end{bmatrix} = \frac{1}{V_{dc}} \cdot \begin{bmatrix} V_{dc} m \left((M-1)/2\right) \cos(\theta) \\ V_{dc} m \left((M-1)/2\right) \cos\left(\theta - 2\pi/3\right) \\ V_{dc} m \left((M-1)/2\right) \cos\left(\theta + 2\pi/3\right) \end{bmatrix} \tag{2}$$

where m is the reference's modulation index, $\theta = 2\pi ft$ is the reference's phase angle, and f is the output frequency.

The CMV caused by the inverter v_{cm} is determined by the difference in potential between the load's neutral point n and the common node o of the BCMLI, as depicted in Fig. 1. Equivalently, v_{cm} could be expressed as the averaged value among the inverter's phase voltages, which yields

$$v_{cm} = \frac{1}{V_{dc}} v_{no} = \frac{1}{V_{dc}} \left(\frac{v_{ao} + v_{bo} + v_{co}}{3} \right). \tag{3}$$

Considering every possible M^3 *abc* state in an MLI, there are $3M - 2$ combinations of CMV that can be generated. Subsequently, every possible CMV that the inverter could generate can be represented by the following set:

$$v_{cm} = -\frac{M-1}{2} + \frac{1}{3} j, \quad j \in \{0,\ 1,\ 2, \ldots,\ 3(M-1)\}. \tag{4}$$

Because M is an odd number, the set of CMVs above would also have an odd number of elements distributed symmetrically and separated by one-third with its center at $v_{cm} = 0$ (i.e., ZCMVs). For instance, in a three-level inverter ($M = 3$), (4) would result in the following set: $v_{cm} = \{-1, -2/3, -1/3, 0, 1/3, 2/3, 1\}$.

III. *GH* COORDINATE SYSTEM

Traditionally, $\alpha\beta$ coordinates were utilized to operate reduced-level three-phase inverters [13]. However, multilevel implementation of $\alpha\beta$ coordinates becomes increasingly complex with larger M because the total number of stationary vectors is $3M^2 - 3M + 1$, implying increasingly complex implementation as lookup tables are required.

Initially introduced in [22], the *gh* coordinate system emerged as a convenient solution for the implementation of SVPWM in MLIs. The transformation to *gh* coordinates can be generated from both line-to-line and phase voltages. For consistency within the article, the transformation from phase voltages is adopted and expressed as [15], [36]

$$\begin{bmatrix} v_g \\ v_h \\ v_o \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{5}$$

where v_g and v_h comprise the 2-D vector, and v_o represents its zero-sequence component. Notice that v_g and v_h are line-to-line voltages centered to v_b, which results in the featured 60° phase between them. For this reason and the normalized *abc* voltage values, every stationary vector in the MLI will hover on the intersection of *gh* integer coordinates.

Fig. 2 illustrates the first sector of the space vector distribution of an M-level inverter in *gh* coordinates, where all possible stationary vectors $\boldsymbol{V_Z} = [v_{g,Z},\ v_{h,Z}]^T$ are scattered across the sector. Note that, in the first sector, $v_{g,Z}$ and $v_{h,Z}$ can only have unsigned integer values as{0, 1, 2, …, M – 1}. Also, the stationary vectors at the outer layer of the sector have no redundancies ($r = 0$), indicating that there is only one combination of *abc* states in the inverter that can generate them. On the other hand, stationary vectors at the inner layers feature an increasing number of redundancies up to $r = M$ – 1 in the zero vector. The number of redundant states in any $\boldsymbol{V_Z}$ within the first sector can be determined by the following expression:

$$r = M - 1 - \left(v_{g,Z} + v_{h,Z}\right). \tag{6}$$

The NTVs can be generated online by first determining the four stationary vectors that comprise the parallelogram where

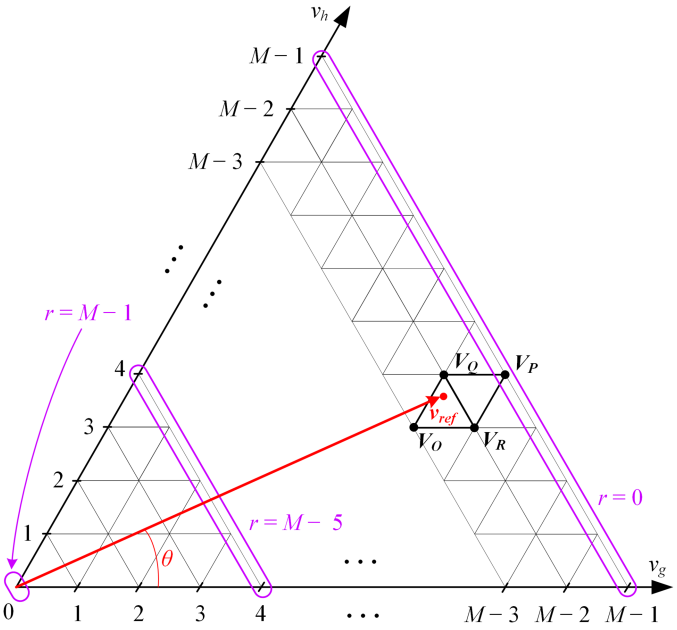

FIGURE 2. First sector of the *gh* space vector plane for an *M*-level inverter.

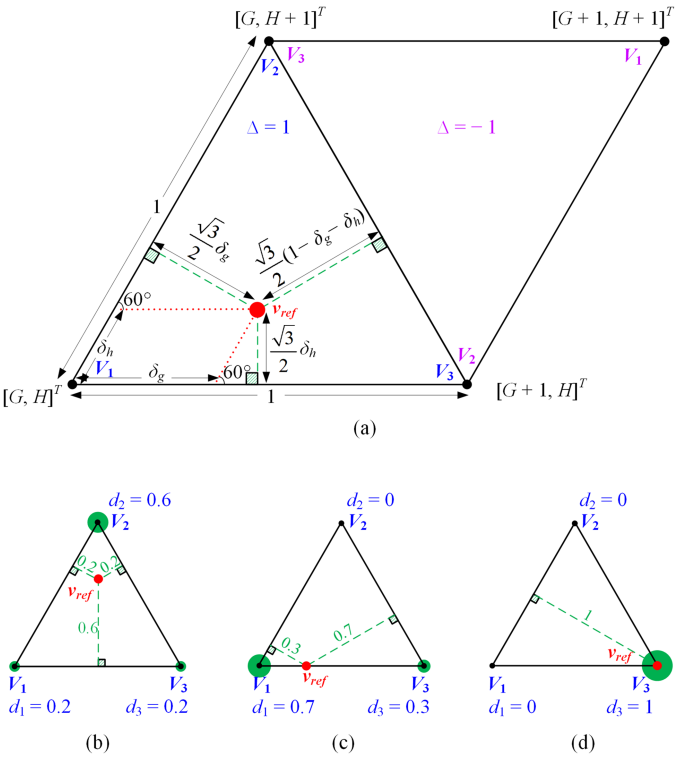

FIGURE 3. (a) Parallelogram containing the NTVs in the *gh* plane. (b), (c), and (d) Examples of the relationship between NTVs' active durations and the normalized perpendicular distances to v_{ref} when $\Delta = 1$.

$\boldsymbol{v_{ref}} = [v_{g,ref}, v_{h,ref}]^T$ is contained, which can be acquired by

$$\begin{cases} \boldsymbol{V}_O = \left[\text{floor}\left(v_{g,ref}\right),\ \text{floor}\left(v_{h,ref}\right)\right]^T \\ \boldsymbol{V}_P = \left[\text{ceil}\left(v_{g,ref}\right),\ \text{ceil}\left(v_{h,ref}\right)\right]^T \\ \boldsymbol{V}_Q = \left[\text{ceil}\left(v_{g,ref}\right),\ \text{floor}\left(v_{h,ref}\right)\right]^T \\ \boldsymbol{V}_R = \left[\text{floor}\left(v_{g,ref}\right),\ \text{ceil}\left(v_{h,ref}\right)\right]^T. \end{cases} \tag{7}$$

Thereafter, further computations with these vectors and the reference vector can narrow down the triangle containing the NTVs [15], [22], [35]. Thus, employing the *gh* coordinate system provides the ability to identify the NTVs online, which eliminates the need for lookup tables.

IV. PROPOSED TECHNIQUE IDENTIFYING REDUCED CMV STATES FOR MLIS

To retrieve the corresponding *abc* states of the inverter, previous works opted to iterate every available *abc* state in each of the NTVs to select the best one satisfying an appointed objective. Hence, the computational power is squandered particularly if larger *M* inverters were operated at low modulation indices, where *r* becomes larger. For this reason, this section presents a technique to readily identify the reduced CMV *abc* state that a *gh* stationary vector can generate. Therefore, by avoiding iterations of every possible state within the NTVs, the computational burden can be improved. Furthermore, only the identification of one vector among the NTVs is necessary for the SVPWM implementation, bolstering the reduction of computational resources. Additionally, as presented in Section V, this technique can reduce the inverter's device switching frequency.

A. NTVS AND THEIR ACTIVE DURATIONS

Fig. 3(a) illustrates an arbitrary parallelogram where the reference is located. There are two opposite direction triangles, one pointing up on the left, and the other pointing down on the right. For future reference, the order chosen for vectors $\boldsymbol{V_1}$, $\boldsymbol{V_2}$, and $\boldsymbol{V_3}$ in both triangles is important. Depending on where the triangle is located, the left-hand side $\boldsymbol{V_1}$ is located at the bottom left side, and the right-hand side $\boldsymbol{V_1}$ is at the top right side of the parallelogram. Next, to determine the triangle where the reference $\boldsymbol{v_{ref}}$ is contained, the first assumption is that it is inside the left-hand side triangle denoted by the variable $\Delta = 1$. Thus, vector $\boldsymbol{V_1}$ is first assumed as

$$\boldsymbol{V_1} = \left[v_{g,1}, v_{h,1}\right]^T = \left[\text{floor}\left(v_{g,ref}\right), \text{floor}\left(v_{h,ref}\right)\right]^T = [G, H]^T \tag{8}$$

where G and H are the arbitrary *gh* components of the bottom left side vector, as shown in Fig. 3(a). Then, the fractional segments that complement $\boldsymbol{v_{ref}}$ are calculated as

$$\begin{cases} \delta_g = \Delta \cdot \left(v_{g,ref} - v_{g,1}\right), & 0 \le \delta_g \le 1 \\ \delta_h = \Delta \cdot \left(v_{h,ref} - v_{h,1}\right), & 0 \le \delta_h \le 1. \end{cases} \tag{9}$$

Analyzing Fig. 3(a), the previous assumption holds true if $\delta_g + \delta_h < 1$. On the contrary, if $\delta_g + \delta_h > 1$, $\boldsymbol{v_{ref}}$ is inside the right-hand side triangle, which is represented by $\Delta = -1$. Consequently, $\boldsymbol{V_1}$ is readjusted by adding one unit to its *gh* components, and (9) is recalculated. In addition, the remaining

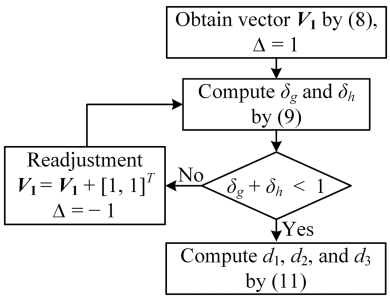

FIGURE 4. Flowchart to obtain V_1, Δ, and active durations d_1, d_2, and d_3.

two adjacent vectors could be found by the following expression:

$$\begin{cases} V_2 = V_1 + [0, \Delta]^T \\ V_3 = V_1 + [\Delta, 0]^T. \end{cases} \tag{10}$$

Once V_1 has been identified, it is essential to determine the active durations of the NTVs to realize v_{ref} by the volt-second-balancing principle for SVPWM implementation. Consequently, a geometrical approach is used to find the active durations d_1, d_2, and d_3 of the vectors V_1, V_2, and V_3, respectively. For clarity, the case $\Delta = 1$ portrayed, as shown in Fig. 3, is considered, however, the case $\Delta = -1$ would adopt the same rationale. First, note, as shown in Fig. 3(a), that the perpendicular distances in green from v_{ref} to every side of the triangle can be directly derived in terms of δ_g and δ_h by trigonometric identities. Second, regardless of the location of v_{ref} inside the unity equilateral triangle, the sum of perpendicular distances always equates to $\sqrt{3}/2$. Then, by dropping this irrational factor, the sum of perpendicular distances can be normalized to 1. Last, the active duration of any vector is equivalent to the normalized distance from its opposing side to v_{ref}. Fig. 3(b)–(d) illustrates some examples indicating the relationship between the normalized perpendicular distance and the active duration. Correspondingly, the active duration of V_1, V_2, and V_3 is equivalent to

$$\begin{cases} d_1 = 1 - \delta_g - \delta_h \\ d_2 = \delta_h \\ d_3 = \delta_g. \end{cases} \tag{11}$$

Notice that, to obtain d_1, d_2, and d_3, only V_1 and the reference vector are required, as shown in (9) and (11), which can be summarized by the flowchart, as shown in Fig. 4.

In applications where the number of levels M is considerable or switching losses and EMI emissions must be minimized, NVM becomes more convenient instead of SVPWM. Thus, among the NTVs, the closest vector V_N can be associated with the vector having the longest active duration as

$$V_N \sim \max(d_1,\ d_2,\ d_3). \tag{12}$$

Subsequently, (12) and (10) can identify the closest vector to operate the three-phase inverter by NVM as presented in Section V.

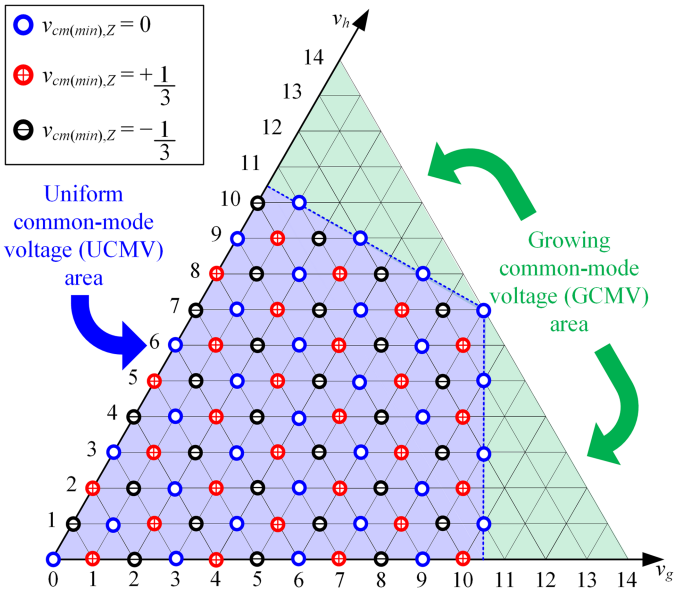

FIGURE 5. First sector of the *gh* space vector plane for an $M = 15$ level inverter and its distribution of minimum CMVs.

B. REDUCED CMV ABC STATE OF STATIONARY VECTORS IN THE GH COORDINATE SYSTEM

The zero-sequence voltage $v_{o,Z}$ linked to an arbitrary stationary vector V_Z is directly proportional to the CMV; it generates as follows:

$$v_{cm,Z} = \frac{v_{o,Z}}{3}. \tag{13}$$

Additionally, each of the $r + 1$ *abc* states contained in V_Z produces a specific CMV. Then, by manipulating (5), (6), and (13), the set of CMVs in any stationary vector can be listed by

$$v_{cm,Z} = \frac{v_{h,Z} - v_{g,Z} + 3r}{6} - k, \quad k \in \{0,\ 1,\ 2, \ldots, r\}. \tag{14}$$

The first sector of the *gh* plane for the 15-level BCMLI is depicted in Fig. 5. By iterating (14), the normalized minimum CMVs across the *gh* plane can be obtained. The minimum CMVs of the vectors inside the blue shaded area are uniformly distributed with the lowest values as follows: –1/3, 0, and 1/3. Therefore, the blue area is denoted as the uniform CMV (UCMV) area. Notice that the UCMV area would correspond to a reference voltage with $m \leq 1$. Naturally, for references with $1 < m \leq 1.155$, the NTVs may be placed in the growing CMV (GCMV) green area. Thus, the minimum CMVs would be larger than $\pm 1/3$ because the boost in dc voltage utilization depends on the injection of zero-sequence components by the three-phase inverter. Consequently, the minimum CMVs in the GCMV area could become as high as $\pm 7/3$ for the $M = 15$ level inverter [see (14)]. By (6) and (14) with $k = 0$, whether a vector V_Z is in the GCMV area is verified if the following

TABLE 1. Iterated CMVs and Calculated Minimum CMV of an Arbitrary Stationary Vector V_Z in the First Sector

V_Z	Iterating CMVs by (14)	Deriving $v_{cm(min),Z}$
$[4, 4]^T$	4, 3, 2, 1, 0, −1, −2, −3, −4	0 by (17), (18)
$[6, 2]^T$	7/3, 4/3, 1/3, −2/3, −5/3, −8/3, −11/3	1/3 by (17), (18)
$[2, 6]^T$	11/3, 8/3, 5/3, 2/3, −1/3, −4/3, −7/3	−1/3 by (17), (18)
$[11, 1]^T$	−2/3, −5/3, −8/3	−2/3 (16)
$[1, 11]^T$	8/3, 5/3, 2/3	2/3 (16)

expression is satisfied:

$$\begin{cases} \frac{3(M-1)-2v_{h,Z}-4v_{g,Z}}{6} < 0, & \text{if } v_{g,Z} > v_{h,Z} \\ \frac{3(M-1)-2v_{g,Z}-4v_{h,Z}}{6} < 0, & \text{if } v_{h,Z} > v_{g,Z}. \end{cases} \tag{15}$$

Moreover, as (15) is satisfied, it becomes the minimum CMV that a GCMV stationary vector can generate, which is given by

$$v_{cm(\min),Z} = \begin{cases} \frac{3(M-1)-2v_{h,Z}-4v_{g,Z}}{6}, & \text{if } v_{g,Z} > v_{h,Z} \\ -\frac{3(M-1)-2v_{g,Z}-4v_{h,Z}}{6}, & \text{if } v_{h,Z} > v_{g,Z}. \end{cases} \tag{16}$$

Conversely, from (14), it is possible to calculate the minimum CMV of a UCMV vector. First, if $v_{h,Z} - v_{g,Z}$ in the fractional segment of (14) is a multiple of 3, such a fraction would result in an integer. Then, there will exist a k value that causes (14) to be zero; thus $v_{cm(min),Z} = 0$. Second, if $v_{h,Z} - v_{g,Z}$ in the fractional segment of (14) is a unit larger (when $v_{h,Z} > v_{g,Z}$) or two units lower (when $v_{g,Z} > v_{h,Z}$) than a multiple of 3, there will exist a k value that yields $v_{cm(min),Z} = 1/3$. Finally, with $v_{h,Z} - v_{g,Z}$ two units larger (when $v_{h,Z} > v_{g,Z}$) or one unit lower (when $v_{g,Z} > v_{h,Z}$) than a multiple of 3, $v_{cm(min),Z} = -1/3$. Based on this principle, the following expressions can identify the minimum CMV of UCMV stationary vectors:

$$\eta = \left(v_{h,Z} - v_{g,Z}\right) (\text{mod } 3) \tag{17}$$

and

$$v_{cm(min),Z} = \begin{cases} 0, & \text{if } \eta = 0 \\ 1/3, & \text{if } \eta = 1 \text{ or } \eta = -2 \\ -1/3, & \text{if } \eta = 2 \text{ or } \eta = -1. \end{cases} \tag{18}$$

Table 1 lists some of the arbitrary gh stationary vectors $\boldsymbol{V_Z}$ in the first sector of the 15-level BCMLI with its iterated and calculated minimum CMVs. It is verified that (16), (17), and (18) can accurately compute the minimum CMV of any vector. As a result, the unique abc state associated with the $v_{cm(min),Z}$ of a vector $\boldsymbol{V_Z}$ can be generated as explained in Section V.

C. EXTENDING THE COMPUTATIONS TO FURTHER SECTORS IN THE 360° GH PLANE

The presented calculations above are valid for the first sector of the gh space vector, which corresponds to unsigned integer values in the gh stationary vectors. To utilize these computations for every sector, the vectors in further sectors (having at least one negative gh component) are virtually shifted onto the first sector. Thus, any sector would follow the same distribution, as presented in Fig. 5, allowing the utilization of the derived expressions. The sector number Y can be determined by the phase angle as

$$\begin{cases} Y = 1, & \text{if } 0° < \theta \le 60° \\ Y = 2, & \text{if } 60° < \theta \le 120° \\ Y = 3, & \text{if } 120° < \theta \le 180° \\ Y = 4, & \text{if } 180° < \theta \le 240° \\ Y = 5, & \text{if } 240° < \theta \le 300° \\ Y = 6, & \text{if } 300° < \theta \le 360°. \end{cases} \tag{19}$$

Consequently, irrespective of the sector number, the gh components would always be zero or positive and can be rewritten from (5) as

$$\begin{bmatrix} v_g \\ v_h \\ v_o \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ 1 & 1 & 1 \end{bmatrix} \cdot \boldsymbol{A}^{Y-1} \cdot \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} (-1)^{Y+1} \tag{20}$$

where

$$\boldsymbol{A} = \begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix}. \tag{21}$$

This shifting procedure can be easily implemented by storing (20) into the six conditionals of (19). $\boldsymbol{A}$ serves as a shift matrix that progressively swaps the order of the abc signals in every sector, and the sign alternating factor reverses their polarity. Thus, v_g and v_h components are always zero or positive. However, to work in any sector with immovable variables, the RST signals with subfixes R, S, and T are introduced as

$$\begin{bmatrix} v_R \\ v_S \\ v_T \end{bmatrix} = \boldsymbol{A}^{Y-1} \cdot \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} (-1)^{Y+1}$$

$$= \begin{cases} [v_a, v_b, v_c]^T, & \text{if} Y = 1 \\ [-v_c, -v_a, -v_b]^T, & \text{if} Y = 2 \\ [v_b, v_c, v_a]^T, & \text{if} Y = 3 \\ [-v_a, -v_b, -v_c]^T, & \text{if} Y = 4 \\ [v_c, v_a, v_b]^T, & \text{if} Y = 5 \\ [-v_b, -v_c, -v_a]^T, & \text{if} Y = 6. \end{cases} \tag{22}$$

Notice that the RST signals correspond to the last three factors of (20). Namely, if $Y = 1$, subfixes R, S, and T would correspond to subfixes a, b, and c, respectively. This new set of orderly subfixes is convenient when implementing the switching sequences for any sector, as presented in Section V.

V. SWITCHING SEQUENCE DESIGN AND IMPLEMENTATION OF THE PROPOSED STRATEGY

The inverter's abc state exclusive to the minimum CMV of a gh stationary vector $\boldsymbol{V_Z}$ in any sector Y can be derived by the following inverse transformation:

$$\begin{bmatrix} v_{a,Z} \\ v_{b,Z} \\ v_{c,Z} \end{bmatrix} = \frac{1}{3}(-1)^{Y+1}\boldsymbol{B}^{Y-1} \cdot \begin{bmatrix} 2 & 1 & 3 \\ -1 & 1 & 3 \\ -1 & -2 & 3 \end{bmatrix} \cdot \begin{bmatrix} v_{g,Z} \\ v_{h,Z} \\ v_{cm(min),\mathbf{Z}} \end{bmatrix} \tag{23}$$

where

$$\boldsymbol{B} = \boldsymbol{A}^{-1} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 0 & 0 \end{bmatrix}. \tag{24}$$

To illustrate the switching sequence design, the first sector is presented in this section as an example. Therefore, (23) in the first sector ($Y = 1$) can be rewritten as

$$\begin{bmatrix} v_{a,Z} \\ v_{b,Z} \\ v_{c,Z} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & 1 & 3 \\ -1 & 1 & 3 \\ -1 & -2 & 3 \end{bmatrix} \begin{bmatrix} v_{g,Z} \\ v_{h,Z} \\ v_{cm(min),\mathbf{Z}} \end{bmatrix}. \tag{25}$$

As a result, signals a, b, and c correspond to R, S, and T, respectively. Given that the following analyses happen in the first sector ($R = a$, $S = b$, $T = c$), the abc signals are employed to better elucidate the design and implementation of the switching sequences.

A. SWITCHING SEQUENCE DESIGN OF SVPWM

A small portion of the first sector of the gh plane corresponding to the UCMV area for the 15-level BCMLI is depicted in Fig. 6(a), where $8 \leq v_g \leq 10$ and $0 \leq v_h \leq 2$. In addition, from (25), the corresponding 3-D abc states are acquired and displayed in magenta. Notice that there is always one clamped phase inside the triangles, which provides an alternative to reduce the device switching frequency. However, the appropriate switching sequence must be appointed to have minimum commutations in the active phases. This can be accomplished by first applying the vector with $v_{cm(min)} = 1/3$, next the vector with $v_{cm(min)} = 0$, and finally, the $v_{cm(min)} = -1/3$ vector. Under this principle, the order of the vectors $\boldsymbol{V_1}$, $\boldsymbol{V_2}$, and $\boldsymbol{V_3}$ within the sequence can be determined. The case of clamped phase-a is taken as an example to illustrate the switching sequence design. When phase-a is clamped and $\Delta = 1$, as depicted in Fig. 6(a), $\boldsymbol{V_1}$ [see Fig. 3(a)] corresponds to the first vector with $v_{cm(min)} = 1/3$, $\boldsymbol{V_2}$ to the second vector with $v_{cm(min)} = 0$, and $\boldsymbol{V_3}$ to the third vector with $v_{cm(min)} = -1/3$. Thus, the symmetrical sequence can be realized with five segments by $\boldsymbol{V_1} \rightarrow \boldsymbol{V_2} \rightarrow \boldsymbol{V_3} \rightarrow \boldsymbol{V_2} \rightarrow \boldsymbol{V_1}$. On the other hand, when phase-a is clamped and $\Delta = -1$, the vector with $v_{cm(min)} = 1/3$ is $\boldsymbol{V_3}$ [see Figs. 3(a) and 6(a)], the vector with $v_{cm(min)} = 0$ is $\boldsymbol{V_2}$, and $\boldsymbol{V_1}$ is the vector with $v_{cm(min)} = -1/3$. As a result, the symmetrical sequence can be realized by ordering the five segments as $\boldsymbol{V_3} \rightarrow \boldsymbol{V_2} \rightarrow \boldsymbol{V_1} \rightarrow \boldsymbol{V_2} \rightarrow \boldsymbol{V_3}$.

In the case of the GCMV area, two small portions of the first sector for the cases $v_{g,Z} > v_{h,Z}$ and $v_{h,Z} > v_{g,Z}$ are depicted in Fig. 6(b) and (c), respectively. Equivalent to the UCMV case, the sequences that minimize the commutations in the active phases are also depicted for the GCMV area. As shown in Fig. 6(b), if $v_{g,Z} > v_{h,Z}$, the phase-a is always clamped. Conversely, as seen in Fig. 6(c), phase-c is clamped if $v_{h,Z} > v_{g,Z}$. Note that phase-b is never clamped throughout the GCMV area of the first sector. Yet, all phases will exchange their commutation profiles at subsequent sectors, balancing the clamped and active stages of every phase across the 360° gh plane.

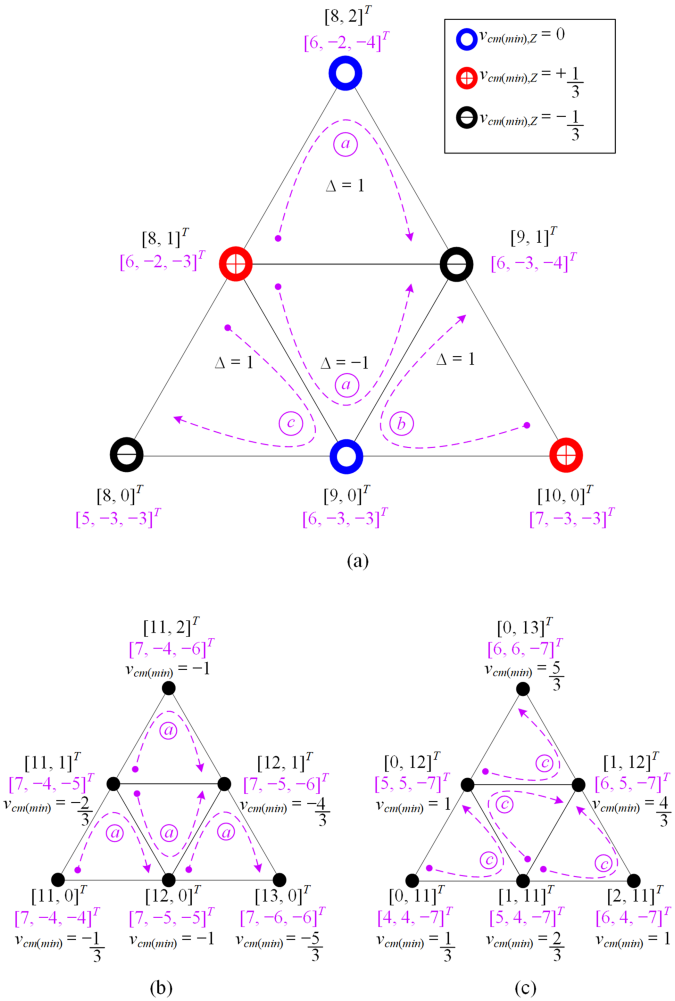

FIGURE 6. ***gh*** **plane portions of the** $M = 15$ **inverter's first sector. (a) Portion in the UCMV area and vector sequences. Portion in the GCMV area and vector sequences when (b)** $v_{g,Z} > v_{h,Z}$ **and (c)** $v_{h,Z} > v_{g,Z}$**.**

B. CARRIER IMPLEMENTATION OF SVPWM

The carrier implementation of the switching sequence is presented in Fig. 7 for the clamped phase-a case and both triangle types. The carrier is a symmetrical triangular wave with frequency $f_s = 1/T_s$. The previously designed sequences can be seen in the dynamic switching states s_a, s_b, and $s_c \in \{0, 1\}$. To implement the sequences, these dynamic switching states are referenced to the constant states (or floor level states) N_a, N_b, and $N_c \in \{0, \pm 1, \pm 2, \ldots, \pm [-1+(M-1)/2]\}$. Thus, the normalized switched output voltage of the inverter can be realized by these two components as follows:

$$\begin{bmatrix} v_{a,sw} \\ v_{b,sw} \\ v_{c,sw} \end{bmatrix} = \frac{1}{V_{dc}} \begin{bmatrix} v_{ao} \\ v_{bo} \\ v_{co} \end{bmatrix} = \begin{bmatrix} N_a \\ N_b \\ N_c \end{bmatrix} + \begin{bmatrix} s_a \\ s_b \\ s_c \end{bmatrix}. \tag{26}$$

The constant states can be obtained by exclusively evaluating the abc states of $\boldsymbol{V_1}$ ($[v_{a,1}, v_{b,1}, v_{c,1}]^T$) obtained from (25). As seen in the switching sequence of Fig. 7(a) for $\Delta = 1$, $\boldsymbol{V_1}$

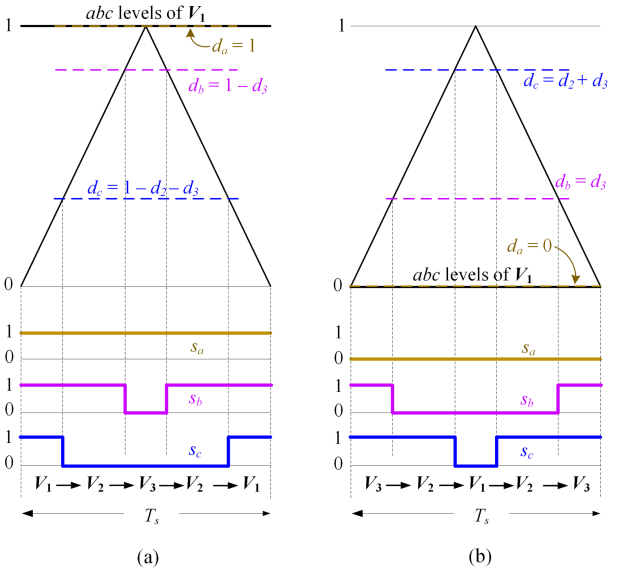

FIGURE 7. Switching sequence and carrier implementation when phase-*a* is clamped. (a) $\Delta = 1$. (b) $\Delta = -1$.

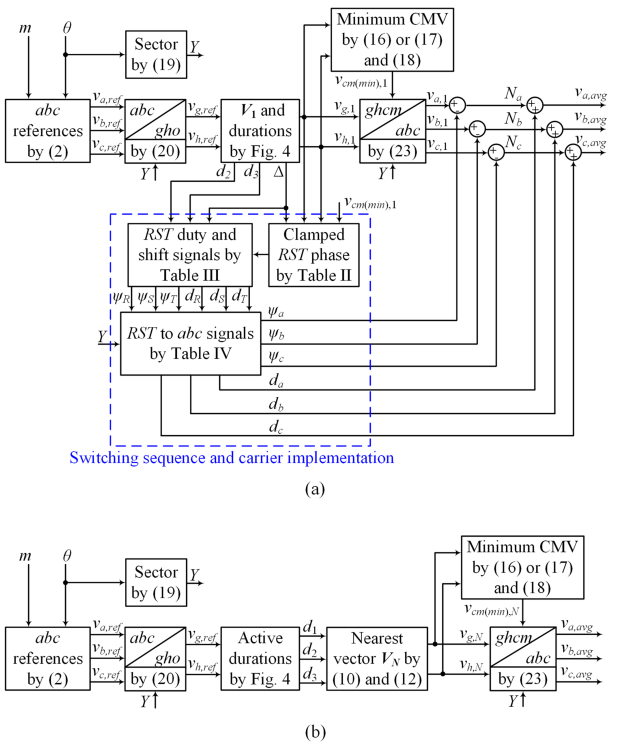

FIGURE 8. Proposed technique implementation modes. (a) SVPWM. (b) NVM.

corresponds to all ON states in s_a, s_b, and s_c, which means that $[v_{a,1}, v_{b,1}, v_{c,1}]^T$ would be placed on top of the carrier. Therefore, all phases must be shifted one unit down to obtain the constant states. As a result, the constant states are obtained by applying the level shift $[\psi_a, \psi_b, \psi_c]^T = [1], [1], [1]^T$ as

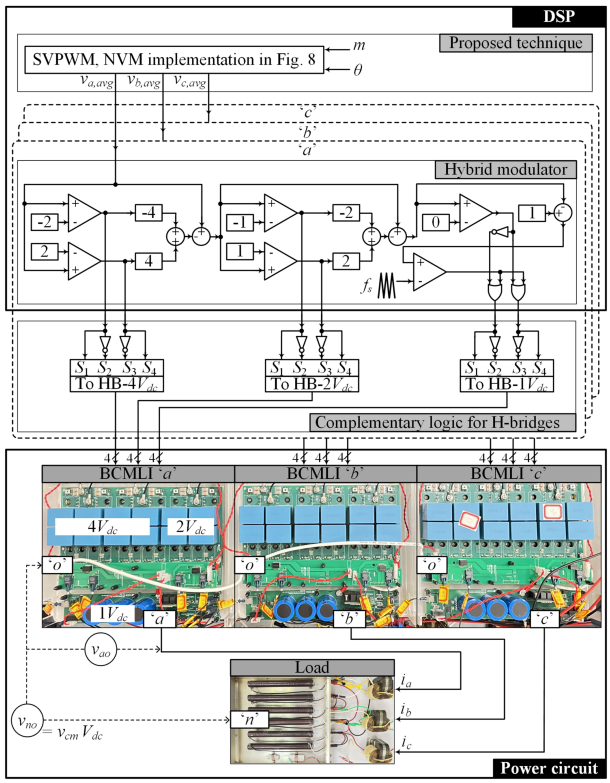

FIGURE 9. Comprehensive block diagram for the experimental implementation of the proposed method in the three-phase $M = 15$ BCMLI.

follows:

$$\begin{bmatrix} N_a \\ N_b \\ N_c \end{bmatrix} = \begin{bmatrix} v_{a,1} \\ v_{b,1} \\ v_{c,1} \end{bmatrix} - \begin{bmatrix} \psi_a \\ \psi_b \\ \psi_c \end{bmatrix}. \tag{27}$$

Once the constant levels N_a, N_b, and N_c have been determined, the duty cycle signals d_a, d_b, and d_c can be calculated to generate the sequence. First, since s_a is always on during the sequence, $d_a = 1$. Second, s_b turns OFF to generate only $\boldsymbol{V_3}$; thus, $d_b = 1 - d_3$. Finally, s_c turns OFF to generate the vectors $\boldsymbol{V_2}$ and $\boldsymbol{V_3}$; hence, $d_c = 1 - d_2 - d_3$. On the other hand, Fig. 7(b) displays the case of clamped phase-*a* and $\Delta = -1$. In this scenario, the constant states N_a, N_b, and N_c match $[v_{a,1}, v_{b,1}, v_{c,1}]^T$ because s_a, s_b, and s_c are always OFF during $\boldsymbol{V_1}$. Thus, the constant states in (27) are obtained with $[\psi_a, \psi_b, \psi_c]^T = [0, 0, 0]^T$. Correspondingly, $d_a = 0$ because s_a is OFF during the sequence, $d_b = d_3$ because s_b turns ON to generate $\boldsymbol{V_3}$, and $d_c = d_2 + d_3$ because s_c turns ON to generate $\boldsymbol{V_2}$ and $\boldsymbol{V_3}$.

As presented above, the switching sequences s_a, s_b, and s_c can be generated by manipulating $\boldsymbol{V_1}$, d_2, and d_3. Yet, the presented procedure to obtain d_a, d_b, and d_c represents the case of clamped phase-*a* in the first sector. Therefore, to properly construct d_a, d_b, and d_c, in any case, it is essential to identify the clamped phase in the NTVs. As previously explained in Fig. 6(b) and (c) for the GCMV area, the criterion $v_{g,1} > v_{h,1}$ or $v_{h,1} > v_{g,1}$ is sufficient to identify the clamped

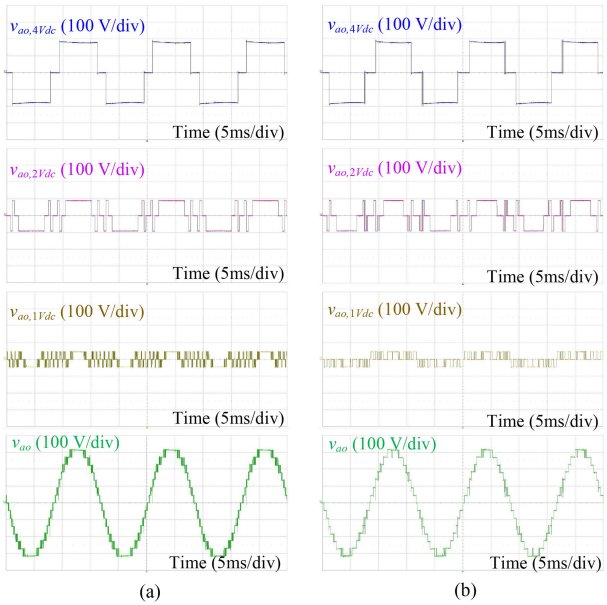

FIGURE 10. Partial and total voltages in phase-*a* produced by the hybrid modulator in the BCMLI 1:2:4 ($p = 2$) under (a) SVPWM mode and (b) NVM mode with $m = 1$.

TABLE 2. Determination of the Clamped Phase in the NTVs by Assessment of V_1 in the 360° Plane

Area by (15)	Assessment	Clamped phase
UCMV	$\lambda = 1$ by (28)	$R = a$, for ($Y = 1$)
UCMV	$\lambda = 0$ by (28)	$S = b$, for ($Y = 1$)
UCMV	$\lambda = -1$ by (28)	$T = c$, for ($Y = 1$)
GCMV	$v_{g,1} > v_{h,1}$	$R = a$, for ($Y = 1$)
GCMV	$v_{h,1} > v_{g,1}$	$T = c$, for ($Y = 1$)

phase. However, for the UCMV area case, an additional step is required. Once again, $\boldsymbol{V_1}$ can be used to identify the clamped phase by evaluating its minimum CMV and the triangle type that contains it. Subsequently, the clamping factor λ can be defined as

$$\lambda = \text{sign}\left(\Delta \cdot v_{cm(min),1}\right). \tag{28}$$

Carrying on with the first sector case, if $\lambda = 1$, then phase-*a* is clamped; if $\lambda = 0$, then phase-*b* is clamped; if $\lambda = -1$, then phase-*c* is clamped. These scenarios can be verified in Fig. 6(a). Additionally, employing the relationship between the *abc* and *RST* signals in (22), the clamped *RST* phase can be determined for any sector as presented in Table 2. Note that only calculations involving $\boldsymbol{V_1}$ are needed to identify the clamped phase within any NTVs.

For any sector in the 360° plane, once the clamped *RST* phase has been identified, the algorithm assigns the level shift $[\psi_R, \psi_S, \psi_T]^T$ values accordingly. Subsequently, the duty cycle signals d_R, d_S, and d_T can be generated employing $[\psi_R, \psi_S, \psi_T]^T$, the vectors' active durations, and Δ for any sector, as presented in Table 3. The first sector case, as shown in Fig. 7, can be verified in Table 3 by substituting the subfixes *R*, *S*, and *T* with *a*, *b*, and *c*, respectively. Finally, Table 4 shows the generalized procedure to retrieve the *abc* signals from the immovable *RST* signals. The displayed shift and polarity reversal of the *RST* signals to retrieve the *abc* signals per sector can be corroborated with the relationship between these signals presented in (22).

C. IMPLEMENTATION OF THE PROPOSED TECHNIQUE WITH SVPWM AND NVM

The presented technique for identification of the reduced CMV states with reduced computational burden and the device switching frequency is implemented, as shown in Fig. 8. In a nutshell, the technique takes the reference parameters *m* and θ and generates the averaged *abc* reference voltage signals for carrier implementation, which are obtained as follows:

$$\begin{bmatrix} v_{a,avg} \\ v_{b,avg} \\ v_{c,avg} \end{bmatrix} = \begin{bmatrix} N_a \\ N_b \\ N_c \end{bmatrix} + \begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix}. \tag{29}$$

As mentioned in Section IV, the modulation can be implemented in two manners: SVPWM and NVM. Fig. 8(a) depicts the SVPWM implementation, where it becomes clear that $\boldsymbol{V_1}$, Δ, d_2, and d_3 are sufficient to obtain the averaged *abc* reference voltages. Concurrently, the NVM can be easily realized by identifying the closest vector $\boldsymbol{V_N}$ in Fig. 8(b). Of course, because d_a, d_b, and d_c are zero in NVM, the *abc* reference voltages would always have integer values.

VI. EXPERIMENTAL VERIFICATION

Although the proposed technique can operate in both asymmetrical and symmetrical MLI topologies, the asymmetrical BCMLI, as shown in Fig. 1, is more advantageous due to the reduced switching and, thus, is employed in the experimental verification. Utilizing the system parameters listed in Table 5, Fig. 9 depicts the complete block diagram of the experimental setup employed to verify the effectiveness of the proposed technique. The DSP unit (TMS320F28377D) executes the proposed technique and performs the three-phase hybrid modulation via its pulsewidth modulation channels. Following this, the hybrid modulator operates the BCMLI in such a manner that only the HB-1V_{dc} (cell with the lowest dc voltage in the asymmetrical structure) is allowed to commutate at the switching frequency f_s, if required [37]. Although SVPWM satisfactorily operates with a low f_s value, it has been set to 10 kHz aiming at a high resolution in the stepping of NVM with large *M*. Because of the low computational burden of the proposed methods, f_s could be much higher when NVM is implemented in converters with considerably large *M*. Finally, the output signals of the hybrid modulators are sent to a logic interface to generate the complementary signals for the gate drivers of the three-phase BCMLI.

The partial and total output voltage waveforms of phase-*a* produced by the hybrid modulator are illustrated in Fig. 10 under $m = 1$. Notice that, in the SVPWM case, as shown in Fig. 10(a), only the HB-1V_{dc} cell can commutate at the switching frequency. However, because of the commutation

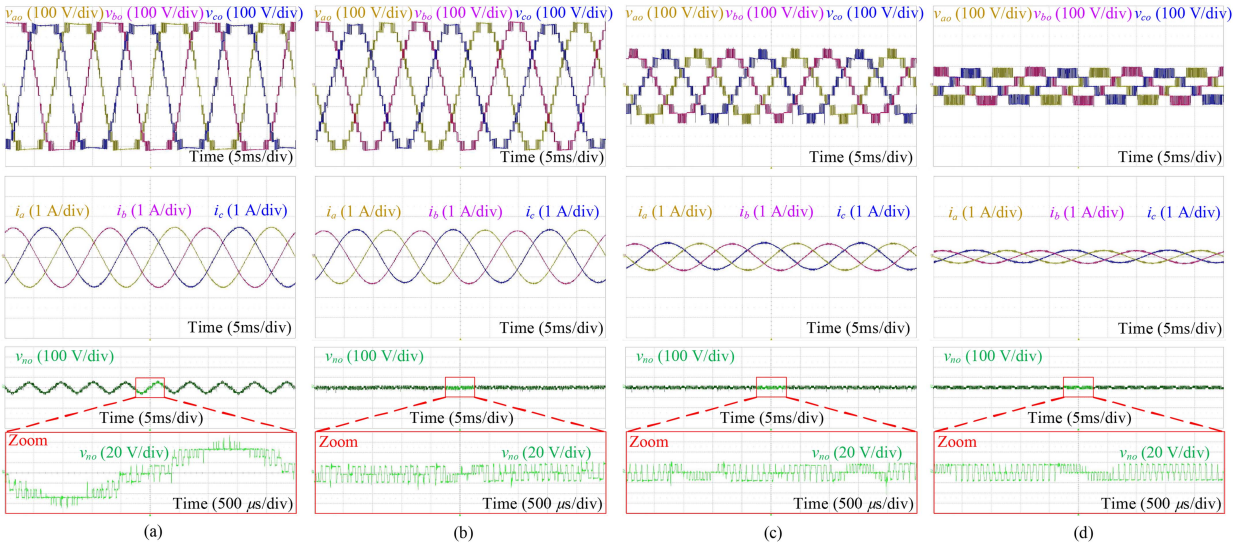

FIGURE 11. Steady-state output waveforms of the SVPWM mode with (a) $m = 1.15$, (b) $m = 1$, (c) $m = 0.5$, and (d) $m = 0.25$.

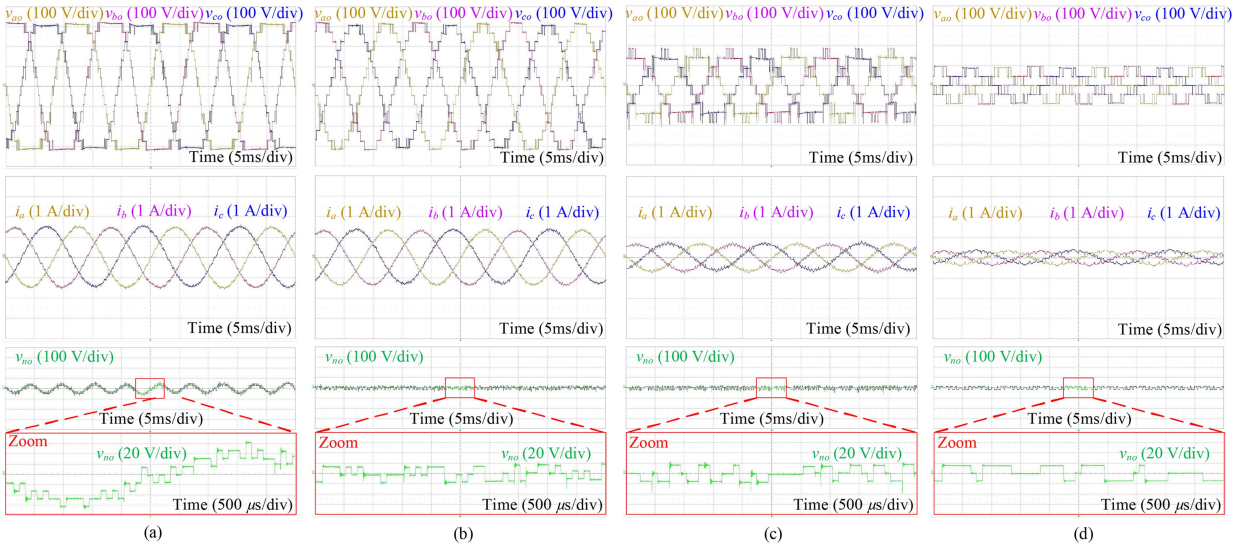

FIGURE 12. Steady-state output waveforms of the NVM mode with (a) $m = 1.15$, (b) $m = 1$, (c) $m = 0.5$, and (d) $m = 0.25$.

TABLE 3. Determination of the *RST* Duty Cycle Signals in the 360° Plane

Clamped phase	Triangle type (Δ)	Level shift			Duty cycle signals			Switching sequence
		ψ_R	ψ_S	ψ_T	d_R	d_S	d_T	
R	1	1	1	1	ψ_R	$\psi_S - \Delta.d_3$	$\psi_T - \Delta.(d_2 + d_3)$	$V_1 \rightarrow V_2 \rightarrow V_3 \rightarrow V_2 \rightarrow V_1$
R	−1	0	0	0	ψ_R	$\psi_S - \Delta.d_3$	$\psi_T - \Delta.(d_2 + d_3)$	$V_3 \rightarrow V_2 \rightarrow V_1 \rightarrow V_2 \rightarrow V_3$
S	1	0	0	1	$\psi_R + \Delta.d_3$	ψ_S	$\psi_T - \Delta.d_2$	$V_3 \rightarrow V_1 \rightarrow V_2 \rightarrow V_1 \rightarrow V_3$
S	−1	1	0	0	$\psi_R + \Delta.d_3$	ψ_S	$\psi_T - \Delta.d_2$	$V_2 \rightarrow V_1 \rightarrow V_3 \rightarrow V_1 \rightarrow V_2$
T	1	0	0	0	$\psi_R + \Delta.(d_2 + d_3)$	$\psi_S + \Delta.d_2$	ψ_T	$V_2 \rightarrow V_3 \rightarrow V_1 \rightarrow V_3 \rightarrow V_2$
T	−1	1	1	1	$\psi_R + \Delta.(d_2 + d_3)$	$\psi_S + \Delta.d_2$	ψ_T	$V_1 \rightarrow V_3 \rightarrow V_2 \rightarrow V_3 \rightarrow V_1$

feature of the proposed technique, there are regions where the output of the phase-a HB-1V_{dc} cell is clamped (simultaneously, the other two phases' HB-1V_{dc} cells commutate). Thus, the average switching frequency observed in the output voltage of each phase of the inverter is about 67% of f_s. Alternatively, Fig. 10(b) plots the voltage waveforms when the NVM mode is implemented. Clearly, the output voltage's switching frequency is much lower than in the SVPWM case. In the best-case scenario, the average switching frequency of the output voltage with NVM would approximate that of the NLM ($M \times f = 900$ Hz). Yet, because NVM steps with vectors instead of levels, additional commutations may occur in the phase voltage, as observed in Fig. 10(b). This yields a variable

TABLE 4. Determination of the *abc* Duty Cycle Signals for Each Sector in the 360° Plane

Sector (Y)	d_a	d_b	d_c	ψ_a	ψ_b	ψ_c
1	d_R	d_S	d_T	ψ_R	ψ_S	ψ_T
2	$-d_S$	$-d_T$	$-d_R$	$-\psi_S$	$-\psi_T$	$-\psi_R$
3	d_T	d_R	d_S	ψ_T	ψ_R	ψ_S
4	$-d_R$	$-d_S$	$-d_T$	$-\psi_R$	$-\psi_S$	$-\psi_T$
5	d_S	d_T	d_R	ψ_S	ψ_T	ψ_R
6	$-d_T$	$-d_R$	$-d_S$	$-\psi_T$	$-\psi_R$	$-\psi_S$

TABLE 5. System Parameters

Symbol	Parameter	Value
V_{dc}	BCMLI's base voltage	45 V
v_{ao}	Phase-a voltage ($m = 1$)	220 V
P_{out}	Output power ($m = 1$)	600 W
R	Load Resistance	240 Ω
L	Load Inductance	9 mH
f	Output frequency	60 Hz
f_s	Carrier frequency	10 kHz

average switching frequency slightly higher than $M \times f$, yet much lower than f_s.

Fig. 11 presents the steady-state operation of the proposed method under SVPWM operation with $m = 1.15$, $m = 1$, $m = 0.5$, and $m = 0.25$. In every case, the three-phase output voltages and currents were measured, showing the balanced operation of the inverter. Additionally, the CMV (v_{no}) is maintained within the reduced boundary of $\pm 1/3 V_{dc}$ (± 15 V), as shown in Fig. 11(b)–(d). For the case of $m = 1.15$, as shown in Fig. 11(a), the CMV is reduced as much as possible while allowing the maximization of the dc bus voltage utilization by zero-sequence voltage injection. Because of this, the total harmonic distortion (THD) is 13.8% in the phase voltages. The steady-state operation of the NVM mode for the same modulation indices is depicted in Fig. 12. Overall, the reduced CMV and balanced three-phase operation performance are equal to the SVPWM mode. Nevertheless, the reduced commutation profile of the NVM modes reduces the losses and EMI emissions because reduced switching frequency appears at the CMV. Also, the power quality is comparable to that of the SVPWM mode when the modulation index is large, which also implies that NVM could be satisfactorily implemented to large M inverters. The power quality profile of both methods can be observed in Fig. 13, where harmonic contents and THD for Figs. 11 and 12 are displayed and compared.

The step-up response of the inverter's output waveforms with the proposed technique from $m = 0.5$ to $m = 1.155$ (maximum dc voltage utilization) is illustrated in Fig. 14. Initially, for both SVPWM and NVM modes, the inverter only outputs nine voltage levels, yet the CMV is kept between the designed boundaries of ± 15 V. However, after stepping up to $m = 1.15$, 15 levels are featured while the boundaries of the CMV increase to maximize the dc bus voltage utilization, allowing larger currents to flow to the load. Clearly, any change in the reference vector can be tracked immediately for both SVPWM and NVM modes, as observed in Fig. 14.

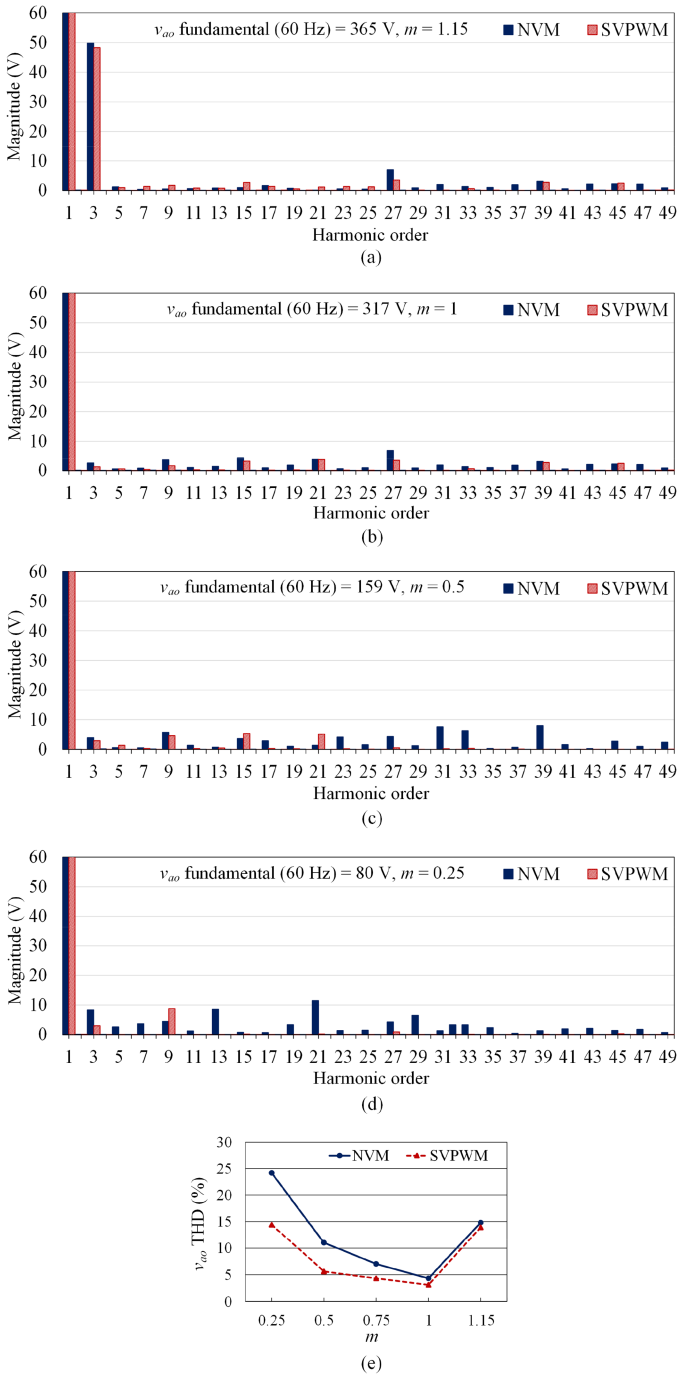

FIGURE 13. Power quality of the NVM and SVPWM methods. FFT results with (a) $m = 1.15$, (b) $m = 1$, (c) $m = 0.5$, and (d) $m = 0.25$. (e) Overall THD comparison.

A comprehensive comparison of the proposed techniques with previous works has been listed in Table 6. The calculation time in the DSP was measured as 5.4 μs for the SVPWM mode, as shown in Fig. 8(a), whereas the NVM mode, as shown in Fig. 8(b), took 5 μs for completion. Thus, both operation modes consume reduced computational resources

TABLE 6. Comparison of the Proposed Techniques With Previously Reported Space Vector Techniques

Technique	Calculation time TMS320F28377D	Calculation time affected by levels M	Selection of *abc* states in the switching sequence	Maximum v_{cm} (m <1)	Maximum m	Average phase switching frequency
SVPWM [21]	35 μs (M = 5)	Yes	Online: Reduced Iterations	Unbounded	1.155	f_S
SVPWM [35]	27.7 μs (M = 7)	Yes	Online: Iterations and carrier-based modulation	Unbounded	1.155	f_S
SVPWM [29]	9.9 μs (M = 9)	No	Online: Directly by three vectors	0	1	f_S
Proposed SVPWM	5.3 μs (M = 15)	No	Online: Directly by single vector	±1/3	1.155	$2f_S/3$
Proposed NVM	5 μs (M = 15)	No	Online: Directly by single vector	±1/3	1.155	> M×f (m = 1)

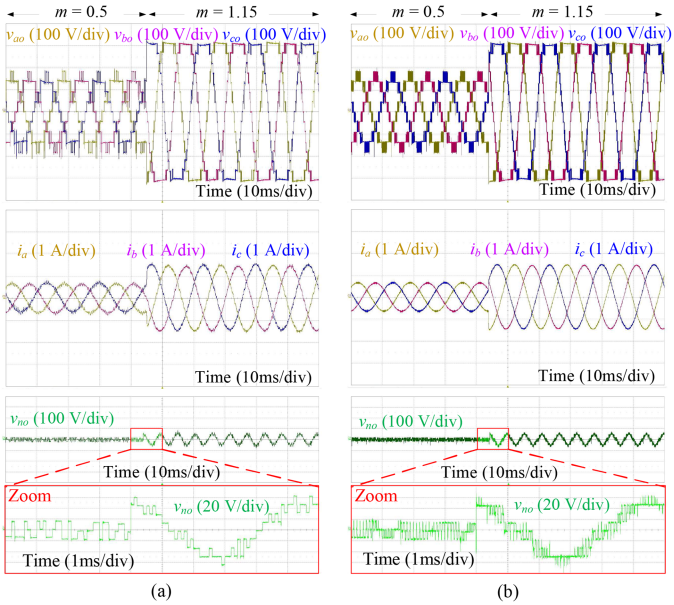

FIGURE 14. Step-up response waveforms from m = 0.5 to m = 1.15 under (a) NVM mode and (b) SVPWM mode.

compared with previous techniques. Additionally, their calculation time would not be affected if they were implemented in larger M-level inverters. Also, unlike the technique in [29], the proposed SVPWM technique realizes the modulation with reduced CMV states from a single vector, which further simplifies the computations. If further redundancies were required, such reduced CMV states could be taken as a base to generate the additional redundant states. The proposed techniques have full dc bus voltage utilization capability while limiting the CMV to the minimum required for $1 < m \leq 1.15$ and to $\pm 1/3$ for $m \leq 1$. Finally, as explained in Fig. 10, the proposed techniques feature reduced phase voltage average switching frequency (reduced commutations) compared with other techniques. Thus, they are suitable for large M inverters, where the NVM mode could be used during large m, while the SPWVM mode could be used for low m, to maintain high power quality in some applications.

VII. CONCLUSION

A reduced CMV technique for fast online identification of the inverter's *abc* state in a single *gh* stationary vector among the NTVs has been developed for a high number of levels. The initial effort was to apply the technique to a BCMLI, but the same technique can also be used for a conventional MLI to reduce the computational effort regardless of the number of levels in the MLI. Furthermore, the implementation of reduced CMV SVPWM clamps one phase while switching the remaining two phases every sampling period, which reduces the commutations in the devices. Additionally, a simple implementation of NVM can be performed with the reduced CMV technique for further reduction in switching losses and EMI emissions. Both NVM and SVPWM implementation modes do not lose the dc bus voltage utilization. Overall, the presented technique features implementation flexibility for both symmetrical and asymmetrical MLIs. The experimental work was performed in the asymmetrical BCMLI, which verified the feasibility of the proposed technique.

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