

Single-Sourced Double-Stage Multilevel Inverter for Grid-Connected Solar PV Systems

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ABSTRACT Design challenges for grid-connected solar photovoltaic systems related to the power conditioning units are power quality, efficiency, reliability, cost of implementation, etc. This article deals with a single dc-source-based double level-doubling network high-resolution multilevel inverter topology with the appropriate blend of switches to address most of the practical constraints of central inverter application. A two-stage high-resolution multilevel inverter solution is adapted to double the inverter utilization as well as to increase efficiency. Reactive power handling and fault blocking capability of the system are also demonstrated in this work. The converter is extensively simulated using MATLAB/Simulink. Experimental results from the laboratory prototype confirm the usefulness of the proposed concepts.

INDEX TERMS Central inverter, grid-connected PV inverter, high-frequency switching, level doubling network (LDN), maximum power point tracking (MPPT), multilevel inverter, photovoltaic (PV).

I. INTRODUCTION

The growing demands for energy and environmental emissions due to pollution encourage research and substantial investments related to green energy sources in the world.

A photovoltaic (PV) inverter is one of the most important components of the PV system [1], [2], [3]. Current research focuses on the development of different topologies for inverters to achieve high power quality, efficiency, reliability, and power handling capability to support the grid with the limited number of components [4].

In this article, PV inverters for large-scale solar PV applications (multi-mega-watt (MW) scale) are investigated. One of the bottlenecks for such an inverter is that the solar PV array voltage has to be restricted between 600–900 V due to the insulation limit of PV modules [5], [6]. For multi-MW power rating of a system, if the voltage is limited to a few hundreds of volt, then the current has to be in the kiloampere range. In order to maintain power quality with reasonable filter size, the grid-connected inverter needs to operate at substantially high switching frequency. Chopping high current at higher frequency generates very high switching losses in the power electronic converters. This trades off not only with the efficiency [7] but also with the reliability. The switching losses

get dissipated in the device and cause the temperature to rise significantly that reduces reliability.

A two-level inverter is cost effective; however, to get reasonable power quality with limited filter size, high-frequency operation is required [8], [9]. Due to this high frequency, switching losses will be more and this will be manifested in terms of increase in the temperature or heat dissipation of device. Hence, this inverter trades off not only with power quality but also with reliability. Other option is to use the same two-level inverter with large filter [10] but cost, volume, and losses in the filter increases several times. The two-level inverter produces large dv/dt , electromagnetic interference, and harmonic distortion in comparison with multilevel inverters. In multilevel inverters, as number of levels increases, it brings down the switching frequency. This gives motivation for investigation on multilevel inverters, where low-voltage switches can be used and can effectively bring down the filter size [11].

Due to simplicity and relatively lower filter losses, three-level neutral point clamp (NPC) inverters are being developed for solar PV applications [12], [13]. NPC inverters [14], [15] do not produce common mode current, so they are widely adapted in PV applications compared to the two-level

inverters. The major disadvantage of this converter is that it requires an input of double voltage (for same ac output voltage) compared to the full-bridge inverter. This three-level converter also necessitates the use of a high-frequency grid filter such as that in an H bridge inverter.

High-performance PV inverters, such as the cascaded H-bridge (CHB) converter [16], [17] and the modular multilevel converter (MMC) [18], [19], have been developed to provide a greater number of output voltage levels, as well as high efficiency, reliability, and modularity.

The CHB configuration requires multiple PV arrays to feed different H-bridges [20], [21]. If the PV array is divided in multiple small arrays, then it requires much higher number of cable sets to be drawn from the field. It causes higher amount of installation cost and interarray leakage current due to the leakage capacitance of the PV modules between its terminal and frame. Symmetrical CHB is also not suitable to use for PV applications as a large number of substrings (that work at higher switching frequency) are required to maintain power quality.

An unbalanced power generation among the phases due to partial shading, different temperature on the cells, dust, etc., is the critical problem in the CHB converter [22]. It can lead to power mismatch in the phases. To solve this issue, various methods are proposed in [23], [24], [25], [26], and [27]. Use of cascaded H6 configuration is reported to address the problem of unequal duty cycle in power cells that provides higher power quality. This problem of power mismatch is solved by injecting the zero-sequence voltage (ZSV) in each phase [25], [26]. The ZSV exchanges active and reactive power among the phases and helps in injecting balanced power in the grid. In this article, the ZSV is calculated by considering active and reactive power supplying to the grid. By exchanging the reactive power with the grid can extend the capability of CHB in terms of supplying the balance active power into the grid. A novel configuration is presented in which the star-connected CHB-MLI is replaced with a delta connection [27]. It improves power balancing capabilities by allowing it to operate at low irradiances without current and voltage overrating.

In comparison to CHB topologies, the MMC has better capacity to deal with issues such as unbalanced power generation [28], [29], [30], [31], [32]. A novel MMC architecture coupled with a PV array with capability of having maximum power point tracking (MPPT) control without the use of a dc-dc converter is reported in [28]. It reduces losses and implementation cost. However, this topology poses a challenge regarding galvanic isolation. The proposed methodology in [29] and [30] produces balanced arm current for MMCs during power mismatch and various grid faults to enhance system reliability. A novel Z-type MMC with self-balanced capacitors is reported in [33]. Power loss associated with the balancing circuit is reduced in this work.

Switched capacitor transformerless inverters for a grid-connected PV fed system are proposed in [34], [35], and [36]. These converters have voltage boosting capability and can eliminate the problem of leakage current. A switched

capacitor converter [37] for NPC-MLI is proposed in [29], which requires only one dc source and is fed by a PV array for a grid-connected system to provide a cost-effective solution.

In an asymmetrical multilevel inverter [38], [39], [40], [41], [42], it is found that different amount of power to be fetched from individual PV array. Specially, when system is operating under partial shading, then the difference of power causes larger PV array to divert from MPPT to maintain power quality and many times it causes unbalancing. In asymmetric MLI, low-voltage arrays cannot be connected to PV as they create the issue of interarray leakage current and uneven power distribution ratio that also vary with different modulation indexes.

As compared to CHB topologies, the MMC offers high scalability, modularity, and increased capability to handle unbalanced situations [43]. A circuit architecture for PV-fed grid integration has been developed in [44] to replace arm inductors with open-end transformers, which decreases voltage stress and rating of devices. A review on various single dc-source-based multilevel inverter topologies has been done in [45]. The analysis is reported on the basis of number of levels, voltage rating, number of semiconductor devices, number of dc sources, and its applications.

In the literature using the concept of level doubling network (LDN) derived topologies [46], power sharing of lower voltage bridges is significantly reduced compared to other asymmetric MLI topologies. In this work, 1:7 ratio of asymmetry is used to get higher number of output voltage levels. Main bridge is fed by a common PV array and isolated sources are used to feed auxiliary bridges. Although the power required by these isolated sources is very less, it is reflected in total system cost. These isolated sources have been removed with the help of a low-gain PI controller [47]. In this converter, only main bridge is fed by dc source. For grid-connected solar PV applications, all the main bridges are merged with the help of transformers and fed by a common PV array. As three dc buses are combined, there will be no mismatch during unbalancing. Hence, system will not deviate from MPPT and power quality will be maintained. Boost converter is used in between PV and inverter. This two-stage converter helps to nearly double the power handling capacity of inverter as compared to single-stage converters. The following points are discussed throughout this article.

- 1) A high-resolution double LDN-based multilevel inverter is used for a two-stage grid-connected solar PV inverter. This configuration not only brings additional flexibility in control circuit but also almost doubles the power handling capacity of the inverter stacks by adding a dc-dc converter.
- 2) Isolation transformer required for central inverter application is utilized to merge the dc bus of three phases in order to reduce capacitor requirement and to mitigate the possibility of interarray leakage current.
- 3) A single PV array is used to feed the main bridge of converter through the dc-dc converter. This is done in

order to avoid unbalance current injection in to the grid during partial shading.

- 4) High resolution of the converter reduces the coupling inductor size to minimum. This results into higher reactive power handling capacity owing to lower voltage drop across the inductor.
- 5) The converter is inherently capable of limiting the fault current in the event of a dc-side short circuit.
- 6) Worst-case capacitor requirement for a two-stage inverter operation (with limited modulation index variation) is investigated. It is found that the capacitor requirement is substantially lower than the single-stage inverter that operates in a wide range of modulation index (0.5 to 1.0).

This article is organized as follows. Section I identifies the design constraints for next-generation PV inverter with the goals of efficiency, reliability, and cost effectiveness. Section II explains the concept of LDN. Section III mainly deals with two-stage conversion and also addressed the limitations of the major topologies reviewed in Section I. Section IV explains the fault-blocking capability of the proposed inverter topology. Section V analyses the reactive power injection capability and its comparison with other topologies. Section VI contains simulation results. Section VII reports the experimental results using the laboratory prototype. Section VIII compares the proposed inverter topology with well-known converter topologies for solar PV application. Section IX concludes the work.

II. CONCEPT OF LDN-DERIVED TOPOLOGY

The concept of LDN is first time proposed in the literature to get the higher number of output voltage levels in a CHB multilevel inverter [48]. This concept is applicable for both symmetric and asymmetric converter topologies. LDN helps to reduce the power rating of the isolated auxiliary sources. It is observed that with the existing H-bridge if a half-bridge is added, nearly double the number of output voltage levels can be achieved. Full-bridge is fed by dc source and half-bridge is fed by capacitor that maintains half the voltage of dc source of the corresponding full-bridge. Fig. 1 depicts the single-phase module of LDN, which consists of cascaded connection of one full-bridge and half-bridge. Floating capacitors of half bridges are self-balanced, and they do not require any closed-loop control. Symmetric CHB gives $2n+1$ output voltage levels but with the help of LDN, $4n+1$ levels can be achieved. Here, n indicates the number of H-bridges per phase. Hence, five levels can be achieved with the help of one module. These half bridges absorb power in one-half cycle and deliver the same amount of power in the next half cycle in steady state. Finally, the half-bridge's dc bus voltage ideally stays constant at the end of one cycle, as shown in Fig. 1(a). Fourier analysis of LDN voltage depicts that it will contain only even harmonics and dc component. Moreover, if the product of LDN voltage and current is integrated over a cycle, it will be zero (assuming that the load current consists

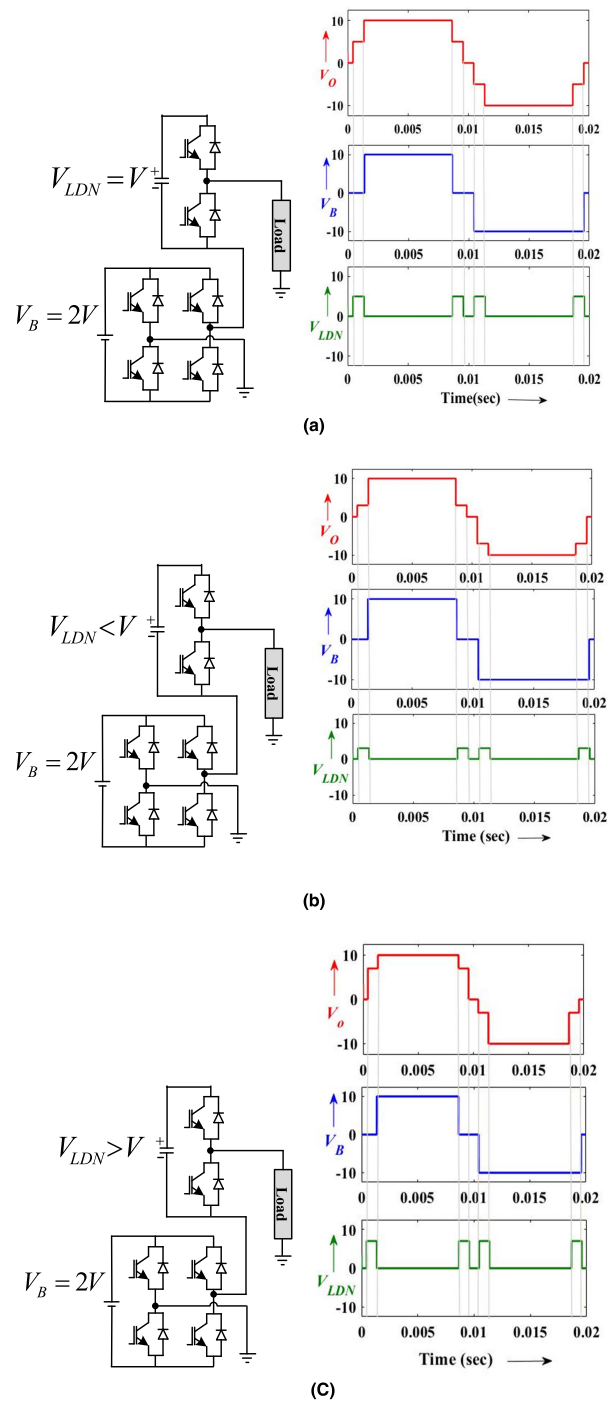


FIGURE 1. LDN circuit and its operation. (a) Steady-state operation (when $V_{LDN} = V_B$) and transient operation. (b) When ($V_{LDN} < V_B$). (c) When ($V_{LDN} > V_B$).

of fundamental component and odd harmonics). Thus, it will not consume any power at steady state.

In transient condition, when LDN voltage is less than the desired voltage (i.e., $V_{LDN} < 0.5 V_B$), the voltage waveforms for bridge, LDN, and module are shown in Fig. 1(b). The five-level output waveform will contain negative dc components and even harmonics. Due to the negative dc component,

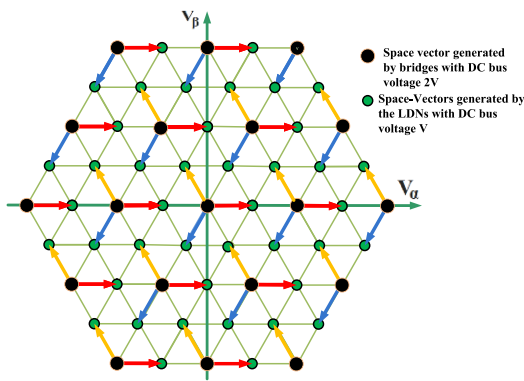


FIGURE 2. Space vector plane for three-phase modules.

charging will be more than discharging and it will force to build up the LDN voltage.

Similarly, when LDN voltage is greater than the desired voltage (i.e., $V_{LDN} > 0.5V_B$), as shown in Fig. 1(c), LDN capacitor will be overcharged. The positive dc component of current will help to discharge the capacitor. Hence, LDN voltage will be maintained at the desired voltage ($V_{LDN} = 0.5V_B$) without any closed-loop mechanism irrespective of any operating condition. It is important to note that there may be an offset voltage in the capacitor voltages during start-up transient. However, during steady state, dc offset created by the LDN voltage is compensated by its corresponding full-bridge. As a result, there is no lower order harmonics and dc offset in the ac output voltage.

LDN will be bypassed to get even voltage levels (positive or negative) and LDN will be active to get odd voltage levels in output. LDN generates only positive voltage with respect to ground in the circuit shown in Fig. 1. The output voltage and current of LDN maintain half-wave symmetry.

The capacitor requirement of LDN depends on the output current magnitude and conduction time of the LDN. LDN waveforms (current through LDN and voltage across LDN) should be repetitive in every half cycle at steady state. The output voltage of LDN does not consume energy with fundamental and odd harmonic component of the load in the steady state.

In order to implement LDN operations in the space vector plane, asymmetrical hexagonal decomposition is modified to suit for this purpose. Space vector plane for the three-phase module (combination of bridge and LDN) is shown in Fig. 2. Black dots represent space vectors generated by the full bridges and green dots are the space vectors generated by half bridges (LDN) whose dc bus voltage is half of the main bridge voltage. One complete three-phase module can generate 61 space vectors without violating the LDN principle. Once a space vector is formed by a particular LDN, then the same LDN will be used to build the complimentary space vector, i.e., space vector with 180° phase shift to satisfy the self-balancing operation of LDN.

In the literature, two modules (one full bridge and LDN) are considered, which are known as main module (consisting

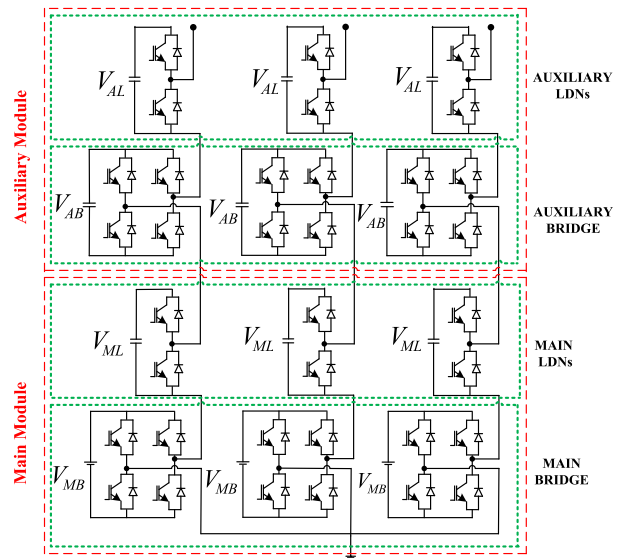


FIGURE 3. Topology with 1:5 ratio of asymmetry.

main bridge and main LDN) and auxiliary module (consisting auxiliary bridge and auxiliary LDN), respectively. Available literature reported that 1:7 is the optimal ratio of asymmetry between main bridge and auxiliary bridge when auxiliary bridges are fed by dc sources. In this work, main bridges of three phases are merged with the help of isolation transformer and fed by a common PV array for grid-connected solar PV applications. Power requirement by auxiliary sources is just 7% of total power rating but still bidirectional dc-dc converter is required for these three auxiliary bridges. These bidirectional converters required good insulation coordination. Hence, even auxiliary source power requirement is just 7% of total rated power, it involves significant amount of implementation cost.

The topology is improvised further to remove these isolated auxiliary sources and for that tradeoff is done in number of output voltage levels. It is found that 1:5 is the optimal ratio of asymmetry that can work without auxiliary dc sources throughout the range of modulation index. The topology with one dc source per phase is shown in Fig. 3. The optimal ratio is calculated in such a way that the entire power of input reference voltage or fundamental component should be generated entirely through main module. Then, the difference of reference voltage and voltage generated by main module will become the reference of auxiliary module. As main bridge is generating the fundamental, which is equivalent to the fundamental of reference, input of auxiliary module will not have any fundamental component. The fundamental component of input reference voltage should match with fundamental component of the output of main module in steady state. Auxiliary bridge will have zero fundamental and it will not be able to dissipate or absorb power. Capacitors of main LDN's and auxiliary LDN's are self-balanced. Lookup table-based feed forward controller is used so that all fundamental components will be generated by the main module. Low-gain PI controller

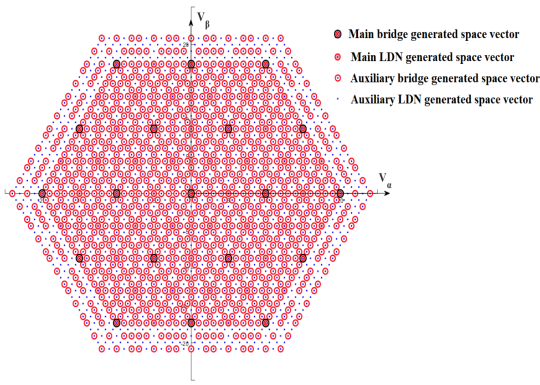


FIGURE 4. Space vector map for 1:5 ratio of asymmetry.

is used to balance the capacitor of auxiliary bridges during transient and nonlinear situation.

The effective space vector plane is depicted in Fig. 4. In this plane, LDN operation will be satisfied as well as auxiliary bridge capacitors will be balanced. In order to remove auxiliary voltage source, 1:5 is the optimal ratio of asymmetry and this space vector map explains the boundary for self-balancing of capacitors. Fig. 4 explains the number of ways space vectors are generated by different modules of the converter, i.e., main module (main bridge and main LDN) and auxiliary module (auxiliary bridge and auxiliary LDN). Fig. 4 depicts the outer periphery of space vector plane that only consists of space vectors generated by auxiliary bridge and auxiliary LDN. Hence, it is helpful to increase the modulation range.

III. TWO-STAGE INVERTER TOPOLOGY WITH COMMON DC BUS

A. OPERATION OF TWO-STAGE PV INVERTER

Grid-connected two-stage PV inverters fairly work at constant modulation index owing to nearly constant dc-link voltage of the inverter. Modulation indexes may vary in smaller range (may be 0.8 to 1) due to variation in grid voltage. The existing inverter with single stage is supposed to operate near 0.5 modulation index in rated condition. However, a two-stage converter operates near unity modulation index. That means, the inverter can be connected to a grid with double voltage compared to a single-stage inverter. Hence, addition of one more stage is helpful to double the inverter power handling capacity.

Device losses (switching loss and conduction loss) of an inverter are significantly dominated by dc-link voltage and device current. In a double-stage inverter, the ac-side voltage is doubled and the current remains the same as compared to a single-stage inverter with the same device and dc-link voltage. Assuming that the dc–dc converter is more efficient, less expensive than an inverter of the same power rating (owing to lower number of components of dc–dc converter compared to an inverter), a two-stage grid-connected PV inverter will result into a lower cost of implementation and higher efficiency

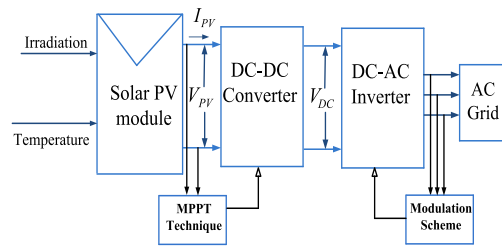


FIGURE 5. Basic diagram of a double-stage converter.

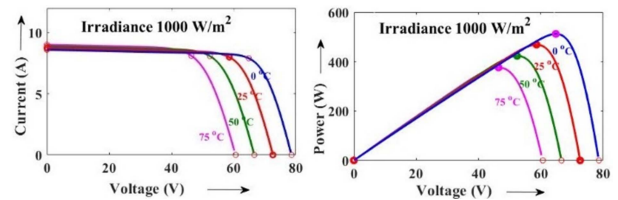


FIGURE 6. I - V and P - V characteristics at constant irradiance.

than a single-stage converter of the same power rating. This optional stage of dc–dc converter also decouples the MPPT control from the PV inverter grid control as shown in Fig. 5. Additionally, it can boost the PV system dc output voltage if required or provide galvanic isolation and perform MPPT control.

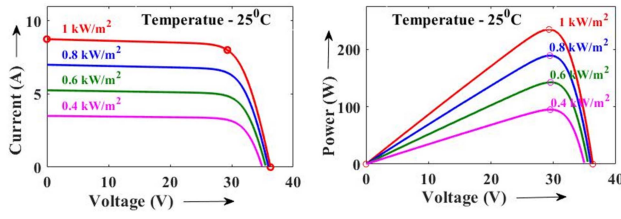
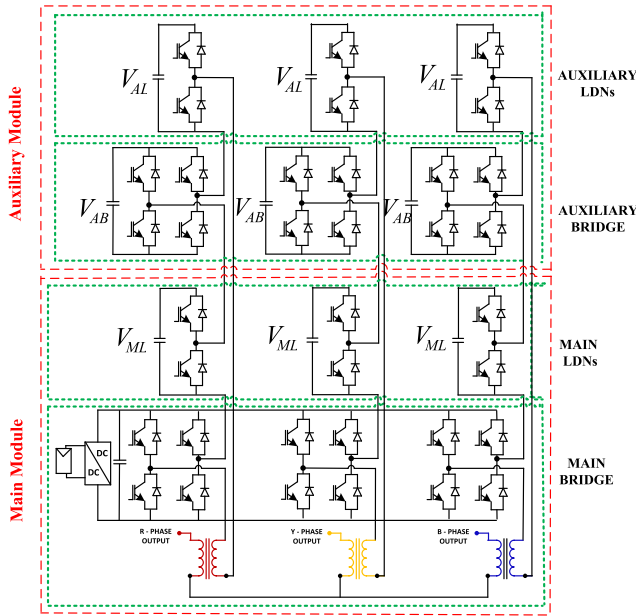
In double stage, a dc–dc converter will take care the MPPT of PV array and the output of dc–dc converter is connected to the capacitor that serves as a dc link of the inverter. An inverter will regulate the voltage of dc link and the MPPT of PV is independent of Inverter operation. A dc–dc converter (boost converter) can push power from the PV array to the dc link based on MPPT control irrespective of the dc-link voltage until the component voltage limit reaches. Grid-connected two-stage PV inverters help to maintain constant dc-link voltage of the inverter. It can be observed from Fig. 9 that two different controllers are used for dc–dc converter and inverter control. Inverter control will try to maintain the desired dc-link voltage and the dc–dc converter will try to extract the maximum power from PV array and push this power to the dc-link capacitor.

Hence, PV voltage variation does not affect the inverter operation. As the PV input changes, the reference I_d changes accordingly in order to maintain the constant dc-link voltage.

I - V and P - V characteristics of a PV module at constant irradiance (1000 w/m^2) and constant temperature (25°C) are shown in Figs. 6 and 7, respectively. Operating voltage of the PV array changes due to insolation and temperature, as shown in Figs. 6 and 7, respectively. However, two-stage operation of this converter topology ensures reasonably constant dc-link voltage of the main bridge.

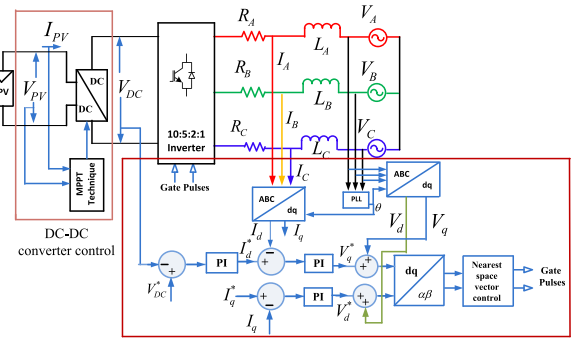
B. COMMON DC BUS WITH ISOLATION TRANSFORMER

The proposed topology aims to overcome the limitations of existing grid-connected PV inverter topologies. Removal of


FIGURE 7. *I-V* and *P-V* characteristics at constant temperature.

FIGURE 8. Two-stage three-phase single-sourced converter topology with isolation transformers.

isolation transformer reduces cost and improves system efficiency. However, for a PV central inverter, it is evident that multi-MW power cannot be evacuated without three-phase 11 kV grid, i.e., at least 11 kV grid is required, and the maximum PV array voltage cannot be more than 900 V due to insulation failure and potential-induced degradation. Hence, transformer isolation cannot be avoided. Modification of topology is done for grid-connected applications, as shown in Fig. 8. In the proposed topology, dc buses of three phases cannot be merged without electrical isolation, as shown in Fig. 8. Step-up transformers are used in order to provide isolation and avoid leakage current. Main bridge of the LDN-based topologies can be merged with the help of isolation transformer. In this work, a two-stage converter (extra dc–dc converter as marked in Fig. 8) is used to increase the power handling capacity. Common dc bus will help to avoid interarray leakage current and power imbalance due to partial shading.

In case of three different PV arrays, partial shading causes unbalanced current injection into the grid. In this situation, an active filter will be required to take care of unbalanced current. When dc buses of three phases are merged, there is a possibility of trading off with net energy yield of the PV array


FIGURE 9. Modulation scheme for grid-connected solar PV application.

in partial shading condition. However, a single dc source will feed the three phases without any unbalanced current. Merging three dc buses also helps to optimize the capacitor size, i.e., number of cables. It reduces dc bus voltage ripple as compared to one when three phases are fed by individual sources, thereby reducing the capacitance requirement of main dc bus. A primary-side open-winding three-phase transformer is used to merge dc buses of three phases. To protect open-winding transformer core from saturation, no dc component should be present in the phase voltage.

A modulation scheme for the grid-connected solar PV application is shown in Fig. 9. Active component of the inverter output current will be decided on the basis of dc-link capacitor voltage. Reference current will be generated by a PI controller, which is actually going to maintain the reference voltage of capacitor. The difference of actual capacitor voltage and reference voltage is sent to the PI controller. The output of PI controller is the active component of the grid-connected inverter. As current reference will change, quadrature component of grid voltage will change. The quadrature sinusoidal component will get added up with grid voltage to generate inverter reference voltage. The grid voltage is constant and quadrature voltage corresponding to current will change, which will finally change the inverter voltage magnitude and angle.

1) RELATION BETWEEN DC-LINK VOLTAGE AND GRID VOLTAGE

In the proposed work, grid voltage is adjusted by using a transformer to get maximum inverter utilization. In central inverter application, output voltage is usually raised by using power transformer as MW scale power cannot be injected to a low-voltage distribution bus. This same transformer can be used to customize the grid voltage to have better inverter utilization. The dc bus voltage (V_{dc}) of the inverter is kept at the highest possible voltage that will have negligible effect on potential-induced degradation or safety issue.

$$\left| \vec{V}_{\alpha\beta} \right|_{\max} = 1.81 V_{MB} \quad (1)$$

$$V_g = \left(V_{MB} * 1.81 * \frac{\sqrt{2}}{\sqrt{3}} \right). \quad (2)$$

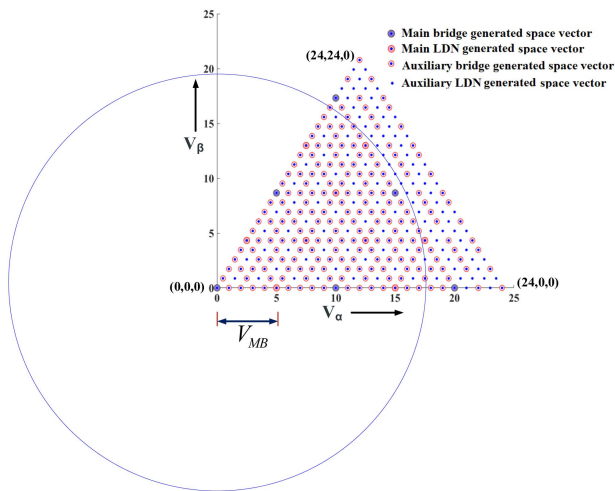


FIGURE 10. Maximum magnitude of rotating vector $\vec{V}_{\alpha\beta}$ for 1:5 ratio of asymmetry.

The maximum magnitude of ac output voltage possible at unity modulation index for a particular dc bus voltage can be calculated from Fig. 10. The peak magnitude of rotating reference vector ($|\vec{V}_{\alpha\beta}|$) possible for 1:5 ratio of asymmetry is given in (1). In the absence of any auxiliary module, the magnitude of rotating reference vector would be restricted to $1.732 V_{MB}$ without entering into overmodulation. Considering this, the relationship between V_{MB} (dc bus voltage of main bridge) and grid voltage (line) V_g is given in (2). In this article, main bridge voltage is taken as 160 V; hence, corresponding maximum grid voltage at unity modulation index will be 237 V to generate 43 levels in line-to-line voltage. Grid voltage V_g can be as high as voltage given in (2).

C. POWER QUALITY AND SWITCHING LOSS OPTIMIZATION

Two-level and three-level inverters are cost-effective solutions. These inverters can give high power quality with high operating frequency (that means at the cost of high switching losses). The proposed topology offers negligible switching and filter losses and at the same time high power quality with some tradeoff in conduction losses. However, conduction losses in a given topology are not proportional to the number of switches and they can be limited. Conduction loss of this inverter topology can be 50% higher than the two-level inverter. Two-level inverter devices should be capable of operating at higher switching frequency to obtain equivalent power quality. High-frequency switching devices required in the two-level inverter invite higher conduction loss and corresponding cooling requirement.

In the proposed topology, most of the switching is at fundamental frequency as switches of main bridge operate at near fundamental frequency. Moreover, high-frequency switching operation is pushed to the low-voltage cells.

Switching losses and filter size are not compromised in order to maintain power quality in the proposed work. On the other hand, there is some tradeoff in conduction losses.

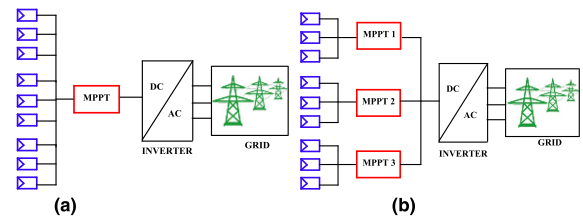


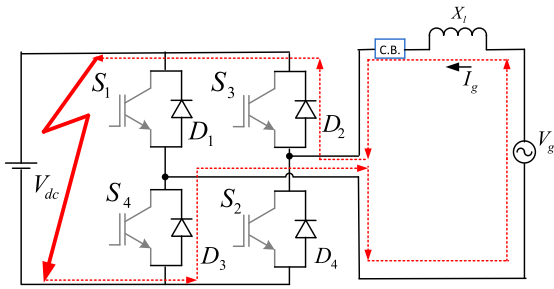
FIGURE 11. PV inverter with maximum power point trackers. (a) Single MPPT. (b) Multiple MPPT.

D. UTILIZATION OF MULTIPLE MPP TRACKERS FOR TWO STAGE

Performance of a central inverter connected to a large PV array (spread over large area) normally gets affected due to moving cloud or partial shading. For a single MPPT tracker, global maximum power point can be detected in case of partial shading. This global maximum power point does not ensure that individual subarray of module will work at its maximum power point. However, if module is divided into multiple subarrays with its dedicated dc–dc converter, then each of the subarray will be capable of operating at their individual maximum power point. Multiple MPPT trackers are advantageous in terms of dividing the PV array into multiple small parts and subsequently higher energy yield is possible. Multiple MPPTs provide more design flexibility and flexibility in types of modules. Moreover, the losses due to shading and mismatch remain less in case of multiple maximum power point trackers as compare to single MPPT. It is evident that the two-stage converter will be required as a single-stage converter cannot offer multiple MPPT tracking. Hence, a two-stage converter with multiple MPP trackers [50] is considered in this work. A solar PV inverter with single MPPT and multiple MPPTs is shown in Fig. 11. All the dc–dc converters responsible for their individual MPPT tracking are connected to a common dc link at their output end. The voltage of this common dc link is independently controlled by the power flow controller of the inverter. Hence, multiple MPPTs incorporated by different dc–dc converters do not interfere with each other. For MW scale power, the PV array is expected to spread over large area, which is prone to be affected by partial shading due to moving cloud. Single MPPT is detrimental for maximum power yield as well as dc–dc converter (for MPPT tracking) of such large power rating may not be economical and reliable.

IV. FAULT BLOCKING CAPABILITY

The proposed single-sourced double LDN-based topology provides dc fault blocking capability. Fault response of the proposed topology is analyzed in this section. This is also compared with well-established topologies such as two-level or three-level converter, which is used in PV systems. It can be observed in Fig. 12 that dc fault can either be because of dc-link capacitor failure or short circuit in PV array itself. Under this fault, two-level or three-level converters acts like a short-circuited rectifier, i.e., a rectifier with its dc bus short circuited. In that situation, even if pulses from IGBTs are

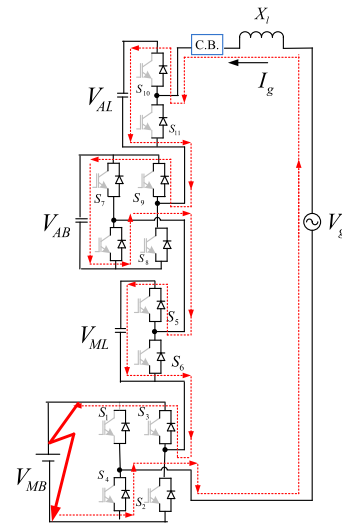

FIGURE 12. Bridge inverter with dc fault.

withdrawn, the reverse diodes will keep on carrying current irrespective of the polarity of the ac voltage. High current will flow through switches, which can overheat the devices and may cause complete failure of devices.

This situation can be avoided with the help of dc breaker or semiconductor-grade fuse. Both have its implications on cost. A dc breaker is an expensive solution, and a semiconductor-grade fuse is likewise not a cheap one. Moreover, those fuses are to be replaced after failure that also deals with down time (time takes to replace semiconductor fuses). Associated cost for that downtime involves loss of power injection into the grid. Moreover, depending on the position of the fault, dc breaker will be able to block the fault current. In such conditions, another option for protecting the converter is to deploy an ac circuit breaker on the ac side of the converter, as shown in Fig. 12. Although an ac circuit breaker is going to take much larger time as high as 20 ms, the fault current can be as high as several times the rated current. Assuming per unit impedance of 0.05 for the filter, the worst-case current from the ac fault transient can be twice of V/X_L ratio. That amount of high current will not be possible to extinguish or quench before the first zero crossing or 20 ms. Hence, fault handling in a standard converter topology is definitely a matter of challenge, which brings a substantial restriction on converter operation. While considering the proposed topology as shown in Fig. 13, when the current exceeds a particular value, pulses are withdrawn, which is very standard feature of a gate driver. Withdrawal of pulses can be initiated independently (through V_{CESAT} protection) and no central controller is needed for that purpose.

After first line of action, V_{ML} (main LDN capacitor voltage), V_{AB} (auxiliary bridge capacitor voltage), and V_{AL} (auxiliary LDN capacitor voltage) will start working like a rectifier while V_{MB} will get short circuited. The equivalent circuit after fault is shown in Fig. 14, in which the main bridge is shown as fault impedance and C_{ML} , C_{MB} , and C_{AL} are capacitances of main LDN, auxiliary bridge, and auxiliary LDN capacitors, respectively.

It can be observed from Fig. 14(a) and (b) that there are three rectifiers in series that will be capable of blocking the fault current in either direction. Moreover, this converter is proposed for the three-phase system. Hence, if there is positive half cycle for one of the phases, then there will be a


FIGURE 13. Proposed inverter topology with dc fault.

negative cycle for at least one of the phase. In such a situation, line-to-line voltage is going to be blocked by V_{AB} in both the phases and V_{ML} , V_{AL} in one of the phases, which is given in (3).

Due to these voltages, current gets restricted while the voltage across capacitor will rise. It is evident that fault current will not be rising to the objectionable value to damage the device and much before that V_{CESAT} protection comes into picture. Then capacitor voltage will be restricted from rising to an exorbitant value. In worst case, the total capacitor voltage will be same as given in (3). This worst case will occur in the absence of ac circuit breaker. Due to ac circuit breaker, current (I_g) will not rise to excessive value to raise the capacitor voltage very fast. This current will also extinguish at first zero crossing of line-to-line voltage (\widehat{V}_{LL}) or after 20 ms due to circuit breaker operation. Expressions for peak current, voltage rise in main LDN, auxiliary bridge, and auxiliary LDN capacitor are given in (4), (5), and (6) and these vary with time. After one cycle, circuit breaker will operate, and in one cycle, variation in capacitor voltage will be small.

$$\widehat{V}_{LL} \approx 2V_{AB} + V_{ML} + V_{AL} \quad (3)$$

$$V_{ML}(t) = V_{ML(0)} + \frac{1}{C_{ML}} \int I_g(t) dt \quad (4)$$

$$V_{AB}(t) = V_{AB(0)} + \frac{1}{C_{AB}} \int |I_g(t)| dt \quad (5)$$

$$V_{AL}(t) = V_{AL(0)} + \frac{1}{C_{AL}} \int I_g(t) dt. \quad (6)$$

V. ACTIVE AND REACTIVE POWER INJECTION

A two-stage converter provides more flexibility to inject active and reactive power as dc bus voltage remains almost constant, whereas in a single stage, dc bus voltage varies as per insolation. In the two-level inverter, as shown in Fig. 15(a), due to high filter inductor, the voltage drop across inductor

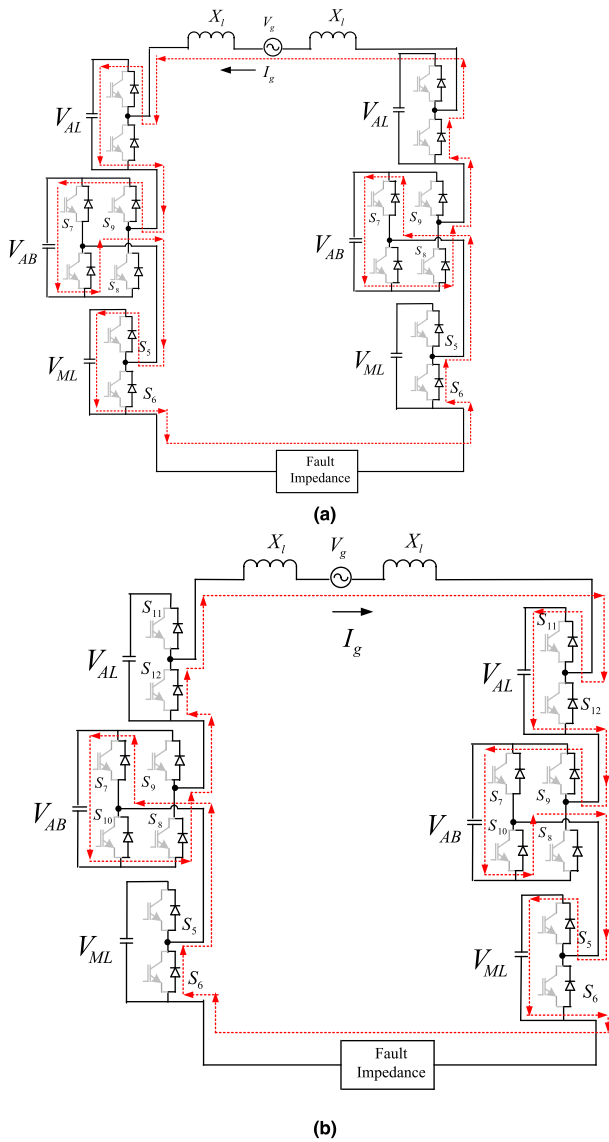


FIGURE 14. Fault current blocked by capacitor voltage in (a) first half cycle and (b) second half cycle.

will be high. This acts as a major constraint for injecting reactive power into the grid. The impact of coupling inductor on capability curve gives a clear idea about power injection limit.

The proposed topology, as shown in Fig. 15(b), with a two-stage configuration requires substantially smaller coupling inductor. The fundamental component of the voltage drop across the inductor will be small. So other than reducing the filter size and losses in filter, this topology is also expected to facilitate higher reactive power injection for the same voltage drop across inductor. Small voltage difference between the inverter voltage and grid voltage can cause high reactive power injection; hence, smaller drop in coupling inductor for the same grid current.

Capability curve for a two-level inverter and for the proposed multilevel inverter having equivalent power rating, grid

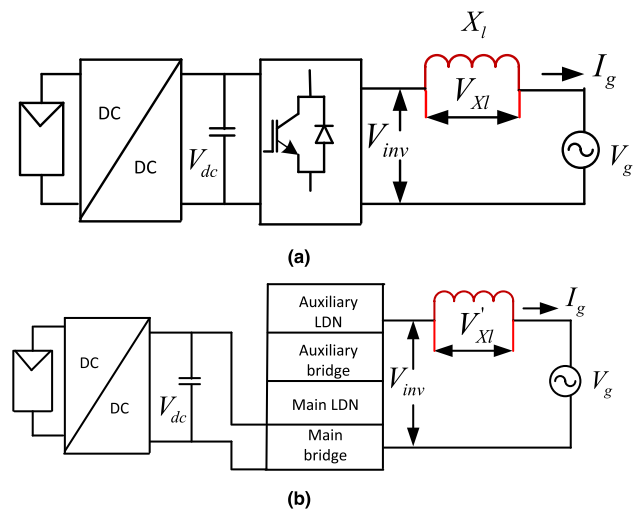


FIGURE 15. Power flow in (a) two-level inverter and (b) proposed inverter topology with $V_{XL} \gg V'_{XL}$.

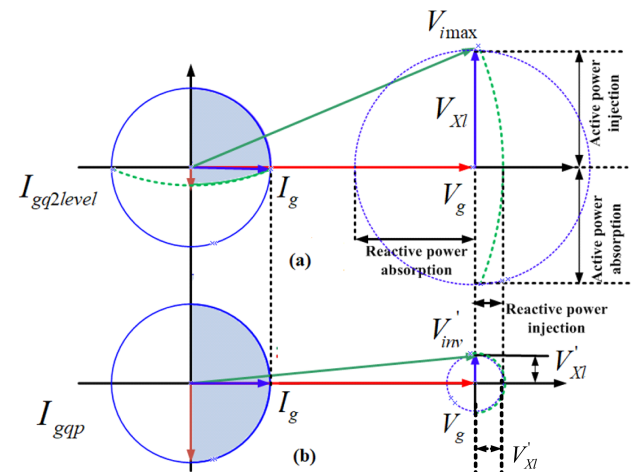


FIGURE 16. Reactive power injection limit. (a) Two-level inverter. (b) Proposed inverter topology.

voltage, and dc bus voltage is compared in Fig. 16. This figure consists of two separate phasor diagrams. Fig. 16(a) is for two-level inverter, which is having a higher size of filter, and Fig. 16(b) is for the proposed converter topology with lower or negligible filter size. In the two-level inverter, it is considered that the maximum possible output voltage is V_{imax} (maximum inverter output voltage for a two-level inverter) for maximum dc bus voltage and maximum modulation index. In this situation, grid voltage can be adjusted in such a way that it will be able to pump its rated current. The rated current I_g for a two-level inverter is given in (7), where V_{xl} is the voltage drop on the coupling inductor and X_L is the coupling inductor impedance. The maximum reactive power can flow when inverter output voltage at its maximum and power angle between V_{imax} and V_g (grid voltage) is zero.

When the angle between V_{imax} and V_g is zero, then the magnitude of phasor difference between them (i.e., V_{xl}) becomes

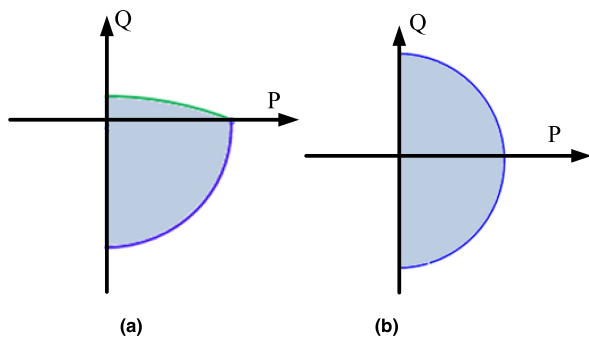


FIGURE 17. Capability curve for (a) two-level inverter and (b) proposed inverter topology.

minimum, as shown in Fig. 16. This restricts the reactive power injection capability of the converter. Hence, the reactive power injection limit in such a condition is not restricted by device current.

In the proposed converter topology, the filter size is small for the same current I_g . It can be observed that V'_{XL} , i.e., the voltage drop on the coupling inductor, for the proposed inverter will be much smaller due to the low value of X'_L (coupling inductor impedance for the proposed topology), as observed in Fig. 16. This is also an indication that V'_{inv} (inverter output voltage for the proposed inverter) required to inject rated power is smaller than V_{imax} , as shown in Fig. 16(b), which is the maximum possible inverter voltage. Fig. 16 compares the active and reactive power limits of a conventional two-level inverter and the proposed converter for same output voltage and current rating of both the inverters connected to the same grid voltage. Fig. 16(a) shows the capability curve for a two-level inverter, and (b) shows the capability curve for the proposed inverter. The maximum possible output voltage V_{imax} and rated grid current I_g are identical for both the inverters, as shown in Fig. 16. It is observed that this same inductor voltage drop V'_{XL} results in higher reactive power in the presented topology due to the lower requirement (value) of filter inductor. The same magnitude of I_g in quadrature is possible with zero power angle between the inverter output voltage and grid voltage and the proposed inverter is going to operate at its maximum voltage in such condition as given in (8). This is the condition to inject pure reactive power with an assumption of negligible coupling resistance. So, entire capability curve can be represented like a circle, as shown in Fig. 17(b). The quadrature component of grid current and reactive power for the two-level inverter and proposed inverter topology is given in (9)–(13), where I_{gq} is the quadrature component of grid current, $I_{gq2level}$ is for the two-level inverter, and I_{gqp} is for the proposed inverter topology. Q_{2level} exhibits the reactive power injection limit of two-level inverter, whereas Q_p is for the proposed inverter topology. In the converter topology presented, reactive power is going to limit by a current carrying capability of inverter. For all practical purpose, current carrying capability is independent of phase angle in the proposed converter.

Due to low impedance of the filter inductor, current injection capability is not restricted by voltage, which happens in two-level inverter, as shown in Fig. 17(a). Here, it is clearly observable that reactive current injection capability has increased substantially. Moreover, this comparison is done with an assumption that the output voltage for a two-level inverter and the presented converter topology will be the same for same dc bus voltage. However, the presented converter topology is expected to yield higher ac output voltage compared to a two-level inverter (with same dc bus voltage) owing to its modulation and the voltage levels offered by the auxiliary cells with floating capacitors. Hence, for the same dc bus voltage, grid voltage can be higher: this will help to have effective device utilization.

$$I_g = \frac{V_{XL}}{X_l} \quad (7)$$

$$|V'_{XL}| = |V_{imax}\angle 0^\circ - V_g\angle 0^\circ| \quad (8)$$

$$I_{gq} = \frac{(V_{inv} - V_g)}{X_l} \quad (9)$$

$$I_{gq2level} = \frac{(V_{imax} - V_g)}{X_l} \quad (10)$$

$$Q_{2level} = V_g * I_{gq2level} \quad (11)$$

$$I_{gqp} = \frac{(V'_i - V_g)}{X'_l}, \text{ where } X_l \gg X'_l \quad (12)$$

$$Q_p = V_g * I_{gqp}. \quad (13)$$

VI. SIMULATION RESULTS

Simulation for a grid-connected PV system using the proposed converter is performed in the MATLAB/Simulink. To test the validity of the topology's fault-blocking capacity, a dc fault is created in simulation. The converter configuration used for simulation is shown in Fig. 8, and the important parameters for simulation are stated in Table 1. All the dc buses of main bridge are merged and the voltage of main dc link is maintained at 800 V with the help of dc–dc converter. A transformer is used to merge the dc buses of all the three phases and to provide galvanic isolation. The three-phase line-to-line voltage at the primary side of transformer is considered as 1.028 kV and at secondary side is as 11 kV. The following sections present the performance of an inverter in both normal and fault conditions.

A. NORMAL INVERTER OPERATION

The dc-link voltage of the main bridge is shown in Fig. 18 and it is maintained at 800 V with the help of a dc–dc converter. The PV array MPP voltage at the standard test condition is restricted to 800 V due to the insulation limit of the PV modules. The voltage across main LDN, auxiliary bridge, and auxiliary LDN capacitors is shown in Fig. 19(a), (b), and (c) respectively. Main LDN and auxiliary LDN do not require any closed-loop controller to balance the capacitor voltage, whereas auxiliary bridge needs a low-gain PI controller. The

TABLE 1. Simulation Parameters

Parameters	Values
Voltage of main bridge	800 V
Voltage of main LDN	400 V
Voltage of Auxiliary bridge	16 V
Voltage of Auxiliary LDN	80 V
Maximum line-to-line voltage primary (rms)	1.028 kV
Load Current primary (rms)	57.27 A
Maximum line-to-line voltage secondary (rms)	11 kV
Load Current secondary (rms)	5.35 A
Nominal energy of main LDN capacitor	5 J/kVA
Nominal energy of Auxiliary bridge capacitor	2.1 J/kVA
Nominal energy of Auxiliary LDN capacitor	0.6756 J/kVA

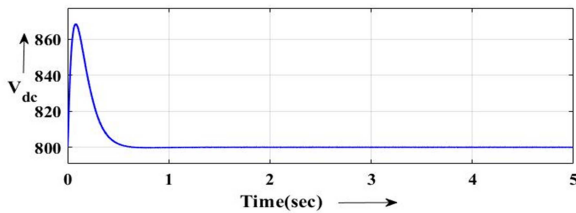


FIGURE 18. DC-link voltage across main bridge.

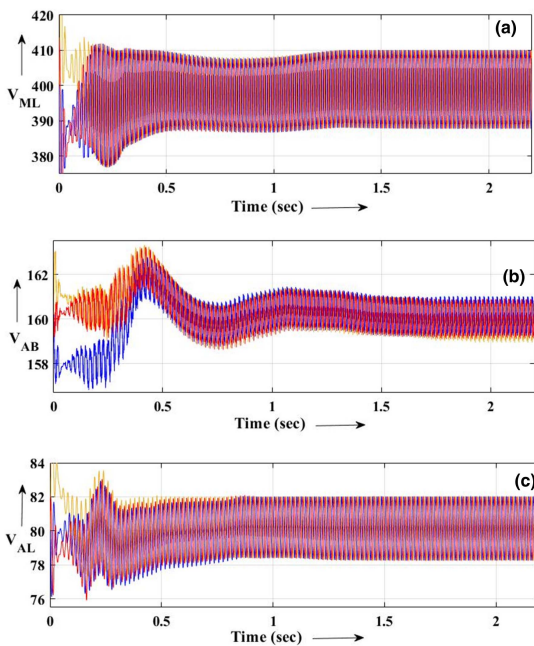


FIGURE 19. Voltage across (a) main LDN capacitors, (b) auxiliary bridge capacitors, and (c) auxiliary LDN capacitors.

high-resolution line-to-line voltage output for unity power factor load is given in Fig. 20. The line-to-line voltage and corresponding phase voltage are given in Fig. 21. It is appearing that phase voltage contains many harmonics, whereas line voltage is near sinusoidal. Phase voltage consist of only triplen harmonics (generated by space vector modulation), which will be canceled out in line-to-line voltage. This helps to get near sinusoidal waveform. There is no impact of dc offset in steady state, as shown in Fig. 21. Phase voltages and corresponding cell voltages are shown in Fig. 22. Over the period of one

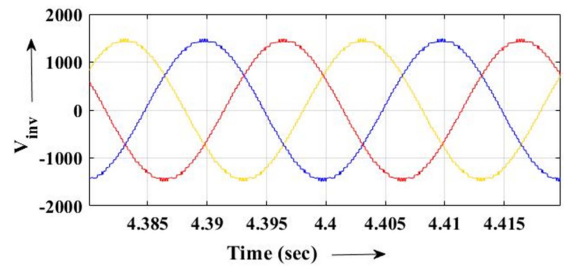


FIGURE 20. Output line-to-line voltage.

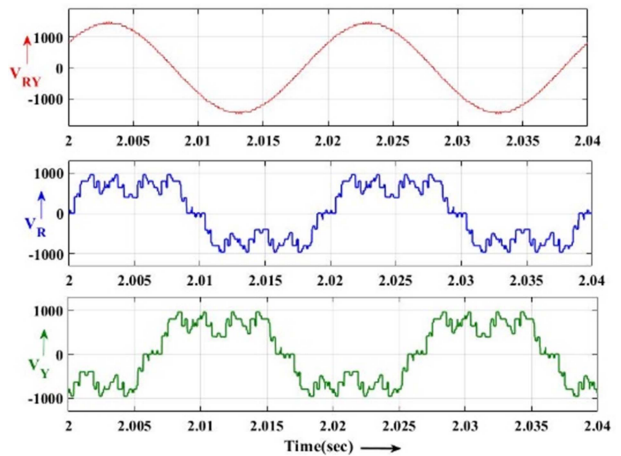


FIGURE 21. Inverter output line voltage and corresponding phase voltages.

cycle, the integration of phase voltage helps to determine its dc component. In present case, the integration of phase voltage gives zero value, which indicates the absence of dc component in phase voltage.

Output voltage THD is shown in Fig. 23, and it can be observed from this plot that all the harmonic components are less than 0.5% and the THD of the voltage waveform is below 2%. In the presented converter topology, output current THD is less than 0.8% and it can be observed from Fig. 24 that it will not contain any high-frequency component, whereas for same parameters and power rating and to get same power quality in two-level inverter, switching frequency has to be around 20 kHz, which causes high switching losses and reduces the reliability. The fast Fourier transform (FFT) analysis of converter output current is given Fig. 25 as 20 kHz switching frequency is not feasible for high power range (several kilowatts to megawatts).

Hence, to maintain the power quality, filter size has to be high enough. It will cause high rms voltage across filter as well as high loss per kilogram. For a pulsewidth modulation operation in two-level inverter, the grid has to be coupled to the inverter through a high-frequency inductor. A CRGO core-based inductor is not effective against a high-frequency voltage component. On the other side, for the presented inverter owing to its near sinusoidal output voltage, a normal CRGO core can be used. As a result, the leakage inductance of the transformer (made of CRGO core) is sufficient to use as a coupling inductor. Moreover, the rms voltage appearing across

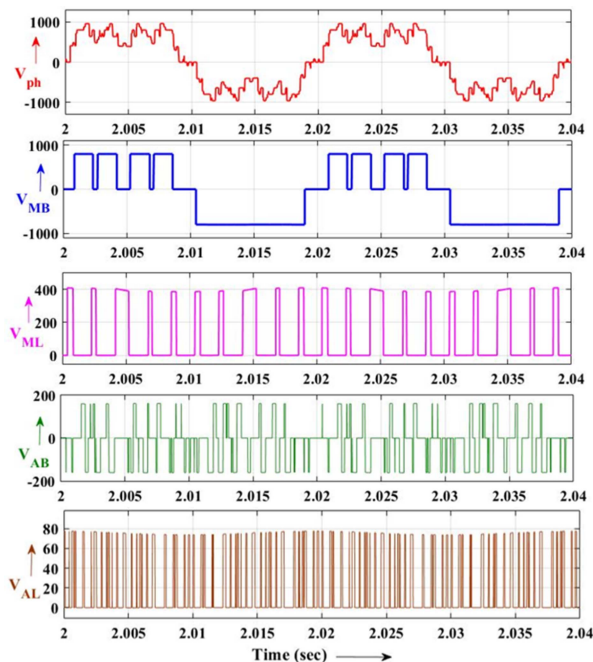


FIGURE 22. Phase voltage and corresponding cell voltages.

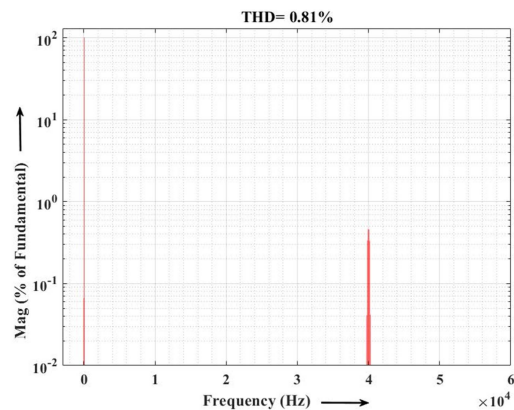


FIGURE 25. FFT analysis of output current of the two-level inverter.

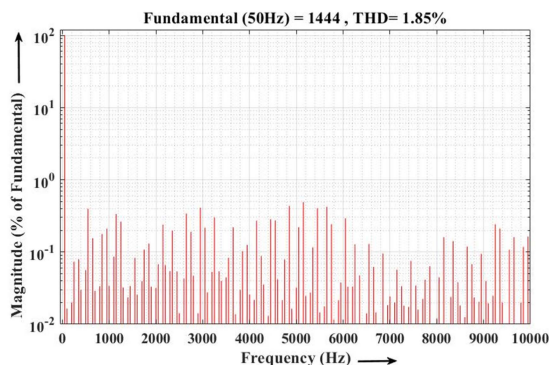


FIGURE 23. FFT analysis of the presented inverter output voltage.

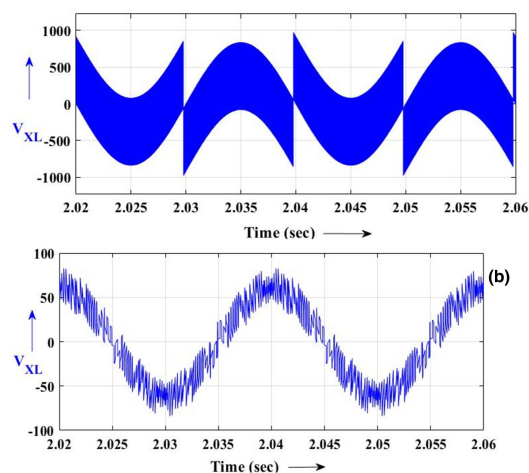


FIGURE 26. Voltage drop across coupling inductor in (a) two-level inverter and (b) presented converter topology.

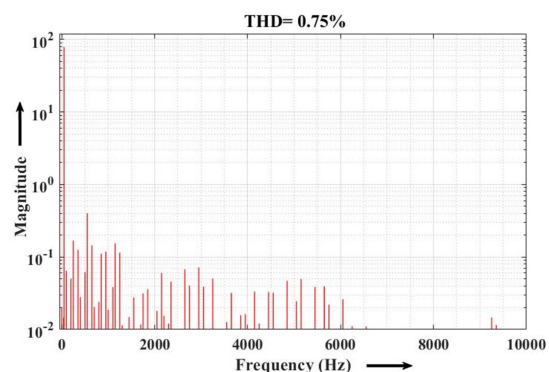


FIGURE 24. FFT analysis of output current of the presented inverter topology.

the coupling inductor is lower in the presented converter compared to a two-level inverter. It is important to note that the most dominating loss component in the inductor is the eddy current loss, which increases with square of the proportion to the rms voltage appearing across the inductor. Fig. 26 depicts the waveform of the voltage drop across the coupling inductor. Fig. 26 clearly shows that the rms voltage across the inductor is roughly 376 V in a two-level inverter, but it is only 44 V in the presented inverter topology.

For a two-stage operation, the inverter works at nearly 0.8 to 1 modulation index. Hence, the number of switching per fundamental cycle is plotted for 0.8 to 1 modulation index range, as shown in Fig. 27. In this range, switches of main bridge operate near the fundamental frequency. The maximum switching frequency for main LDN switches is around 500 Hz. Similarly, auxiliary bridge and auxiliary LDN switches operate at the switching frequency of 1.15 kHz and 2.6 kHz, respectively. However, auxiliary module switches are operating at a higher switching frequency, but they are operating at very low dc bus voltage.

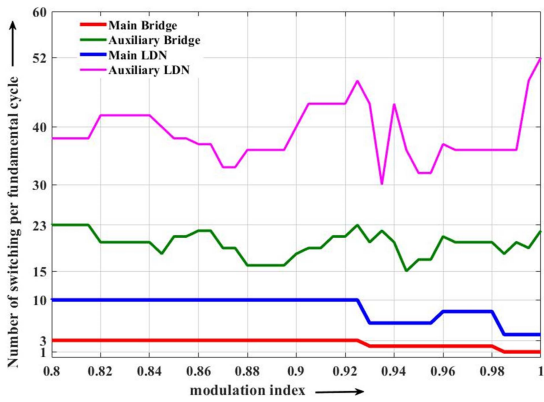


FIGURE 27. Number of switching w.r.t. modulation index for two-stage inverter.

Grid voltage and current waveforms for different power factors are shown in Fig. 28(a)–(c). The transmission system operators (TSOs) usually demand 33% of reactive power injection capacity with respect to active power limit of the inverter, i.e., power factor of 0.95. This is done to ensure that reactive power demand of the load is fulfilled by the inverter. Fig. 28(b) and (c) shows the current with power factor 0.95 lagging and leading, respectively. Three-phase grid currents are illustrated in Fig. 29 and it can be observed that it is maintaining good power quality.

The waveforms for active and reactive power are shown in Fig. 30. Fig. 30(a) represents pure active power injection into the grid and, in this situation, grid voltage and current will be in the same phase (zero phase difference).

Fig. 30(b) represents active and reactive power injection and, in this case, grid current will lag the grid voltage by some phase angle. Active power injection and reactive power absorption are illustrated in Fig. 30(c). Negative reactive power indicates that grid current leads the grid voltage by some phase angle.

B. INVERTER OPERATION DURING DC FAULT

Simulation results of the proposed topology are compared with the two-level inverter and presented in this section. Grid voltage and current at the secondary side of transformer for unity power factor operation are shown in Fig. 28(d). The dc bus voltage and current after fault are shown in Fig. 31(a) and (b), respectively. It can be observed from Fig. 31(b) that the grid current increased from 245 to 2000 A after fault. However, the inverter can be protected with an ac circuit breaker. However, this high current cannot be quenched before first zero crossing. This high current is sufficient to destroy the current carrying components of the system. This may demand an additional dc breaker, as explained in Section V. Fig. 32(a) and (b) shows the dc-link voltage and grid current after fault for the proposed converter. In Fig. 32(b), first red-phase current will come to zero and total current of the system will be distributed in rest of the two phases. The grid current after fault increased from 81 to 380 A and that amount

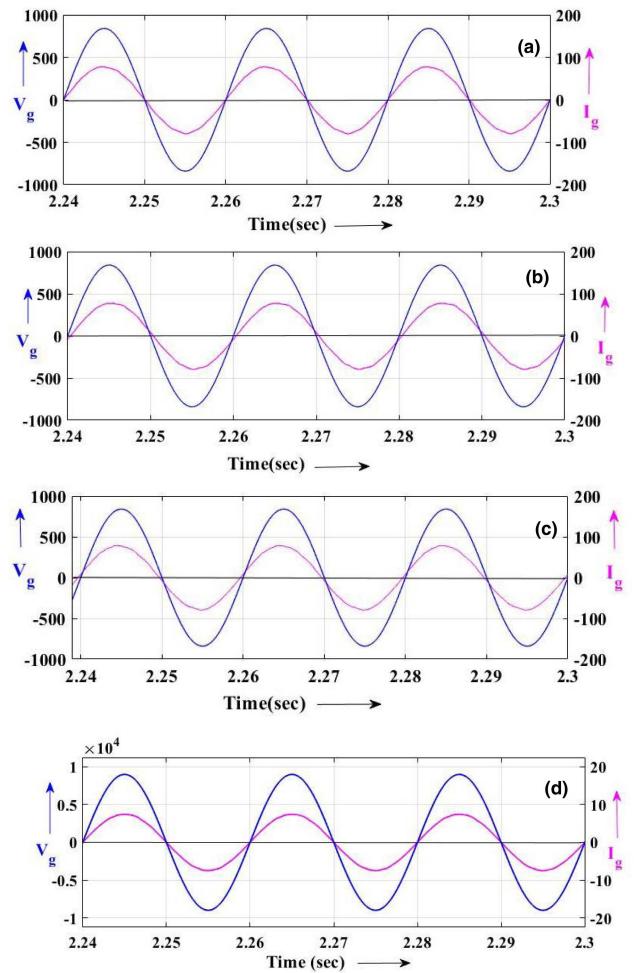


FIGURE 28. Grid voltage and current at (a) unity power factor, (b) lagging power factor (reactive power injection), (c) leading power factor (reactive power absorption), and (d) secondary side of transformer at unit power factor.

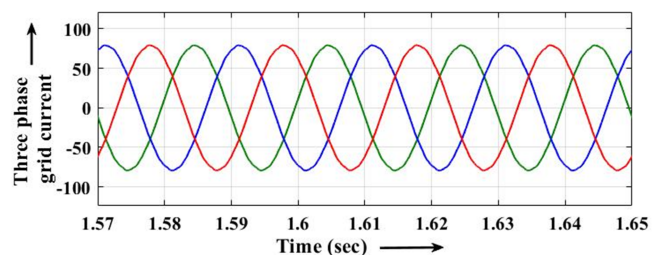


FIGURE 29. Three-phase grid current.

of current can be easily handled by the reverse-diodes of the switches for 20 ms. Active devices will be turned OFF immediately after fault as the gate-pulse for the active switches will be withdrawn just after fault (due to short-circuit protection mechanism incorporated in most of the gate drivers).

In proposed topology, floating capacitor voltages will help to block the grid current after dc fault, as discussed in Section V. The variation of voltage across main LDN capacitor,

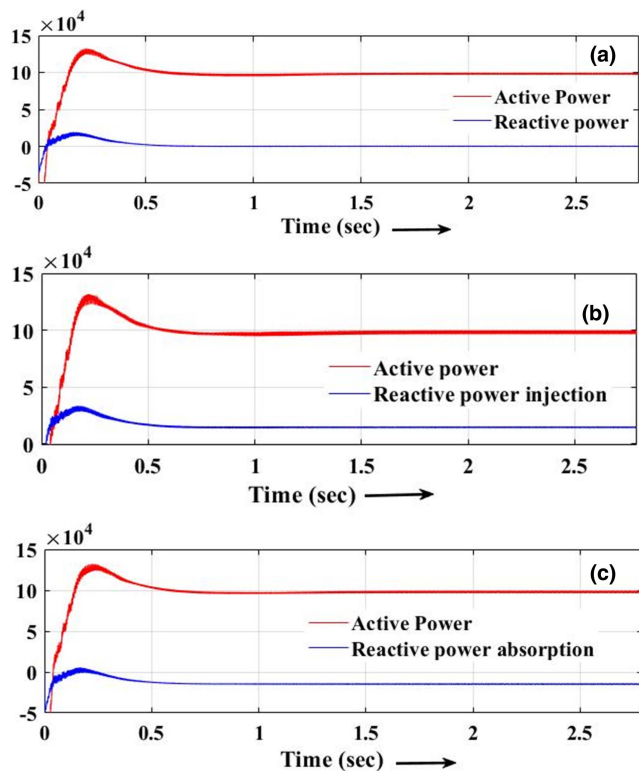


FIGURE 30. Power flow control. (a) Active power injection and zero reactive power. (b) Active and reactive power injection. (c) Active power injection and reactive power absorption.

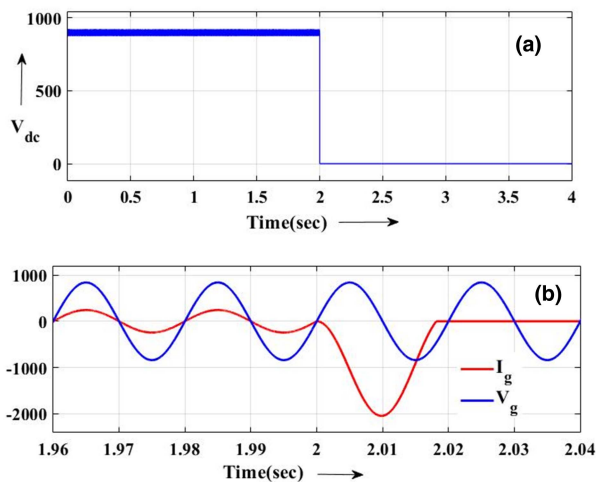


FIGURE 31. Two-level inverter after dc fault. (a) DC bus voltage. (b) Fault current.

auxiliary bridge capacitor, and auxiliary LDN capacitor for two phases is shown in Fig. 33(a), (b), and (c), respectively. It is relevant to observe that the capacitor voltages are raised after fault (within tolerable limit). This has restricted the magnitude of fault current. Note that the capacitors will be blocking the fault current, as illustrated in Fig. 13. For the presented topology, inverter behavior after dc fault is shown in Fig. 34. Fig. 34(a) and (b) illustrates inverter output voltage and grid current before fault and after fault.

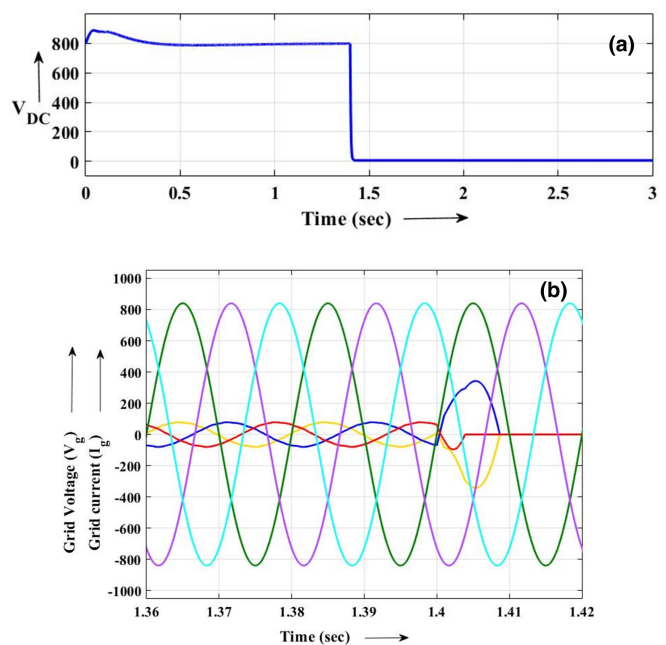


FIGURE 32. Proposed multilevel inverter after dc fault. (a) DC bus voltage. (b) Fault current.

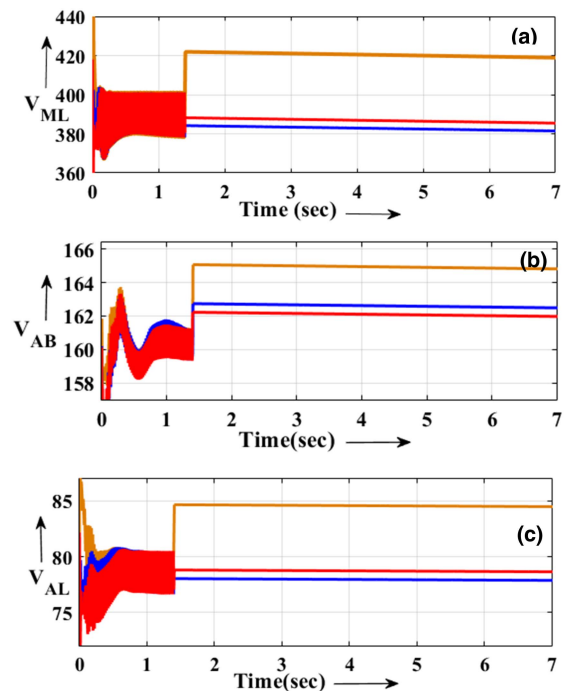


FIGURE 33. Capacitor voltage after fault. (a) Main LDN. (b) Auxiliary bridge. (c) Auxiliary LDN.

For a two-stage operation, inverter works at nearly 0.8 to 1 modulation index. Usually, the capacitor requirement of the floating cells is higher at lower modulation index. Capacitor requirement for the floating cells can be reduced. The worst-case capacitor requirement of main LDN, auxiliary bridge, and auxiliary LDN for complete modulation index range is shown in Figs. 35–37. Capacitor requirement is plotted against

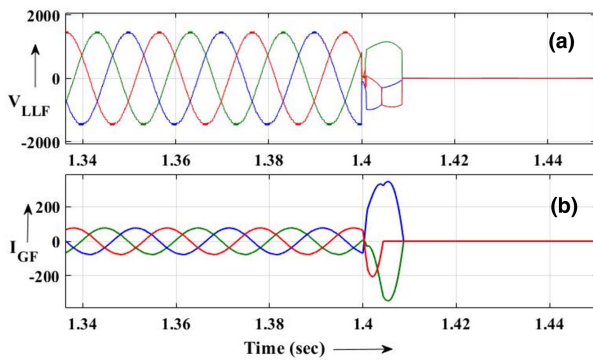


FIGURE 34. Inverter behavior after dc fault for presented topology. (a) Inverter output voltage. (b) Grid current.

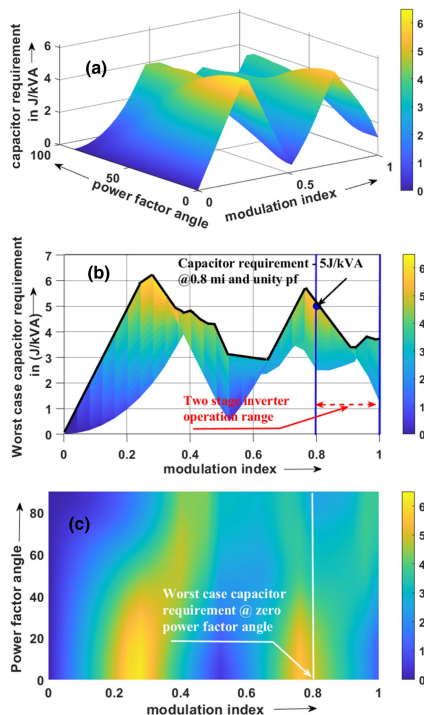


FIGURE 35. Worst-case capacitor requirement of main LDN (in modulation index range of 0.8–1). (a) 3-D plot. (b) Upper and lower boundaries of capacitor requirement. (c) Top view.

the modulation index and power factor angle for rated current and $\pm 10\%$ voltage ripple with respect to nominal voltage.

Fig. 35(a) shows the worst-case capacitor requirement for main-LDN in J/kVA w.r.t. different power factors and different modulation indexes. This plot has been taken from modulation index zero to unity and power factor angle of 0 to 90°. This 3-D plot has different peaks and those are basically peak of different capacitor requirements in different conditions.

However, the proposed inverter with its double stage operation is supposed to operate between 0.8 to unity modulation index. Hence, this modulation index range is considered for the worst-case capacitor requirement design.

Fig. 35(b) indicates the worst-case requirement of capacitance with respect to modulation index. These upper and lower

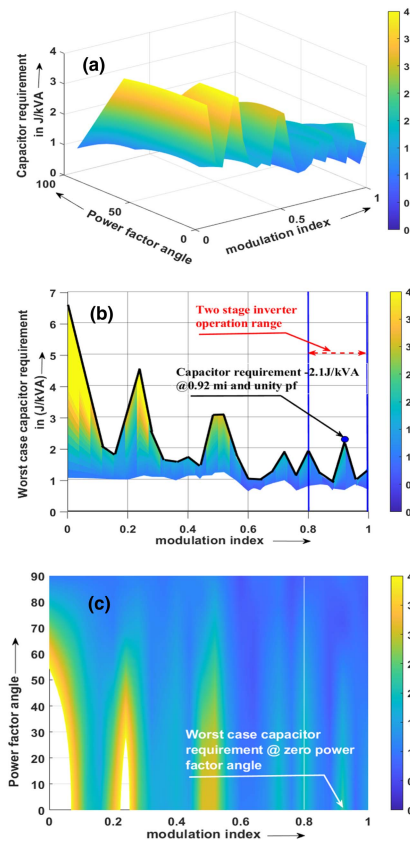


FIGURE 36. Worst-case capacitor requirement of auxiliary bridge (in modulation index range of 0.8–1). (a) 3-D plot. (b) Upper and lower boundaries of capacitor requirement. (c) Top view.

boundaries for each of the modulation index come at different power factor angles. Irrespective of power factor angle, this upper boundary is an indication of worst-case capacitor requirement. In Fig. 35(b), the worst-case capacitor requirement of main LDN is at 0.8 modulation index. The plot shown in Fig. 35(a) is evaluated further w.r.t. its top view, as shown in Fig. 35(c), where the magnitude of capacitor requirement can be found from its color map. In this plot, x and y axes are modulation index and power factor angle, respectively, and the z-axis can be seen from color map. From the color map, it is evident that the highest capacitor requirement for main LDN occurs at a modulation index of 0.8 and at unity power factor (at zero power factor angle).

Hence, from Fig. 35, it can be observed that the worst-case capacitor requirement for main LDN is 5 J/kVA. Similarly, plots are taken for auxiliary bridge and auxiliary LDN, and for them, the worst-case capacitor requirement is 2.1 J/kVA and 0.7 J/kVA, respectively, as shown in Figs. 36 and 37, for double-stage grid-connected operations. Hence, the total capacitor requirement in the two-stage inverter operation for a grid-connected application is 7.8 J/kVA.

The capacitor requirement for the presented converter topology is quite less as compared to the capacitor requirement in J/kVA for the MMC, which is considered

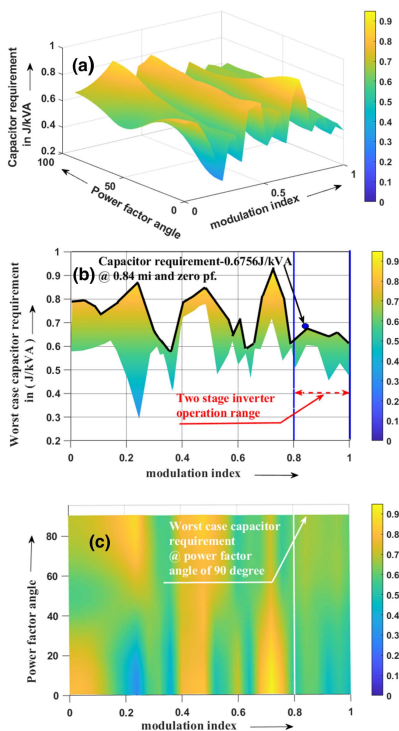


FIGURE 37. Worst-case capacitor requirement of auxiliary LDN (in modulation index range of 0.8–1). (a) 3-D plot. (b) Upper and lower boundaries of capacitor requirement. (c) Top view.

to be one of the well-accepted single dc-source-based high-resolution multilevel converter topologies that adapt very high number of switches to increase their resolution.

VII. HARDWARE RESULTS

A double LDN-based grid-connected asymmetrical multilevel inverter prototype is developed in the laboratory to validate simulation results, as illustrated in Fig. 38. In the proposed topology, dc buses of all the three phases of main bridges are merged using an isolation transformer, as shown in Fig. 8. It is fed by a common dc link maintaining a voltage of 160 V. An optimal ratio of 10:5:2:1 asymmetry is considered for implementation in hardware. Table 2 lists the key hardware configuration parameters.

For a 200 V line voltage and 5 A line current, the effective load impedance is 23.09 Ω per phase (star connection). Considering 50 Hz frequency of the grid, a 5 mH inductor will offer an impedance with the absolute magnitude of 1.57 Ω. Hence, the inductor used in the hardware prototype is effectively 0.067 PU of the total load impedance. Fig. 39 indicates the line-to-line voltage at channel-1 and the corresponding phase voltages at channel-2 and channel-3, respectively. These voltages are generated with a fixed dc bus voltage of main bridge. The off-grid inverter operation for a different modulation index is shown in Fig. 39(a)–(d). It is to be noted that for a two-stage grid-connected operation, the converter will operate in a narrow range of modulation index.

TABLE 2. Hardware Setup Parameters

Parameters	Specifications
Voltage of main bridge	160 V
Voltage of main LDN	80 V
Voltage of Auxiliary bridge	32 V
Voltage of main LDN	16 V
Line inductance (L)	5 mH
Switch specifications	SKM75GB12T4
Three-phase Grid voltage	200 V
Three-phase Grid current	5 A
Main LDN capacitor	4700 μF
Auxiliary bridge capacitor	4700 μF
Auxiliary LDN capacitor	4400 μF
Sampling frequency of dSPACE	25 kHz

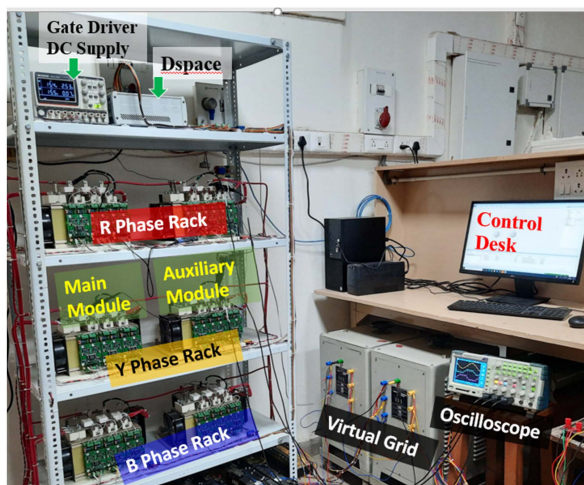


FIGURE 38. View of the experimental setup.

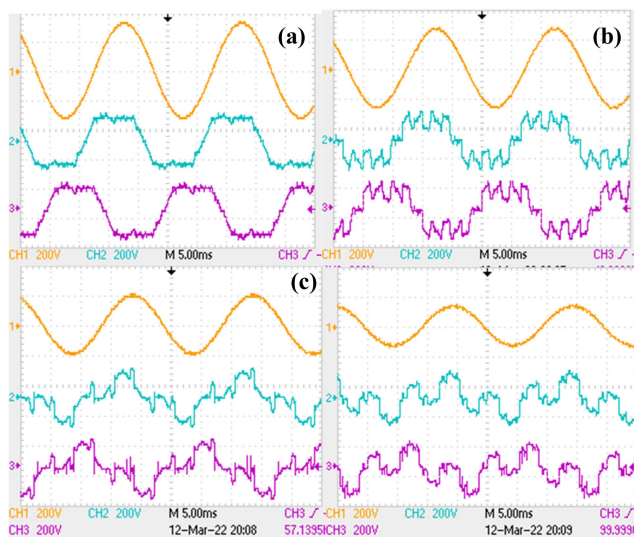


FIGURE 39. Line-to-line voltage and corresponding phase voltages at different modulation index (a) $m = 1$, (b) $m = 0.8$, (c) $m = 0.6$, (d) $m = 0.4$. Channel-1: Line-to-line voltage. Channel-2 and Channel-3: phase voltages.

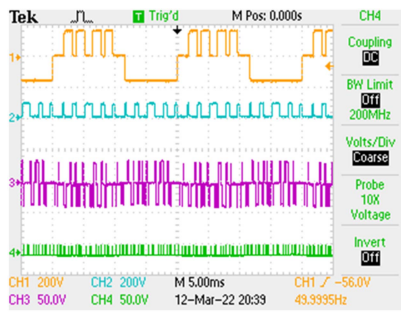


FIGURE 40. Individual cell voltages to form inverter phase voltages for 200 V grid voltage (@ modulation index 0.843). Channel-1: Main bridge. Channel-2: Main LDN. Channel-3: Auxiliary bridge. Channel-4: Auxiliary LDN.

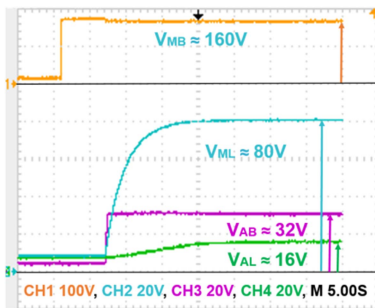


FIGURE 41. Capacitor voltage balancing: Channel-1: Main bridge; Channel-2: Main LDN; Channel-3: Auxiliary bridge; Channel-4: Auxiliary LDN.

However, during fault or in any abnormal grid condition, it is definitely needed to have an operation over the broad range of system voltage as this is usually demanded by the TSOs. The near-sinusoidal line-to-line waveform of inverter output voltage, as shown in Fig. 39, proves that all the four cell voltages are in balanced condition. The output of these four cells is also indicated in Fig. 40. Summing these voltages will result into corresponding phase voltage. LDN voltages are maintained at half of their corresponding bridge voltages and exhibit half-wave symmetry, as shown in Fig. 40. It is clear from Fig. 41 that converter is capable of balancing its floating capacitors over all the range of modulation indices so that it can be connected to the grid not only during the normal operation but also during fault.

When output voltage is varying over wide range, then in such a situation, it is required to supply active power or reactive power without exceeding its rated current capacity. The high-resolution three-phase line-to-line voltage at unity modulation index is shown in Fig. 42. The phase-locked loop is used to synchronize this converter topology to the grid. In the $d-q$ reference frame, active and reactive power are controlled by regulating currents. Grid and dc bus voltages are chosen such that the modulation index is restricted within 0.85 to synchronize with the grid. This ensures sufficient voltage headroom to inject reactive power into grid. Fig. 43(a) shows that inverter voltage and grid voltage are synchronized and there is no phase difference between them. Hence, there will

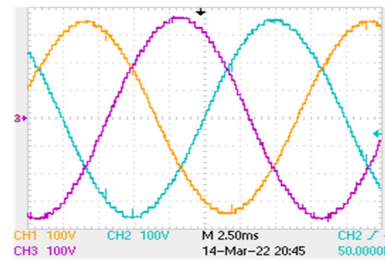


FIGURE 42. Three-phase line-to-line voltage at unity modulation index.

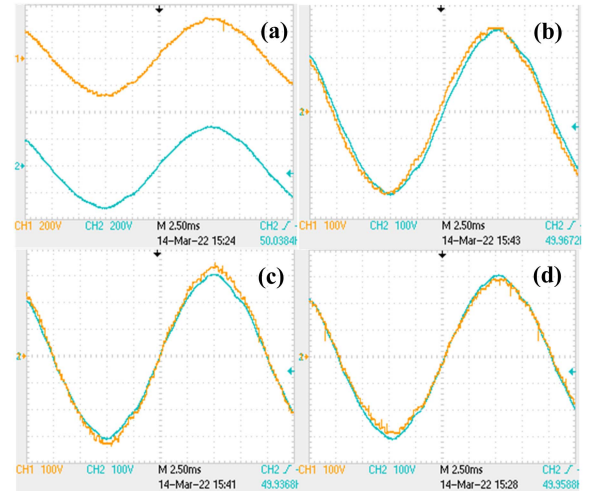


FIGURE 43. Grid synchronization and power flow control: Channel-1: inverter output voltage; Channel-2: grid voltage. (a) Inverter voltage and grid voltage with zero phase angle. (b) Leading inverter voltage with active power injection. (c) Reactive power injection. (d) Reactive power absorption.

be no power flow in absence of quadrature component. When quadrature component is added in grid voltage, then inverter voltage will lead the grid voltage by some angle, and it will be responsible for active power injection into the grid, as shown in Fig. 43(b). When inverter voltage will be greater than the grid voltage, then reactive power injection to the grid will take place, as shown in Fig. 43(c). Similarly, reactive power absorption from grid is shown in Fig. 43(d). This matches well with the concept presented in Section VI.

The power quality of inverter output voltage is a strong function of grid voltage when it operates at the grid following mode. Hence, for analyzing the converter's effectiveness to generate the desired power quality, the inverter is operated in the grid forming mode. In this case, the reference voltage is taken as pure sinusoidal. The FFT of inverter output voltage is shown in Fig. 44(a). It depicts that the fifth harmonic is below 40 dB to the fundamental (50 Hz) that means most dominating fifth harmonic is less than 1% of the fundamental. All other harmonic components are of negligible value. The grid current FFT plot in the grid following mode is shown in Fig. 44(b). It can be observed from Fig. 44(b) that all harmonic components in grid current are found below 50 dB of the fundamental component, i.e., below 0.31% of the

TABLE 3. Comparison of Various Topologies or Grid-Connected Solar PV Application

Topology	Two level[51]	Packed U-Cell [52]-[53]	Half-bridge MMC [54]	Full-bridge MMC [55]	Symmetric CHB [56]	Asymmetric CHB[57]	Presented topology
CVA stress of the devices	Low	Low	High	High	Low	Low	High
Power quality/ resolution	Very Low	Medium	Low	Low	Medium	Very High	Very High
Power imbalance due to partial shading	Not applicable	Not applicable	Very low	Very low	High	High	Very low
Interarray leakage current	No	Yes	No	No	Yes	Yes	No
DC fault blocking ability without dc circuit breaker	No	No	No	Yes	Yes	Yes	Yes
Reactive power injection limit	low	Medium	Low	Low	Medium	High	High
Floating Capacitor requirement	No	Yes	Yes	Yes	No	No	Yes
Switching loss	Very high	Moderate	Moderate	Moderate	Moderate	Very low	Very low
Conduction Loss	Low	Medium	High	High	High	Medium	Medium
Filter loss	High	Low	Medium	Medium	Low	Very low	Very low
Isolated auxiliary sources per phase	Not applicable	No	No	No	Yes	Yes	No

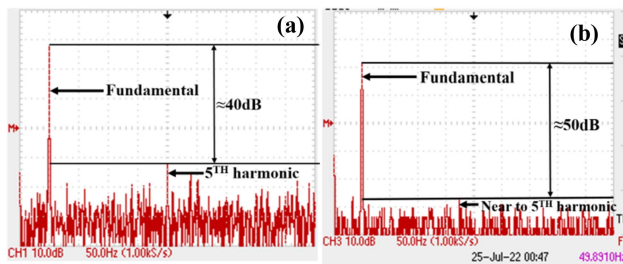


FIGURE 44. Power quality analysis. (a) FFT of grid voltage. (b) FFT of grid current.

fundamental. This is an indication of power quality within specified limit given in standards.

VIII. DISCUSSION

Solar PV systems are one of the most prominent sources of renewable energy. The levelized cost of electricity for solar PV systems is greatly influenced by the performance of power conditioning unit. The majority of practical challenges are associated with grid-connected PV inverters such as efficiency, reliability, power quality and cost. The presented two-stage single-sourced three-phase high-resolution converter topology is compared with other potential and well-known topologies in Table 3 to assess the benefits and limitations of presented topology as compared to other converter topologies for the grid-connected solar PV application.

The total cumulative voltampere (CVA) stress of switches is used to estimate the implementation cost of converter. In the presented topology, in order to eliminate isolated dc sources, CVA stress becomes more as compared to other converter topologies and almost equal to MMC. However, the presented converter topology generates a higher number of output voltage levels as compared to MMC. Despite the fact that the proposed topology appears to have a higher CVA requirement than standard two-level and MLI topologies, it

is important to keep in account that the implementation cost is not expected to increase substantially. This is due to the fact that total converter assembly contains many components other than the semiconductors. Moreover, in two-level or three-level inverters in order to maintain high power quality, derating of power semiconductor switches is required (high switching losses cause high junction temperature that requires derating of converter). This finally increases the CVA requirement of the semiconductor switches. In this section, derating of such converters is not considered. Estimation shows that it could lead to CVA rating of two-level inverter higher than the presented converter.

Present topology can generate a higher number of output voltage levels almost similar to asymmetrical converter topologies. However, asymmetrical converter topologies need a higher number of isolated dc sources than the presented topology that affects the converter cost. The high implementation cost is due to the wide range of power consumption of these isolated sources. Even if the two-level inverter is cost effective, it operates at very high switching frequency in order to get high power quality. For solar PV application (mainly in central inverter), most of the PV array voltage is restricted to 900 V (due to insulation limit), and for high power, it demands higher current (in few kiloampere scale). Operating the system at very high frequency with high current results in higher switching losses, which reduce efficiency and reliability. The two-level inverter with large filter helps to reduce losses and increase efficiency. However, cost, weight, and volume of filter are issues, which cannot be neglected.

The switching loss of the presented converter is negligible as compared to the symmetric CHB and MMC. This is due to the fact that main bridge operates at around fundamental switching frequency and the high switching frequency (1–2 kHz) is imposed to auxiliary cells.

Most of the multilevel inverter topologies have high conduction loss as compared to the two-level inverter. However,

in the presented topology, proper selection of switches can optimize conduction loss. The low conduction loss of MOSFETs makes them an appropriate choice for low-voltage auxiliary modules. IGBT (low frequency) or IGCT can be used in presented topology for main module (high voltage cells) to limit the conduction losses.

In this work, transformers are used to merge dc buses of three phases, which helps to reduce capacitor ripple (finally capacitor requirement) and also eliminates the interarray leakage current. In the presented topology, main bridge is fed by a common PV array, and consequently, there is no power imbalance among the phases owing to partial shading. However, in both symmetric and asymmetric CHBMLI, the PV array diverts from MPPT under partial shading in order to maintain power quality, and this can lead to power unbalancing. Moreover, in uneven shading, all modules cannot operate at same MPP. It results in leakage current due to interarray leakage capacitance.

The presented topology provides the dc fault blocking and limits the fault current without dc circuit breaker (already explained in Section IV). In case of two-level inverter, packed U-cell (PUC), and half-bridge MMC, if due to some reason dc fault occurs, huge short-circuit current may cause successive failure of switches.

The reactive power injection capability of the presented topology is high (as discussed in Section V) as compared to the two-level inverter and MMC. The current injection capability in two-level inverter and MMC is limited by voltage due to the high impedance of the filter inductor.

IX. CONCLUSION

A two-stage single dc-source-based high-resolution PV central-inverter topology is presented in this article. Filter requirement is substantially reduced owing to high-resolution inverter output voltage. This has significantly enhanced the reactive power injection capacity of the inverter owing to smaller voltage drop in coupling inductor. In addition to this, the high-resolution output voltage ensures power quality requirement of the grid. The superior characteristics of the dc fault blocking capability of inverter is also observed and compared with conventional two-level converter. Due to multiple floating capacitors, this converter can restrict the dc fault current compared to a conventional two-level converter. The device utilization of presented converter topology has been improved by adapting the two-stage operation of this converter for a grid-connected solar PV application. The two-stage configuration also offers higher energy capture by enabling multiple maximum power point trackers. The topology is inherently more robust due to losses distributed in a manner where switches operating at higher frequency need to handle less voltage. This also boosts efficiency of the system. Such attractive features with respect to existing central inverter topologies make the proposed inverter competitive. A detail simulation study together with supporting experimental results from the laboratory scale prototype validated the merits of the proposed converter configuration.

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