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Sizing Procedure of Reactive Electric Spring

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ABSTRACT Reactive electric spring (RES) is a technique aimed at stabilizing the user voltage in presence of grid voltage variations by means of a user-encapsulated circuit. In spite of the numerous papers on the matter, no expressions are still available to size the RES elements. This paper fills this lack, by drawing up a sizing procedure of them. The procedure starts with a targeted investigation of the RES operation and exploits the outcomes to provide expressions for the values of the passive elements as well as for the voltage-current ratings of the voltage source inverter (VSI). The sizing expressions are formulated in normalized form to emphasize their dependence on the parameters of the user non-critical load. Focus of the sizing procedure is on the two RES key-elements, namely the AC-side capacitor and VSI but the AC filter inductor and the DC-side capacitor are also sized. Two options for sizing the AC-side capacitor are also discussed. At last, the study case of a user supplied by a low-voltage distribution line is considered and the sizing expressions are utilized to calculate the RES data. Experimental results, obtained by an on-purpose arranged hardware-in-the-loop (HIL) rig, validate the sizing procedure.

INDEX TERMS User voltage stabilization, Reactive Electric Spring (RES), RES sizing, HIL experimentation.

NOMENCLATURE AND NOTATIONS

The nomenclature refers to Fig. 1, which shows the electric circuit of a user equipped with a reactive electric spring (RES).

A. ACRONYMS

CL	Critical load
ES	Electric Spring
RES	Reactive ES
NCL	Non-critical load
SL	Smart Load
VSI	Voltage Source Inverter

B. USER AND RES CORCUITAL ELEMENTS

C_{DC}	RES DC capacitor
C_{ES}	RES AC capacitor
f_G	Grid frequency
L_{CL}	CL inductance
L_f	RES filter inductor
L_{NCL}	NCL inductance
R_{CL}	CL resistance
R_{NCL}	NCL resistance
$\dot{Z}_G$	Line impedance

C. VARIABLES

$\bar{I}_I$	VSI AC-side current
$\bar{I}_{ES}$	C_{ES} current
$\bar{I}_{NCL}$	NCL current
$\bar{I}_{CL}$	CL current
$\bar{V}_{ES}$	C_{ES} voltage
V_{DC}	VSI DC-side voltage
$\bar{V}_G$	Grid voltage
$\bar{V}_I$	VSI AC-side voltage
$\bar{V}_{L,NCL}$	L_{NCL} voltage
$\bar{V}_{NCL}$	NCL voltage
$\bar{V}_{R,NCL}$	R_{NCL} voltage
$\bar{V}_S$	User voltage

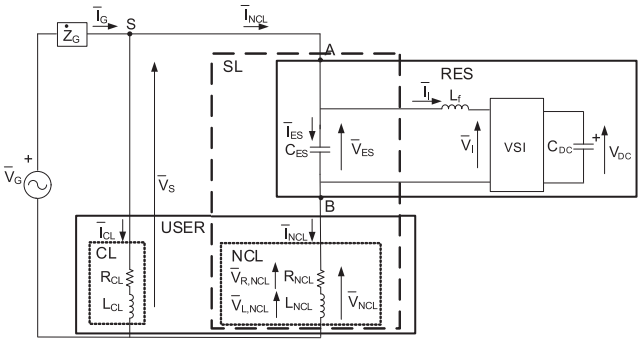

FIGURE 1. **Electric circuit of a user equipped with RES.**

Throughout the paper, the following notations are used: i) phasors and impedances are denoted by upper-case letters overlapped respectively with a bar and a point, ii) DC quantities and magnitudes of phasors and impedances are denoted by no-overlapped upper-case letters, whereby the phasor magnitudes are given in rms values; instantaneous values of the quantities are denoted by lower-case letters, iii) subscripts N, Ov and Uv denote quantities in nominal (N), grid overvoltage (Ov) and grid undervoltage (Uv) conditions, iv) subscripts Mx and Mn denote maximum and minimum values of the quantities within the RES operating range, and v) subscripts Sz and Nr denote respectively the sized quantities and their normalized expressions.

I. INTRODUCTION

The proliferation of intermittent renewable energy sources, such as wind and photovoltaic generators, together with their increasing contribution to the electrical capacity of the grid, is likely to produce a recurrent mismatch between power delivery and power demand [1]. Because of this mismatch, the supply voltage of the users is subjected to deviations that are not tolerated by their critical loads (CLs) [2]. As a matter of fact, a power mismatch due to a surplus of the power delivery increases the grid voltage beyond its nominal voltage and, with it, the user voltage, whilst a shortage of the power delivery decreases it [3]. To avoid that the power quality problem of a deviation in the user supply voltage hinders the deployment of renewable sources [4], various solutions have been proposed at both network and user level for the stabilization of the user supply voltage [5], [6].

Among the user level solutions, Electric Spring (ES) is a technique that has the merit of being put in place by means of a simple circuit [7], also named ES. The circuit is encapsulated in-between the supply point of the user and its non-critical load (NCL) and is essentially composed of an AC-side capacitor, hereafter shortly termed as AC capacitor, and a voltage source inverter (VSI) feeding the AC capacitor. By conception, ES stabilizes the voltage of a user in exchange of a certain deviation of the voltage across NCL.

ES comes in two basic versions: passive and active [8], [9]. In the passive version, like that one shown in Fig. 1, VSI is tied to a DC capacitor at its input side. Hence, a passive ES executes the stabilization task by putting into stake only reactive power and, for this reason, is also referred to as reactive ES (RES).

In the active version, VSI is fed by an energy source, like a battery. Hence, an active ES (AES) can execute the stabilization task by putting into stake both active and reactive power. This makes AES able to perform additional services, in favor of either the user or the grid, such as the power factor correction or the frequency regulation [10], [11], at the price of its higher cost and running complexity.

During the last years, the research activities on ES have been concentrated on its operation [12], circuital topologies [13], [14], and control [15], [16], while the sizing of its circuital elements is only touched upon in [17], [18]. Specifically, paper [17] deals with the setup of VSI and its AC output filter, dwelling on the choice of the switches, their snubbers, and the filter inductor, and paper [18] looks over the impact of some circuital elements on the stability of the ES behavior when connected to the grid.

All the quoted papers, whether they are concerned with either RES or AES, use similar values of the AC capacitor (in the order of 10 μF), but there is no explanation of how this value has been chosen; the same lack of explanations occurs for the other passive elements as well as for the electrical solicitations to which they and VSI are exposed. The purpose of this paper is to fill such a lack for RES, by drawing up a sizing procedure that determines the expressions for the values and the voltage-current ratings of the passive elements and the voltage-current ratings of VSI. The procedure focuses on the two RES key-elements, which are the AC capacitor and VSI, but sizing expressions for the AC filter inductor at the VSI output and the DC capacitor are also determined. It is worth to note that the obtained expressions, besides helping the designers to a prompt evaluation of the RES burden for any potential user, can become a source of reference for future studies on RES sizing.

In detail, the paper is organized as follows. Section II reviews the basic RES operation. Section III paves the way for the sizing procedure by a targeted investigation of the RES operation under grid voltage variations. Section IV formulates the sizing expressions for the RES circuital elements; two sizing options for the AC capacitor are discussed together with their impact on the VSI ratings. Section V applies the previously formulated expressions to the calculation of the RES data for the study case of a user supplied by a low-voltage (LV) distribution line; then, it validates the sizing procedure by the experimental testing of the study case, executed by means of an on-purpose arranged hardware-in-the-loop (HIL) rig. Section VI concludes the paper.

II. BASIC RES OPERATION

Let us refer to Fig. 1, where $\bar{V}_S$ is the voltage at user supply point S, and CL, NCL and SL are respectively the critical load, the non-critical load, and the so-called smart load of the user, being the latter made by the series of RES and NCL. The RES operation relies on a closed-loop control system,

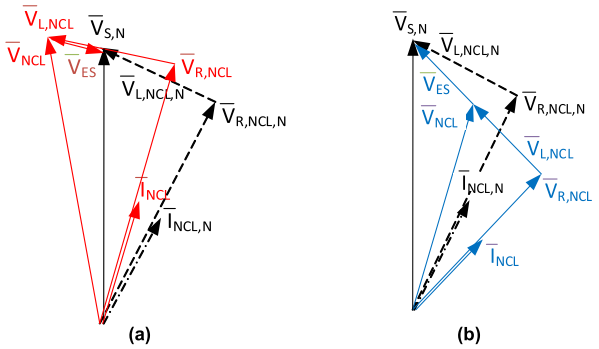

FIGURE 2. SL phasor diagram under (a) grid overvoltage, (b) grid undervoltage.

not shown in Fig. 1, that regulates the magnitude V_S of $\bar{V}_S$ at nominal value $V_{S,N}$ in spite of the grid voltage variations, thus keeping CL supplied at the nominal voltage. To this end, the control system adjusts voltage $\bar{V}_{ES}$ across C_{ES} by controlling VSI output voltage $\bar{V}_I$; the consequent change in the NCL current modifies the voltage drop across the impedance of the distribution line so as to contrast the grid voltage variations. In Fig. 1, the AC voltages and currents are represented in phasor form since the RES sizing is executed under sinusoidal operation. Indeed, voltage and current at the VSI output can be well approximated by their fundamental components on account of the high-frequency PWM control of VSI and the filtering role of inductor L_f.

The relationship between the currents in VSI, NCL and C_{ES} is

$$\bar{I}_I = \bar{I}_{NCL} - \bar{I}_{ES} \tag{1}$$

Current $\bar{I}_{ES}$ leads, of course, $\bar{V}_{ES}$ of $\pi/2$ whilst current $\bar{I}_I$ is lagging $\bar{V}_{ES}$ of $\pi/2$ for RES to exchange only reactive power with SL. It follows from (1) that i) $\bar{I}_{NCL}$ is in quadrature to $\bar{V}_{ES}$; it either leads or lags $\bar{V}_{ES}$ of $\pi/2$ depending on whether the magnitude of $\bar{I}_I$ is lower or greater than the magnitude of $\bar{I}_{NCL}$, and ii) impedance of RES as seen from the terminals A and B of Fig. 1 is of reactive type; moreover, it is capacitive if $I_I < I_{NCL}$ whilst it is inductive in the opposite case.

The circuit of Fig. 1 operates in nominal conditions when the user is supplied at $V_{S,N}$. In such conditions, RES does not exert any stabilizing action. Then, V_{ES} is zero and consequently $\bar{I}_I$ is equal to $\bar{I}_{NCL}$, meaning that VSI draws the NCL current. Under grid overvoltage, the control system forces $\bar{V}_{ES}$ to be in opposition to $\bar{V}_{L,NCL}$; then, current $\bar{I}_{NCL}$ increases and the same occurs for the active power absorbed by NCL; conventionally, a negative sign is assigned to the magnitude of $\bar{V}_{ES}$ under this situation. Conversely, under grid undervoltage, the control system forces $\bar{V}_{ES}$ to be in phase to $\bar{V}_{L,NCL}$; then, current $\bar{I}_{NCL}$ decreases and the same occurs for the active power absorbed by NCL; conventionally, a positive sign is assigned to the magnitude of $\bar{V}_{ES}$ under this situation. The two situations, which are exemplified in Fig. 2, are consistent with the ES concept of satisfying the power demand paradigm, whereby the change in the power absorbed by NCL tracks the change in the power delivery.

The nominal values of the user voltage and the NCL current are related by

$$V_{S,N} = Z_{NCL} I_{NCL,N} \tag{2}$$

where NCL impedance Z_{NCL} is given by

$$Z_{NCL} = R_{NCL}\sqrt{1+\tan^2\varphi_{NCL}} \quad \text{with } \tan\varphi_{NCL} = \frac{X_{NCL}}{R_{NCL}} \tag{3}$$

and φ_{NCL} is the phase angle of the NCL impedance. Quantities $V_{S,N}$, $I_{NCL,N}$ and Z_{NCL} in (2) and (3) are utilized as base values for the normalization.

III. RES STABILIZATION RANGE

The change in the voltage drop across the distribution line impedance contrasting the grid voltage variations hinges upon the change in the active component of the current drawn by the user and the resistive component of the line impedance [19]. Let V_S be stabilized at $V_{S,N}$; then, there is no change of current and voltages in the CL branch of the user, and the sizing of RES can be executed by investigating only the changes of currents and voltages in the SL branch.

A. RES STABILIZATION EXTREMES

1) GRID OVERVOLTAGE

Under grid overvoltage, the maximum active current that SL can draw is reached when $V_{R,NCL} = V_{S,N}$. When this occurs, SL absorbs only active power and the current flowing in it, expressed in normalized form, is

$$I_{NCL,Mx,Nr} \equiv \frac{\frac{V_{S,N}}{R_{NCL}}}{I_{NCL,N}} = \sqrt{1+\tan^2\varphi_{NCL}} \tag{4}$$

Moreover, $\bar{V}_{ES}$ exactly opposes to $\bar{V}_{L,NCL}$, and its magnitude gets the maximum negative value that, expressed in normalized form, is

$$V_{ES,Mx,Ov,Nr} = -\tan\varphi_{NCL} \tag{5}$$

Note that the voltage value in (5) is distinctive of the NCL impedance, specifically of its phase angle.

2) GRID UNDERVOLTAGE

Under grid undervoltage, the minimum current that SL can draw is zero and is reached when $\bar{V}_{ES}$ is exactly equal to $\bar{V}_{S,N}$. When this occurs, no active power is absorbed by NCL. In practice, it is mandated to supply NCL, even if at a reduced power, also under grid undervoltage [20]. This poses a minimum value, designated with $I_{NCL,Min}$, to the current drawn by NCL; in correspondence, V_{ES} gets the maximum positive value, designated with $V_{ES,Mx,Uv}$. Discussion about the values of $I_{NCL,Min}$ and $V_{ES,Mx,Uv}$ is conducted in Section IV.

B. RES OPERATING RANGE

When RES operates between the two extremes quoted above, the loci described by the tips of both $\bar{V}_{R,NCL}$ and $\bar{I}_{NCL}$ are

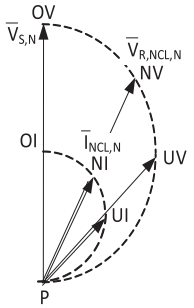

FIGURE 3. Loci of the voltage across R_{NCL} and the current through NCL.

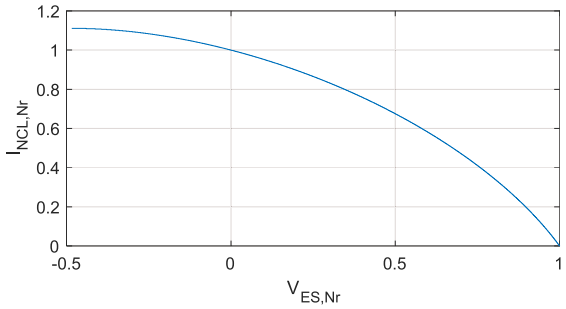

FIGURE 4. $I_{NCL,Nr}$ versus $V_{ES,Nr}$ for $\cos\varphi_{NCL} = 0.9$ and $V_{ES,Nr}$ extending up to 1.

semi-circumferences, as it can be readily realized from the fact that the SL impedance is of resistive-reactive type. The two loci are illustrated in Fig. 3, where NV and NI are the nominal operating points of $\bar{V}_{R,NCL}$ and $\bar{I}_{NCL}$, OV and OI are their extreme operating points under grid overvoltage, UV and UI are their extreme working points under grid undervoltage, and P is their common operating point if NCL would be not supplied under grid undervoltage.

The implicit relationship between the magnitude of $\bar{V}_{ES}$ and that one of $\bar{I}_{NCL}$ is

$$V_{S,N}^2 = \left(V_{L,NCL} + V_{ES}\right)^2 + \left(R_{NCL} I_{NCL}\right)^2 \tag{6}$$

By normalizing (6) to the nominal voltage and solving for I_{NCL}, the following equation is found that relates the normalized magnitude of the NCL current to that of V_{ES}:

$$I_{NCL,Nr} = \frac{-\tan\varphi_{NCL}}{\sqrt{1+\tan^2\varphi_{NCL}}} V_{ES,Nr} + \sqrt{1 - \frac{1}{1+\tan^2\varphi_{NCL}} V_{ES,Nr}^2} \tag{7}$$

Eq. (7) is the crux of the RES sizing. Its graph is plotted in Fig. 4 for $\cos\varphi_{NCL} = 0.9$; signs of I_{NCL} and V_{ES} agree with the assignments done in Section II.

IV. RES SIZING

RES sizing is meant at determining i) the values of the passive components of its circuit, ii) the current and voltage ratings of both the passive components and VSI. The sizing expressions are obtained by help of a procedure that exploits the investigation carried out in the previous Section.

The procedure starts by sizing C_{ES} and VSI. Afterwards, it is completed by sizing filter inductor L_f and DC capacitor C_{DC}.

A. C_{ES} SIZING

Eq. (5) is the maximum magnitude of the C_{ES} voltage under grid overvoltage. A convenient sizing criterion is to select an equal absolute value for the C_{ES} voltage under grid undervoltage, i.e., to impose

$$V_{ES,Mx,Uv,Nr} \triangleq -V_{ES,Mx,Ov,Nr} = \tan\varphi_{NCL} \tag{8}$$

This implies to set the normalized voltage rating of C_{ES}, denoted as $V_{ES,Sz,Nr}$, at $\tan\varphi_{NCL}$.

Further to (8), NCL is supplied also under grid undervoltage, thus satisfying the mandate declared in Section III. By (7) and (8), the NCL current takes the normalized minimum value of

$$I_{NCL,Mn,Nr} = \frac{1 - \tan^2\varphi_{NCL}}{\sqrt{1+\tan^2\varphi_{NCL}}} \tag{9}$$

In correspondence to (9) and for $\cos\varphi_{NCL} = 0.9$, the active power absorbed by NCL becomes about 47% of the nominal one, which is an acceptable reduction.

Current I_{ES} flowing into C_{ES} is proportional to V_{ES}. In normalized form, this can be expressed as

$$I_{ES,Nr} = Y_{ES,Nr} V_{ES,Nr} \tag{10}$$

where normalized admittance $Y_{ES,Nr}$ of C_{ES} is

$$Y_{ES,Nr} = -\frac{Z_{NCL}}{X_{ES}} \tag{11}$$

Its negative value agrees with the convention taken for the sign of the magnitude of V_{ES}.

Let us establish the RES sizing option, designated with A, of not overloading VSI with current. This means that I_I must not exceed current $I_{NCL,N}$ absorbed in nominal conditions.

From the shape of the I_{NCL}-V_{ES} curve in Fig. 4 and (1), option A is met by imposing that (11) is equal to the slope of the I_{NCL}-V_{ES} curve at $V_{ES} = 0$, i.e., by setting

$$-\frac{Z_{NCL}}{X_{ES}} = -\frac{\tan\varphi_{NCL}}{\sqrt{1+\tan^2\varphi_{NCL}}} \tag{12}$$

Solving (12), one gets the following expression for C_{ES}:

$$X_{ES,Sz,Nr} = \frac{\sqrt{1+\tan^2\varphi_{NCL}}}{\tan\varphi_{NCL}} \quad \rightarrow$$

$$C_{ES,Sz} = \frac{\tan\varphi_{NCL}}{2\pi f_G R_{NCL}\left(1+\tan^2\varphi_{NCL}\right)} \tag{13}$$

where f_G is the grid frequency. The maximum current flowing through $C_{ES,Sz}$ is attained at the edges of the V_{ES} range, i.e., for $V_{ES,Nr} = \pm\tan\varphi_{NCL}$. Its absolute value, which is given by (14), sets the normalized current rating of $C_{ES,Sz}$.

$$I_{ES,Sz,Nr} = \frac{V_{ES,Sz,Nr}}{X_{ES,Sz,Nr}} = \frac{\tan^2\varphi_{NCL}}{\sqrt{1+\tan^2\varphi_{NCL}}} \tag{14}$$

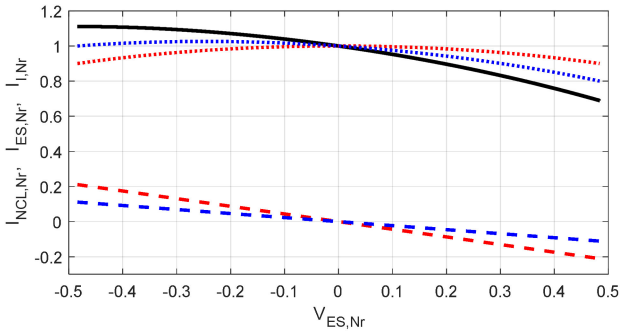

FIGURE 5. $I_{ES,Nr}$ and $I_{I,Nr}$ versus $V_{ES,Nr}$ for $\cos\varphi_{NCL} = 0.9$.

For the value of $C_{ES,Sz}$ in (13), current $I_{ES,Nr}$ as a function of $V_{ES,Nr}$ assumes the values traced in Fig. 5 with dashed red line, whereas the solid black line gives $I_{NCL,Nr}$ as a function of $V_{ES,Nr}$. As the figure outlines, the selection for (11) of a value greater than the slope of I_{NCL}-V_{ES} curve at $V_{ES} = 0$ would rise the value of C_{ES} without any benefit for the RES sizing.

An alternative RES sizing option, designated with B, is to employ a value of C_{ES} smaller than (13). For instance, by imposing that I_{ES} equates the difference between the value of I_{NCL} at $V_{ES,Mx,Ov}$ and $I_{NCL,N}$, it follows that

$$C'_{ES} = \frac{\sqrt{1+\tan^2\varphi_{NCL}} - 1}{2\pi f_G Z_{NCL} \tan\varphi_{NCL}} \tag{15}$$

It can be readily demonstrated that ratio c between C'_{ES} and $C_{ES,Sz}$, given by

$$c = \frac{C'_{ES}}{C_{ES,Sz}} = \frac{\left(\sqrt{1+\tan^2\varphi_{NCL}} - 1\right)\sqrt{1+\tan^2\varphi_{NCL}}}{\tan^2\varphi_{NCL}} \tag{16}$$

is less than 1, thus proving that C'_{ES} is less than $C_{ES,Sz}$. As an example, for $\cos\varphi_{NCL} = 0.9$, ratio c is equal to 0.53. The current flowing through C'_{ES} is traced in Fig. 5 with dashed blue line and, obviously, is c times less than the current flowing through C_{ES} for an equal value of V_{ES}.

The VSI currents for the two design options are worked out from (1) and are traced in Fig. 5 with dotted lines, whereas the red color is used for option A and the blue color for option B. They confirm that current I_I for option A never exceeds $I_{NCL,N}$ in the RES operating range, reaching this value just at $V_{ES} = 0$, i.e., in nominal conditions. Instead, current I_I for option B exceeds $I_{NCL,N}$ all along the RES operating sub-range related to the grid overvoltage situation; the excess gets a maximum of 2.6% at nearly half of the sub-range.

The RES sizing option A is here pursued; then, the value in (13) is taken for $C_{ES,Sz}$.

B. VSI SIZING

Further to the pursuit of RES sizing option A, current rating $I_{I,Sz}$ of VSI is equal to $I_{NCL,N}$, i.e., it is

$$I_{I,Sz,Nr} = 1 \tag{17}$$

Voltage rating of VSI is given by the maximum value of its DC-side voltage V_{DC}. Let the unipolar sinusoidal PWM technique be utilized to control VSI and let m_a be the amplitude modulation index and m_f be the frequency modulation ratio, i.e the ratio between PWM frequency f_{Sw} and f_G. For a value of m_f high enough, inductance L_f is somewhat small, and the voltage drop across it can be neglected. Further to this assumption, it follows that the maximum output voltage of VSI is $V_{ES,Mx}$. Therefore, by (8), the normalized nominal value of V_{DC} is equal to $\sqrt{2}\tan\varphi_{NCL}$. In practice, voltage V_{DC} is subjected to excursions ensuing from two causes, namely i) injection of a current harmonic because of the single-phase AC-DC conversion, and ii) joule losses in the VSI switches and the filter inductor. Cause i) produces a voltage oscillation superimposed to $V_{DC,N}$ at frequency $2f_G$, whilst cause ii) would produce a never-ending decay of V_{DC} if not properly tackled; this is commonly done by a closed-loop regulation of V_{DC} that balances the losses by forcing an active component of current into VSI [21]. Because of the regulation, the excursions of V_{DC} due to the losses are negligible compared to those due the oscillation produced by the current harmonic injection. It is common to confine the amplitude of such an oscillation within voltage band $\pm\varepsilon V_{DC,N}$ around $V_{DC,N}$ by the selection of an appropriate value for the DC capacitor. Then, the sizing voltage of VSI becomes

$$V_{DC,Sz,Nr} = \sqrt{2}\,(1+\varepsilon)\tan\varphi_{NCL} \tag{18}$$

where ε is a positive real number much lower than 1. VSI is modulated in the linear zone along the RES operating range to avoid the occurrence of low-order voltage harmonics. Then, maximum value of index m_a is set at $(1-\varepsilon)/(1+\varepsilon)$ in correspondence to (18) and becomes 1 when V_{DC} is equal to its minimum value of $\sqrt{2}\,(1-\varepsilon)\tan\varphi_{NCL}$. Note that, during RES operation, m_a ranges from 0 to 1, being equal to 0 in nominal conditions.

C. C_{DC} AND L_F SIZING

1) CAPACITOR C_{DC}

As anticipated above, value of DC capacitor C_{DC} must confine the voltage oscillation at frequency $2f_G$ across its terminals within voltage band $\pm\varepsilon V_{DC,N}$. The sizing criterion exposed in [22] is utilized to determine the value of C_{DC}; it imposes that impedance X_{DC} of C_{DC} at frequency $2f_G$

$$X_{DC} = \frac{1}{4\pi f_G C_{DC}} \tag{19}$$

has to fulfill the following equation:

$$X_{DC} = \frac{\varepsilon V_{DC,N}^2}{2V_{I,Sz}I_{I,Ov}} \tag{20}$$

where $I_{I,Ov}$ is the VSI output current under grid overvoltage and by (1), (4) and (14) is equal to $\sqrt{1+\tan^2\varphi_{NCL}}$. It is worth noting that $V_{I,Sz}\cdot I_{I,Ov}$ is the apparent power delivered by the VSI under grid overvoltage and it is the same delivered under grid undervoltage. By equating (19) to (20) and normalizing

TABLE 1 Sizing Procedure Results

RES quantity	Normalized sizing expression
C_{ES} capacitance ($X_{ES,Sz,Nr}$)	$\frac{\sqrt{1+\tan^2\varphi_{NCL}}}{\tan\varphi_{NCL}}$
C_{ES} voltage ($V_{ES,Sz,Nr}$)	$\tan\varphi_{NCL}$
C_{ES} current ($I_{ES,Sz,Nr}$)	$\frac{\tan^2\varphi_{NCL}}{\sqrt{1+\tan^2\varphi_{NCL}}}$
VSI current ($I_{I,Sz,Nr}$)	1
VSI voltage ($V_{DC,Sz,Nr}$)	$\sqrt{2}(1+\varepsilon)\tan\varphi_{NCL}$
L_f reactance ($X_{f,Sz,Nr}$)	$\frac{0.37(1+\varepsilon)\tan\varphi_{NCL}}{\gamma(2m_f-1)}$
C_{CD} reactance ($X_{CD,Sz,Nr}$)	$2\varepsilon\tan\varphi_{NCL}\sqrt{1+\tan^2\varphi_{NCL}}$

the quantities, the sizing expression of C_{DC} becomes

$$X_{DC,Sz,Nr} = 2\varepsilon\tan\varphi_{NCL}\sqrt{1+\tan^2\varphi_{\mathrm{NCL}}} \quad \rightarrow$$
$$C_{DC,Sz} = \frac{1}{4\pi f_G \varepsilon\tan\varphi_{NCL}\sqrt{1+\tan^2\varphi_{\mathrm{NCL}}}Z_{NCL}} \tag{21}$$

2) FILTER INDUCTOR L_F

The filter inductor plays the role of mitigating the harmonics of current produced by the PWM control of VSI. Before going on, it is useful to remember that i) the highest VSI output voltage harmonics with the unipolar PWM are of order $2m_f \pm 1$, and ii) their maximum magnitude is reached for $m_a = 0.6$ and is equal to

$$V_{I,2mf\pm1,Nr} = 0.37V_{DC,Sz,Nr}/\sqrt{2} \tag{22}$$

Value L_f of the filter inductor is sized by the criterion exposed in [22]; it states that the impedance of L_f must keep the current harmonic of highest amplitude and lowest order (here, $2m_f$-1) at a specific level of the maximum output VSI current, i.e., it must be

$$X_{f,Sz,Nr} = \frac{V_{I,2mf-1,Nr}}{I_{I,2mf-1,Nr}} \text{ with } I_{I,2mf-1,Nr} = \gamma I_{I,Sz,Nr} \tag{23}$$

where γ is the level ratio. Eq. (23) relies on the assumption of neglecting the impedance downstream the filter inductor that, at the harmonic of order ($2m_f$-1), is dominated by C_{ES}. By (17), (18), (22) and (23), the sizing expression of L_f in normalized form is

$$X_{f,Sz,Nr} = \frac{0.37\,(1+\varepsilon)\tan\varphi_{NCL}}{\gamma\,(2m_f-1)} \quad \rightarrow$$
$$L_{f,Sz} = \frac{0.37\,(1+\varepsilon)\tan\varphi_{NCL}Z_{NCL}}{\gamma\,(2m_f-1)\,2\pi f_G} \tag{24}$$

where $X_{f,Sz,Nr}$ is the reactance at the grid frequency.

D. SIZING PROCEDURE RESULTS

The results of the RES sizing procedure are summarized in Table 1.

The normalized sizing expressions of the RES quantities point out that

- VSI current is unity further to the pursued sizing option,
- all other quantities are affected by NCL only via the tangent of its impedance phase angle,
- VSI voltage, L_f reactance and C_{CD} reactance are also affected by: i) specifications ε and γ, respectively for the voltage excursions across the DC capacitor and the current harmonics at the VSI output, and ii) VSI frequency modulation ratio m_f.

TABLE 2 Study Case User Data

Quantity	Value
User Nominal Voltage ($V_{S,N}$)	230 V
Grid Frequency (f_G)	50 Hz
CL Nominal Current (I_{CL})	4.8 A
CL Power Factor ($\cos\varphi_{CL}$)	0.9
NCL Nominal Current ($I_{NCL,N}$)	24.2 A
NCL Power Factor ($\cos\varphi_{NCL}$)	0.9
LV Distribution Line Impedance (Z_G)	1 Ω
LV Distribution Line ($\cos\varphi_G$)	0.95

TABLE 3 Study Case RES Data

Quantity	Value
C_{ES} voltage	111 V
C_{ES} current	5.1 A
C_{ES} capacitance	145 μF
VSI voltage	165 V
VSI current	24.2 A
C_{DC} capacitance	6.23 mF
L_f inductance	142 μH

V. STUDY CASE

The results of the RES sizing procedure are exemplified for the study case of a user equipped with RES and supplied at 230 V, 50 Hz by a LV distribution line. The user data of the study case are reported in Table 2. Base values of voltage, current and impedance are respectively $V_{S,N} = 230$ V, $I_{NCL,N} = 24.2$ A and $Z_{NCL} = 9.5\ \Omega$. Design specifications for ε, γ and m_f are respectively 0.05, 0.05 and 400 ($f_{PWM} = 20$ kHz).

A. RES DATA

By (8), (13) and (14), the sizing data for C_{ES} are calculated in: capacitance of 145 μF, voltage of 111 V and current of 5.1 A. By (17) and (18), current and voltage ratings of VSI are respectively 24.2 A and 165 V. Lastly, by (21), the DC capacitance is calculated in 6.23 mF and, by (24), the filter inductance in 142 μH. The maximum magnitude of the ($2m_f$-1)-th voltage harmonic across C_{ES} is found to be of $3.34 * 10^{-2}$ V, and that of the fundamental component of the voltage drop across L_f of 1.08 V, thus verifying the assumptions stated in the sizing procedure. The calculated data are summarized in Table 3. They disclose that the RES data are not very demanding, apart from the value of the DC capacitor due to the single-phase AC-DC conversion.

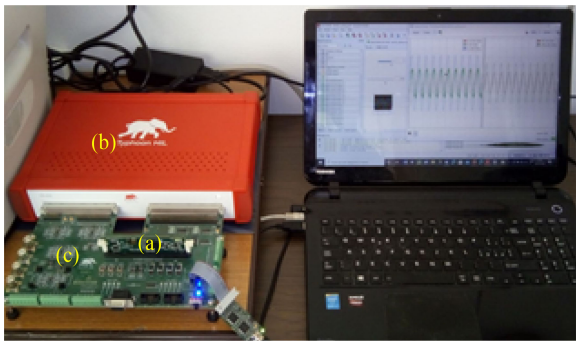

FIGURE 6. Experimental rig: (a) TMS320F28335 card, (b) Typhoon HIL 402 real time emulator, (c) interface board.

Taking into consideration the line impedance, the sized RES is able to stabilize the user voltage against its deviations within the range 220-232 V.

B. EXPERIMENTAL TESTING

The study case has been implemented in an experimental rig and then tested to validate the sizing results. The rig consists of a Typhoon HIL402 real time emulator, a TMS320F28335 DSP control card and a board interfacing the twos, as pictured in Fig. 6.

The RES control system has been designed by exploiting the diagram and the transfer functions arranged in [23]. The algorithms have been synthesized in discrete form by setting the sampling time at $1/f_{PWM}$; they have been first written in C language and then uploaded in the DSP card. The study case has been subjected to the test described below and the samples of the RES and NCL currents and voltages have been recorded by a digital oscilloscope and processed by MATLAB for displaying purposes.

The test starts with the circuit operating in overvoltage conditions and goes on by suddenly dropping the grid voltage at 0.06 s. The magnitude of the grid voltage is such as to lead the user voltage respectively up to 232 V and down to 220 V with no RES regulation.

The responses of the study case to the test are plotted in Fig. 7, whereby Fig. 7(a) plots user voltage v_S (continuous red line), AC capacitor voltage v_{ES} (dashed green line) and VSI current i_I (dotted blue line), whilst Fig. 7(b) plots NCL voltage v_{NCL} (continuous red line) and NCL current i_{NCL} (dotted blue line). To make the current plots more visible, their amplitude has been multiplied by 5. The plots of Fig. 7 demonstrate the excellent RES capabilities in stabilizing v_S at the nominal value of 230 V; moreover, they show that i) under the grid overvoltage, v_{ES} and i_I become respectively equal to 113 V and 22 A, whilst v_{NCL} and i_{NCL} increase respectively to 225 V and 26.7 A, ii) under the grid undervoltage, v_{ES} and i_I -as per design- take again the values of 113 V and 22 A, whilst v_{NCL} and i_{NCL} decrease to 160 V and 16.7 A. Incidentally, it can be noted that the RES control system is able to restore the nominal value of v_S within four grid periods, after the step

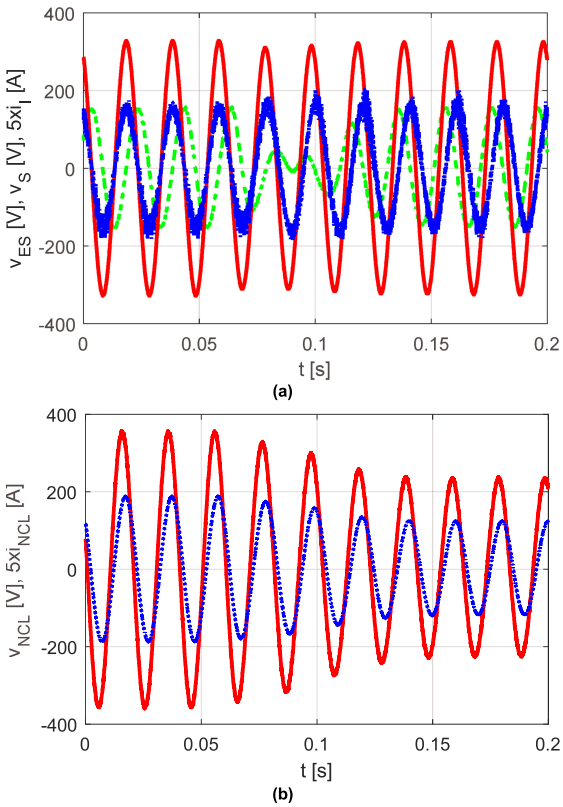

FIGURE 7. Experimental testing: (a) user voltage, C_{ES} voltage and VSI AC-side current, (b) NCL current and voltage.

variation of the grid voltage from its maximum-to-minimum value.

All the voltage and current values obtained from the experimental test in grid overvoltage and undervoltage conditions are in full agreement with what is predicted in Sections III and IV, thus validating the sizing expressions for the RES elements.

VI. CONCLUSION

The paper has presented a procedure to size the circuital elements of RES utilized to stabilize the user voltage under grid voltage variations. The procedure has evolved around the investigation of the RES operation at the extremes of the stabilization range. The outcomes of this investigation have allowed the seamless formulation of the sizing expressions of the two RES key-elements: the AC capacitor and VSI, finding out that they are strictly related only to the NCL impedance. Subsequently, the values of the other two RES elements: the filter inductor and the DC capacitor, have been formulated, finding out that they are also affected by the need of limiting the non-idealities inherent in the VSI conversion.

The sizing expressions have been utilized to calculate the RES data for the study case of a user supplied by a LV distribution line and have been validated by HIL-based experimental testing.

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