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Crosstalk Induced Shoot-Through in BTI-Stressed Symmetrical & Asymmetrical Double-Trench SiC Power MOSFETs

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ABSTRACT In this paper, the crosstalk-induced shoot-through current and induced gate voltage of SiC planar MOSFETs, SiC symmetrical double-trench MOSFETs and SiC asymmetrical double-trench MOSFETs is investigated on a half-bridge circuit to analyse the impact of temperature, drain-source voltage switching rate, gate resistance and load current level on crosstalk-induced properties of different SiC MOSFET structures. It shows that due to the smaller gate-source capacitance, the two double-trench MOSFETs exhibit higher induced gate voltage during crosstalk with the same external gate resistance, which together with the higher transconductance, yield higher shoot-through current than the planar MOSFET. Accordingly, their shoot-through current decreases with increasing of the load current while the planar MOSFET exhibits an opposite trend. The different trend of shoot-through current with temperature on DUTs reveals that the crosstalk in different device structures are dominated by different mechanisms, i.e. threshold voltage and channel mobility with the gate-source capacitance influencing the amplitude. Impact of bias temperature instability with positive and negative gate stressing is measured with a range of stress and recover periods at temperateness ranging between 25 °C to 175 °C. These measurements show that the peak shoot-through correlates with the threshold drift, though with less sensitivity for SiC symmetrical and asymmetrical double-trench MOSFETs compared with the planar SiC MOSFET where the inter-dependence is pronounced. A model is developed for the induced gate voltage and shoot-through current during crosstalk with channel current considered. The comparison of the model results with measurement confirms its capability to predict crosstalk in different MOSFET structures.

INDEX TERMS MOSFET, silicon carbide, crosstalk, double-trench, Bias temperature instability.

I. INTRODUCTION

With the introduction of SiC technology as a replacement of Silicon MOSFETs, better performance is achieved in a wide range of industrial applications. One of the main advantages of SiC MOSFET is its smaller die size, enabling smaller parasitic capacitances [1] which in turn enable fast switching rates. The common switching frequency in Silicon IGBTs is 10 kHz while it can rise to up to 100 kHz by SiC MOSFETs [2]. This enables less switching loss and smaller passive filter requirements, saving space and weight.

In half bridge arrangements as appeared in synchronous dc-dc converters or three-phase dc-ac inverters, one problem for circuit operation is the crosstalk. This mechanism behind this phenomenon is explained in [3], [4]. During the switching event of one device, voltage transition occurs on the complementary device thus displacement current flows through

its gate-drain capacitance. Spurious gate voltage is induced when such displacement current further flows through gate resistance and would unintentionally turn-ON the device once threshold voltage is exceeded. Three factors determines the spurious gate voltage magnitude which are gate resistance, voltage switching rate and ratio of gate-drain capacitance to gate-source capacitance. Hence, SiC MOSFET with capability of high frequency operation are more vulnerable to crosstalk in which the device is driven in semi-short-circuit mode with large thermal stress, arousing reliability issue. Models have been introduced to predict the spurious gate voltage [5]–[7] based on simplified capacitor-resistor circuit. However, under fast switching situation, especially encountered for SiC MOSFET, the parasitic inductance on the loop can no longer be neglected [8], [9] and its impact have been taken into account for spurious voltage calculation [2], [10]. Quite a few work has been done for evaluating crosstalk on SiC MOSFET power module and discrete devices [11]–[13], but little efforts on the latest SiC trench MOSFET.

In this paper, a model is developed for predicting the envelope of shoot-through current during crosstalk, and the magnitude and duration of crosstalk is compared for three devices of similar power rating with different structures under a wide range of switching rate, ambient temperature, gate resistance and load current levels. The cross-sectional schematic drawing of the devices under test is shown in Fig. 1 as Planar, Symmetrical Double-trench and Asymmetrical Double-trench structures [14]. Compared with the planar MOSFET which is the conventional structure, symmetrical double-trench MOSFET is able to deliver lower on-resistance [15], [16] as it implements trenched source region to suppress the E field stress on the gate oxide [17]. However, it also introduced the JFET region between the gate trench and source trench if unit cell is decreased significantly which worsens the static performance [18]. Asymmetrical double-trench MOSFET removes one of the potential JFET regions with one of the source trenches being attached to the gate trench, allowing further scaling down of the unit cells. Another advantage is that the source region semi-surrounds the gate so that the overlapping area of gate to drain is reduced, gate-drain capacitance is reduced to enable faster switching [19], [20]. Given the restrictions experienced by different structures of planar and double-trench SiC devices in terms of bipolar gate voltage limits and *dV/dt* capability, different suppression mechanisms may be needed to effectively mitigate the crosstalk. This work aims to shed light on properties of crosstalk in these different structures to enable selection of appropriate suppression method for each case. Section II discuss the models developed to predict the properties of crosstalk for these structures, Section III describes the experimental set-up, Section IV discusses the measurements analysis while Section V concludes the paper.

II. MODELING OF CROSSTALK

As mentioned, models for the induced spurious gate voltage for SiC MOSFET during crosstalk has been constructed in [2], [5]–[7], [10]. However, these models ignore the impact of shoot-through current incorporating the parasitic inductance on the power loop, and therefore, are unable to predict the peak shoot-through. In this paper, a model for crosstalk is developed with shoot-through current considered. The impact of each parasitic inductance on switching of a MOSFET has been studied in [10], [21]. These indicate that the mutual inductance shared by the main power loop and the gate loop significantly contribute to the disturbances compared with other parasitics on the gate and drain terminal.

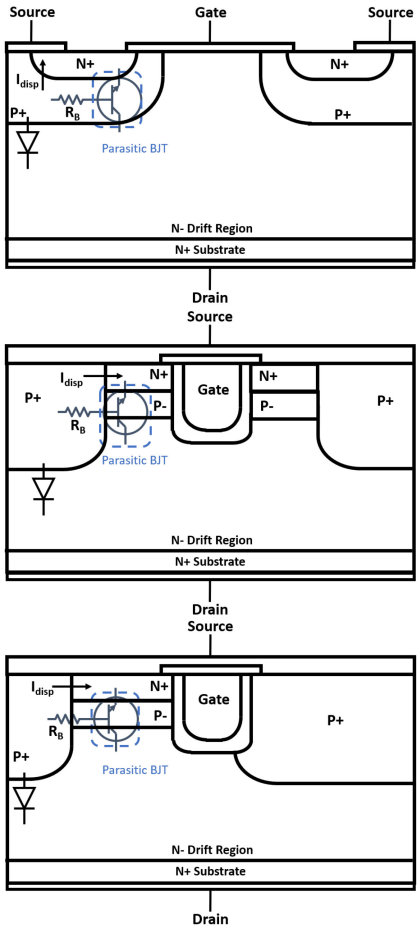

FIG. 1. From top: cross-sectional schematic of SiC planar MOSFET, SiC symmetrical double-trench & SiC asymmetrical double-trench MOSFETs.

The crosstalk can be divided into two stages. The first stage is when the induced gate voltage has not exceeded the threshold value, that is, no shoot-through current occurs and there is only displacement current flowing in the device. The second stage is when the induced gate voltage reaches the threshold value and MOSFET channel is parasitically turned-ON. The MOSFET at this stage is operating at saturation region. The equivalent circuit for these two stages are presented in Fig. 2 where drain, source and gate are represented as D, S and G respectively. In both cases, the drain-source capacitance C_{DS} is omitted [10] as a result of small die area of SiC MOSFET, yielding rather small displacement current through it [10]. The

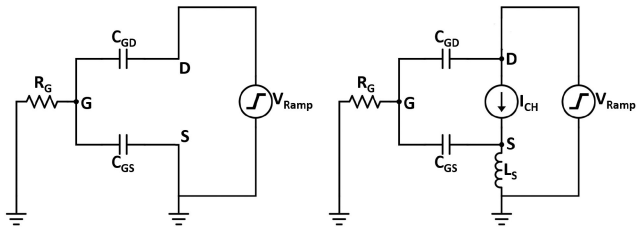

FIG. 2. Equivalent circuits of crosstalk at (top) first & (bottom) second stages.

voltage source V_{Ramp} represents the voltage transition over the DUT initiated by the turn-ON of top device, expressed as:

$$V_{Ramp} = K * t \tag{1}$$

where K is the slew rate until reaching the supply voltage.

During the first stage. Since the shoot-through is not happening, the parasitic inductances on the power loop is neglected for simplification. According to [5], the induced gate voltage has been calculated as:

$$V_{GS} = R_G C_{GD} K (1 - e^{\frac{-t}{R_G C_{ISS}}}) \tag{2}$$

In the second stage, with the increase of induced gate voltage above threshold, a current source representing the MOSFET channel is added to the equivalent circuit as well as the parasitic inductances which produce voltage under channel conduction. Parasitic inductance at drain is neglected since it is shown to have small impact on the induced gate voltage compared with that at source [10]. The equation for the current source of MOSFET channel is given as:

$$I_{CH} = g_{fs} * (V_{GS} - V_{TH}) \tag{3}$$

where g_{fs} is the device transconductance. At this stage, the gate voltage V_G has an initial value of V_{TH}, therefore, can be written as:

$$V_G = V_G' + V_{TH} \tag{4}$$

where V_G' is the variation of V_G during the second stage. Hence, equations can be written for the equivalent circuit as:

$$V_D = V_{Ramp} \tag{5}$$

$$\frac{dC_{GD}(V_{DG}) * V_{DG}}{dt} = \frac{V_G}{R_G} + C_{GS}\frac{d(V_{GS})}{dt} \tag{6}$$

$$V_S = L_S \frac{dI_S}{dt} \tag{7}$$

$$I_S = I_{CH} + C_{GS}\frac{d(V_{GS})}{dt} \tag{8}$$

The gate-drain capacitance C_{GD} is known to be highly dependent on the drain bias, an empirical equation is used for modeling [22]:

$$C_{GD} \approx \frac{C_0}{1 + K\sqrt{V_{DS}}} \tag{9}$$

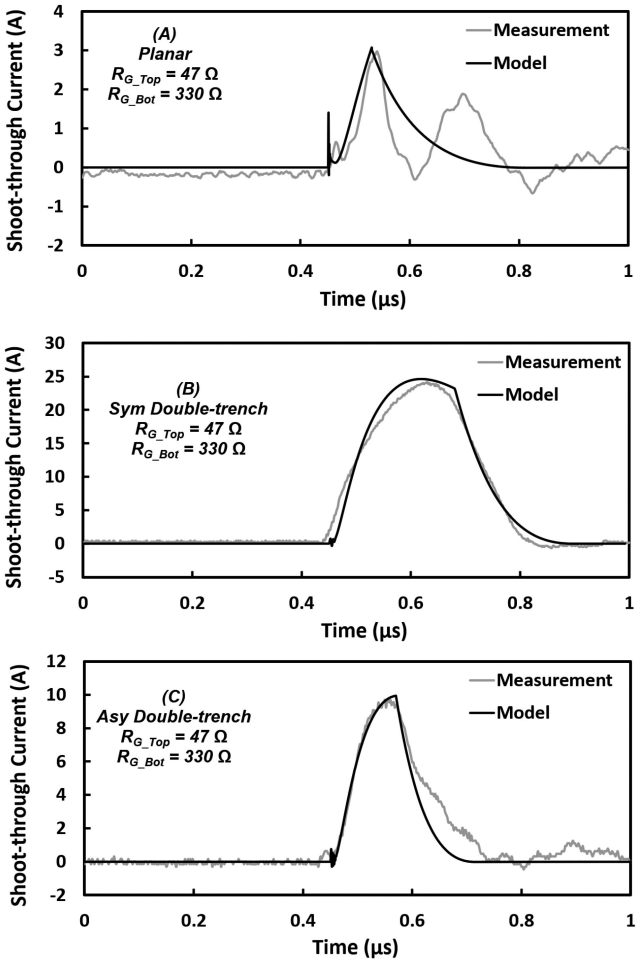

FIG. 3. Modeling of shoot-through current transient waveform with comparison to measurement.

where K and C_0 are fitting parameters. It must be noted that in asymmetrical double-trench MOSFETs, the source region is semi-surrounding the gate trench so that the gate to source overlapping area is increased but gate to drain overlapping area is reduced [19]. Therefore, the gate-source capacitance is increased, and the gate-drain capacitance is reduced compared with the symmetrical double-trench MOSFETs.

A SPICE model based on the circuit shown in Fig. 2 is created and ran for modeling. The transient shoot-through current and induced gate voltage are compared between measurement and modelling in Figs. 3 and 4 for the case of R_{G_Top} and R_{G_Bot} equal to 47 Ω and 330 Ω respectively. The peak values of shoot-through current are extracted from model and measurement for three different structured MOSFETs are plotted in Fig. 5 for a range of R_{G_Bot} with R_{G_Top} equal to 47 Ω. The model's outputs are well representative of the measurements of crosstalk properties with a clear correlation with general envelope of measurements, albeit with some shortfall on the oscillations. The discrepancy is due to the impact of the gate path that is modelled as purely resistive while there are some

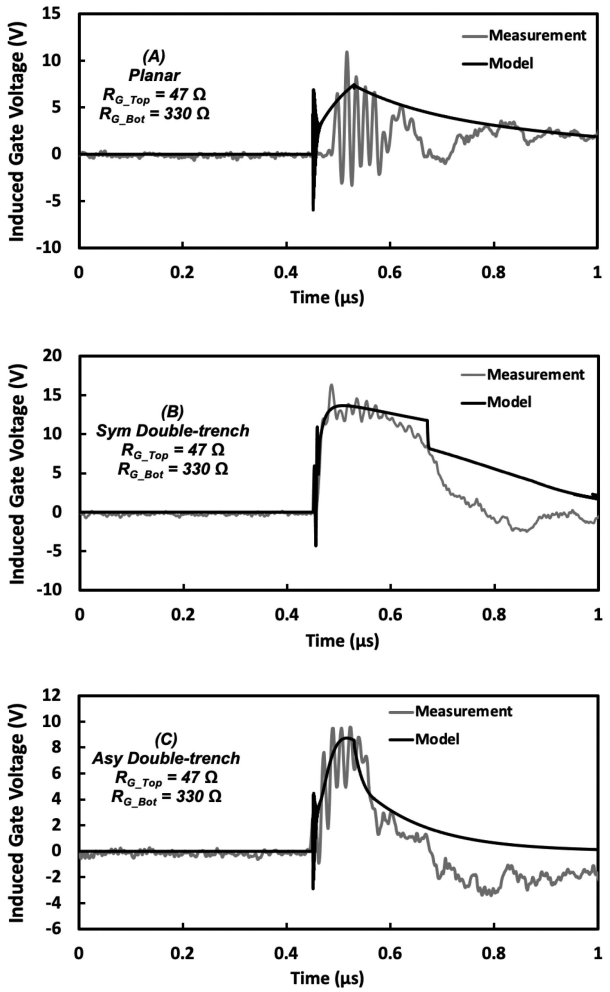

FIG. 4. Modeling of Induced gate voltage transient waveform with comparison to measurements.

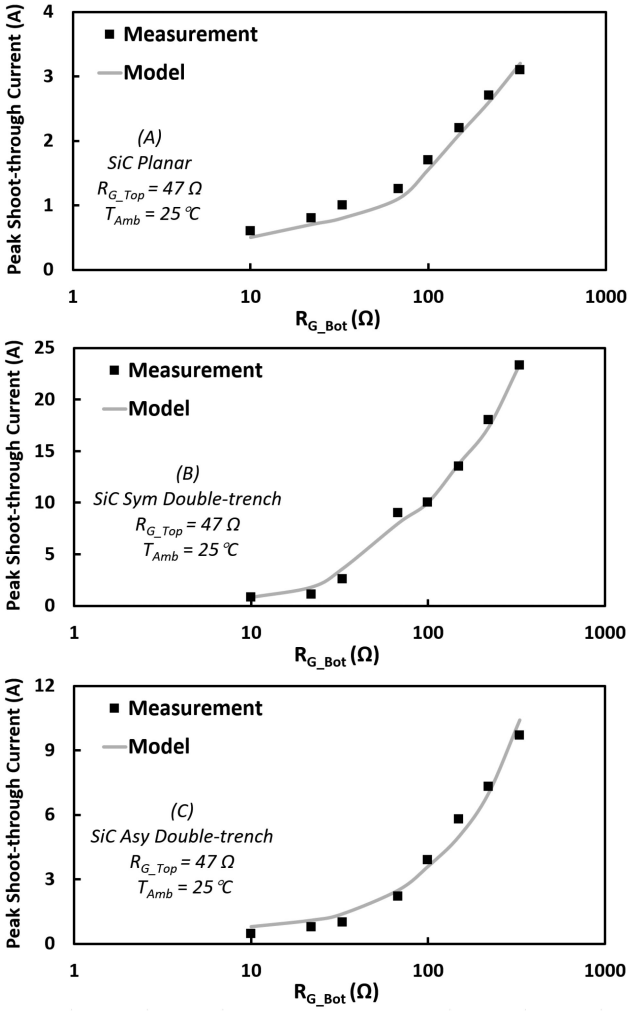

FIG. 5. Modelling of peak shoot-through current with comparison to measurements.

small parasitic inductance and capacitance associated with it, including within the gate driver chip.

III. EXPERIMENTAL SETUP

Experimental measurement are carried out on Rohm SiC planar MOSFET SCT2160, Rohm SiC symmetrical double-trench MOSFET SCT3160 and Infineon asymmetrical double-trench MOSFET IMW120R140M1HXKSA1. The test circuit is shown in Fig. 6 with its schematic which is a half-bridge [23]. The top switching device is fixed to make a fair comparison for DUTs placed at bottom. A transistor socket is used to connect the SiC power MOSFETs to the PCB board. The pin-to-pin parasitic parameters of this socket are measured using the impedance analyser Wayne Kerr 6500B with values as 5.25 nH and 3.6 m Ω at 1 MHz. These are not impacting the measured properties of crosstalk. A single pulse from 18 V/0V gate driver is fed to top switching device so that the full supply voltage V_{DD} falls on DUT at bottom and initiates crosstalk. The R_{G_Top} ranges from 10 Ω to 100 Ω for different switching speed while R_{G_Top} ranges from 10 Ω to 330 Ω to achieve different shoot-through current level. The shoot-through current is measured at the source of DUT with CWT Ultra-mini Rogowski coil (CWT1) and voltage is measured with GW-Instek GDP-100 100 MHz voltage probe on a Keysight MSO7104 A 1-GHz 4 GSa/s oscilloscope. The bandwidths of the probes enable capturing the switching waveforms in the interest of this paper. Further increase of bandwidth enables better capturing of the potential noise on the switching transient waveforms. This, for example, would be necessary in design of gate drivers that aim to suppress the disturbances. This is especially the case for SiC devices where the switching transients are faster, and the device is more prone to oscillations and disturbance by the circuit loop inductance at its output terminals. Devices with the same structure but with different current/voltage ratings are primarily different by the size of die which impacts the size of parasitic components that in turn would influence the magnitude of crosstalk shoot-through and the induced gate voltage. Ambient temperature on DUTs is varied from 25 °C

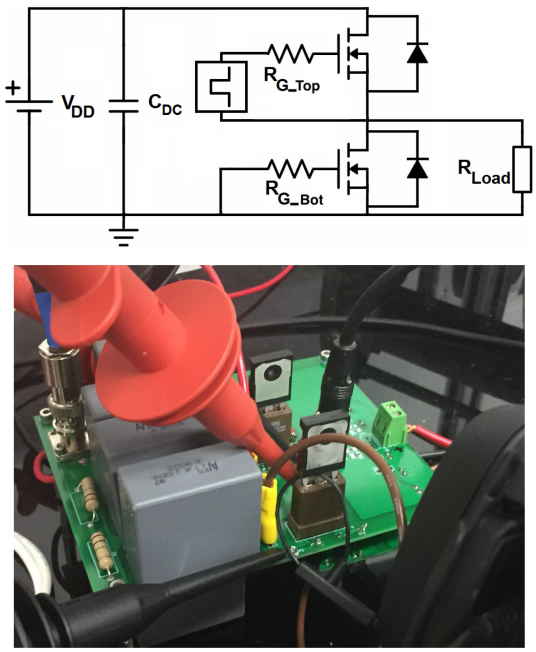

FIG. 6. Test circuit schematic and set-up for crosstalk measurement.

TABLE 1 Measurement Board Components

Parameter	Symbol	Value
DC Capacitor	C_{DC}	9.4 μF
Load Resistor	R_{Load}	2000 Ω
Voltage	V_{DD}	800 V
Ambient Temperature Range	T_{Amb}	25-175°C
Top Gate Resistance Range	R_{G_Top}	10-100 Ω
Bottom Gate Resistance Range	R_{G_Bot}	10-330 Ω

to 175 °C. Table 1 indicates the key parameters for the testing board and experiment conditions.

IV. MEASUREMENT AND ANALYSIS

A. IMPACT OF BOTTOM GATE RESISTANCE

Fig. 7 show the transient waveform of shoot-through current on each DUT for a range of R_{G_Bot} with ambient temperature at 25 °C and R_{G_Top} at 47 Ω. R_{G_Top} 47 Ω is also selected for all the other measurement results in the paper as a representative case since the change of R_{G_Top} will not alter the trend showing in the graphs. Fig. 8 compares the extracted peak value of shoot-through current. It can be seen that as R_{G_Bot} increases, SiC symmetrical double-trench MOSFET experiences the most significant rise in shoot-through current followed by SiC asymmetric double-trench MOSFET and the least change in SiC planar MOSFET. The general increasing trend of shoot-through current with R_{G_Bot} is due to the induced gate voltage raised by the displacement current via C_{GD} coupled with the increased overall impedance of R_{G_Bot} in parallel with C_{GS}. High induced gate voltage allows the

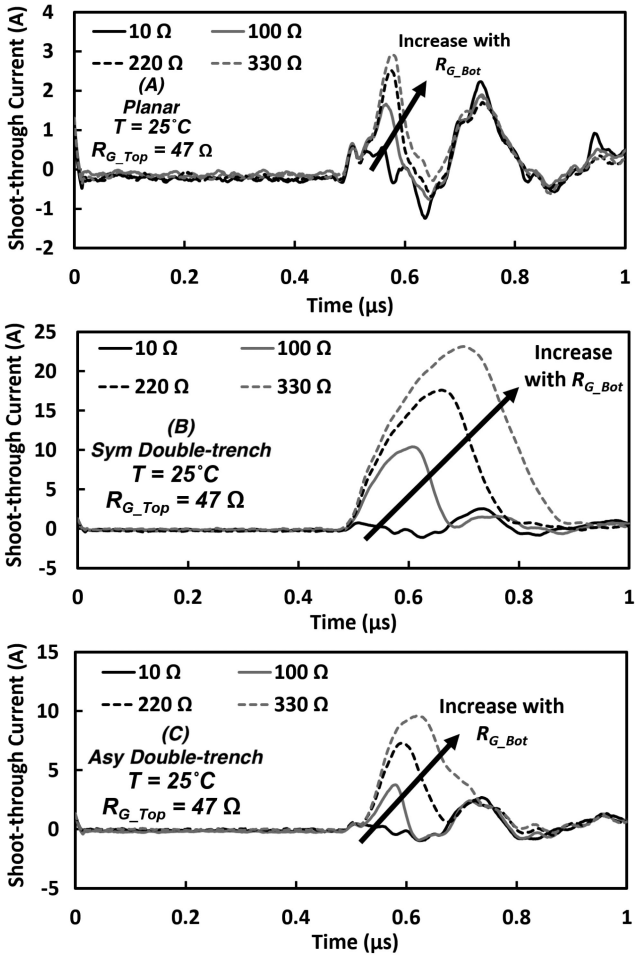

FIG. 7. Transient shoot-through current waveform for a range of R_{G_Bot} for DUTs.

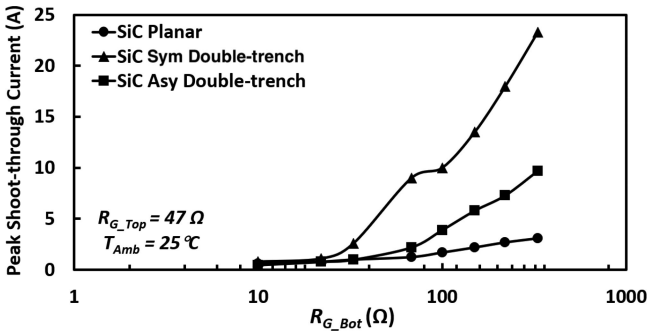

FIG. 8. Peak shoot-through current for a range of R_{G_Bot} for DUTs.

channel to conduct more current with DUT operating in saturation region. The variation level of the induced gate voltage is affected by C_{GS} of device. The value of C_{ISS} and C_{GD} measured at V_{DS} = 0 V, 1 MHz is shown in Table 2 for the three DUTs. Such high parasitic capacitance is an intrinsic feature for planar MOSFET because its low channel density in planar structure [18] requires larger chip size to realize

TABLE 2 Measured C_{GD} and C_{ISS} for DUTs At V_{DS} = 0 V, 1 MHz

DUT	C_{GD} (pF)	C_{ISS} (pF)
SiC Planar	1324	2355
SiC Sym Double-trench	344	711
SiC Asy Double-trench	121	622

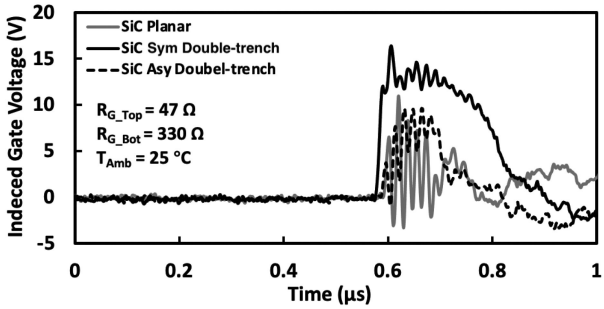

FIG. 9. Induced gate voltage transient waveform for three DUTs.

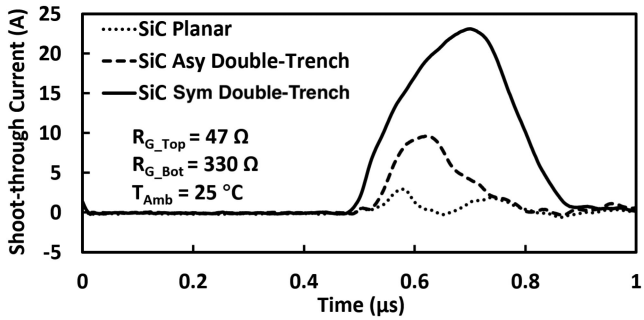

FIG. 10. Shoot-through current transient waveform for three DUTs.

similar current rating as double-trench MOSFET [24]. With larger C_{GS}, the overall impedance of R_{G_Bot} in parallel with C_{GS} would be more dominated by C_{GS} since it behaves as a path of lower impedance at high frequency in such parallel circuit. Therefore, the high C_{GS} grants planar MOSFET low sensitivity of induced gate voltage to R_{G_Bot} whereas low C_{GS} gives two double-trench MOSFETs higher sensitivity and thereby shoot-through current. Since oscillations occur on the measurement of gate voltage, peak induced gate voltage is not representative enough for characterization. Transient gate voltage waveform for three DUTs are plotted in Fig. 9 for a specific case with R_{G_Top} and R_{G_Bot} equal to 47 Ω and 330 Ω respectively under 25 °C, R_{G_Bot} is intentionally chosen to be large to amplify the difference of DUT characteristic. The impact of the induced gate voltage on shoot-though current on the three device technologies is clear in Fig. 10. It shows that the induced gate voltage is the highest for SiC symmetrical double-trench followed by asymmetrical double-trench MOSFET and planar being the smallest despite more serious oscillations showing up on planar MOSFET. The reason for the lower induced gate voltage of asymmetrical double-trench

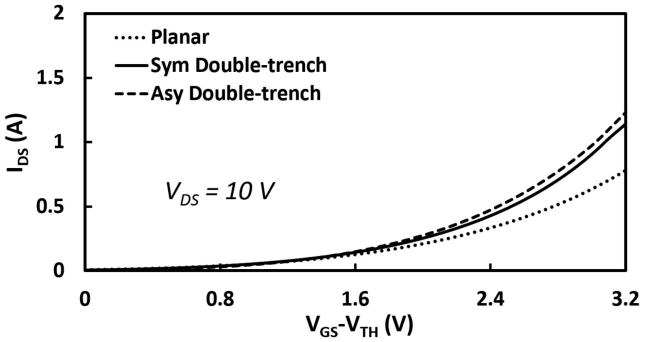

FIG. 11. Transfer characteristics for three DUTs.

MOSFET compared with symmetrical double-trench one can be attributed to the its structure which intrinsically features low C_{GD} [19].

To understand the dependence of peak shoot-through current on R_{G_Bot}, another parameter besides the induced gate voltage must be considered which is the transconductance g_{fs}, expressed as:

$$g_{fs} = \beta * (V_{GS} - V_{TH}) \tag{10}$$

where β is the gain factor of the transconductance and is given by:

$$\beta = \frac{Z_{CH}\mu_n C_{OX}}{L_{CH}} \tag{11}$$

where Z_{CH} and L_{CH} are channel width and length respectively, μ_n is channel carrier mobility and C_{OX} is specific capacitance of gate oxide.

The transfer characteristic of three DUTs are measured shown in Fig. 11 under V_{DS} = 10 V. The slope for the two double-trench MOSFETs are almost the same but more gradual in the case of the Planar MOSFET, hence less contribution to the shoot-through current. Since the sloping is strictly related to device dimensions according to (11), the major factor that leads to this difference is not clear unless the design details could be unveiled.

Another observation is that such high shoot-through current on SiC symmetrical double-trench MOSFET has non-negligible impact in the voltage transition speed initiated by the top switching drive because the channel diverts the current from C_{GD} of DUT, so there is less current to charge up C_{GD}. The transient V_{DS} waveform for SiC symmetrical double-trench MOSFET at different values of R_{G_Bot}, as shown in Fig. 12, exhibits a significant slow down of V_{DS} rise which acts as a negative feedback mechanism to suppress the shoot-through. The V_{DS} transition speed is calculated for three DUTs and plotted against R_{G_Bot} in Fig. 13. The decrease on V_{DS} switching rate is the most noticeable on SiC symmetrical double trench MOSFET and the least for SiC planar MOSFET which corresponds to the most shoot-through and least shoot-through current respectively.

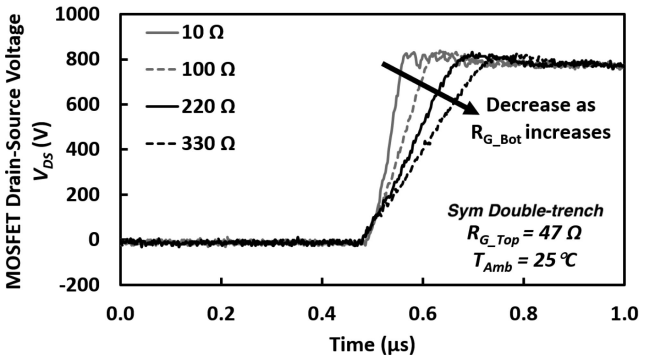

FIG. 12. Transient V_{DS} waveform of SiC double-trench MOSFET for a range of R_{G_Bot}.

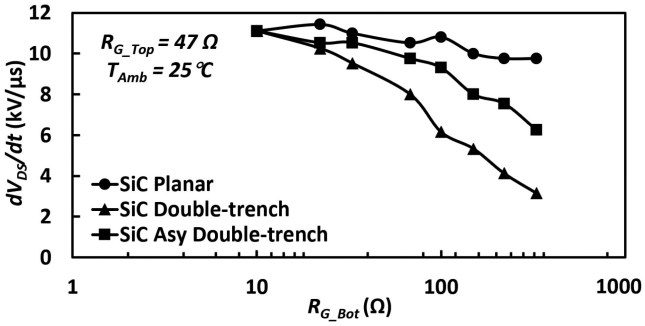

FIG. 13. Calculated V_{DS} switching rate against R_{G_Bot} for three DUTs.

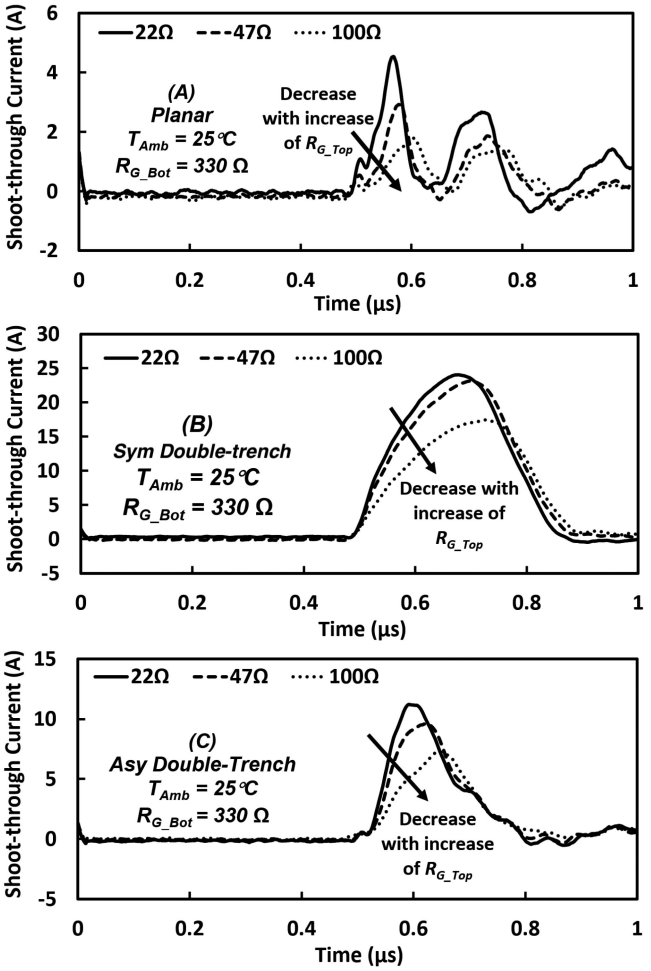

FIG. 14. Transient shoot-through current for a range of R_{G_Top} for DUTs.

B. IMPACT OF SWITCHING RATE

Fig. 14 shows the shoot-through current of each DUT under different switching rate by replacing R_{G_Top} at 25 °C. In this case, R_{G_Bot} is selected to be 330 Ω so that there is significant shoot-through to exaggerate the impact of R_{G_Top}. The shoot-through current experiences decrease as R_{G_Top} increases, because low switching rate generates less displacement current through C_{GD} of DUT for a reduced induced gate voltage. As already indicated in Figs. 12 and 13, the actual dV_{DS}/dt on DUT is not only controlled by R_{G_Top} but also affected by DUT itself. The peak shoot-through current on each DUT is normalized and given on Fig. 15 against R_{G_Top} at both case R_{G_Bot} equal to 330 Ω and 150 Ω. It can be seen that SiC symmetrical double-trench MOSFET is the one that has the lowest sensitivity to R_{G_Top}, though this dependence is enhanced if its R_{G_Bot} is reduced as in Fig. 15(b). This is because that the highest shoot-through current on SiC symmetrical double-trench MOSFET minimizes change of dV_{DS}/dt on it at increasing R_{G_Top}. Due to fairly low shoot-through current, SiC asymmetrical double-trench MOSFET and planar MOSFET maintains good sensitivity to R_{G_Top} in terms of peak shoot-through current.

The measured peak shoot-through current in regard to different R_{G_Top} and R_{G_Bot} for three DUTs are summarized in Fig. 16.

C. IMPACT OF TEMPERATURE

The peak values are extracted and plotted in Fig. 17. When R_{G_Bot} is 330 Ω, three devices shows three different trend regarding to the temperature increase in peak shoot-through current. SiC planar MOSFET has increased shoot-through with temperature while it is opposite for SiC symmetrical double-trench MOSFET, and SiC asymmetrical double-trench MOSFET is nearly constant at all temperature. Since during shoot-through, MOSFET is under saturation region operation. Assumed that the displacement current via parasitic capacitance is negligible, the shoot-through current is subject to (3). By expanding g_{fs} with (11), it yields:

$$I_{Sat} = \frac{Z_{CH}\mu_n C_{OX}}{L_{CH}}(V_{GS} - V_{TH})^2 \tag{12}$$

The parameters that have temperature-dependence are the channel mobility μ_n and the threshold voltage V_{TH}. It is commonly known that high temperature raises of intrinsic carrier density thus reduces V_{TH} [25], [26]. Hence, the change of V_{TH} would enhance the shoot-through at high temperature. V_{TH} for each DUT is measured at conditions $V_{GS} = V_{DS}$, $I_{DS} = 4\ mA$

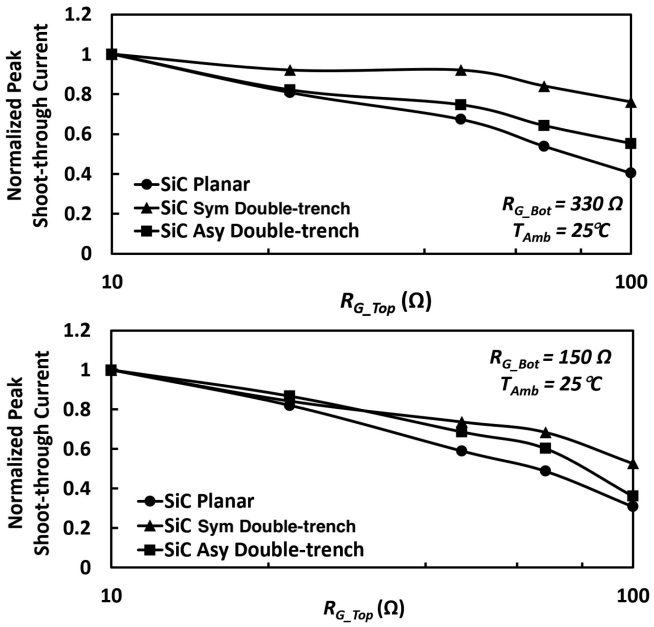

FIG. 15. Normalized peak shoot-through current to R_{G_Top} for each DUT with 330 Ω and 150 Ω R_{G_Bot}.

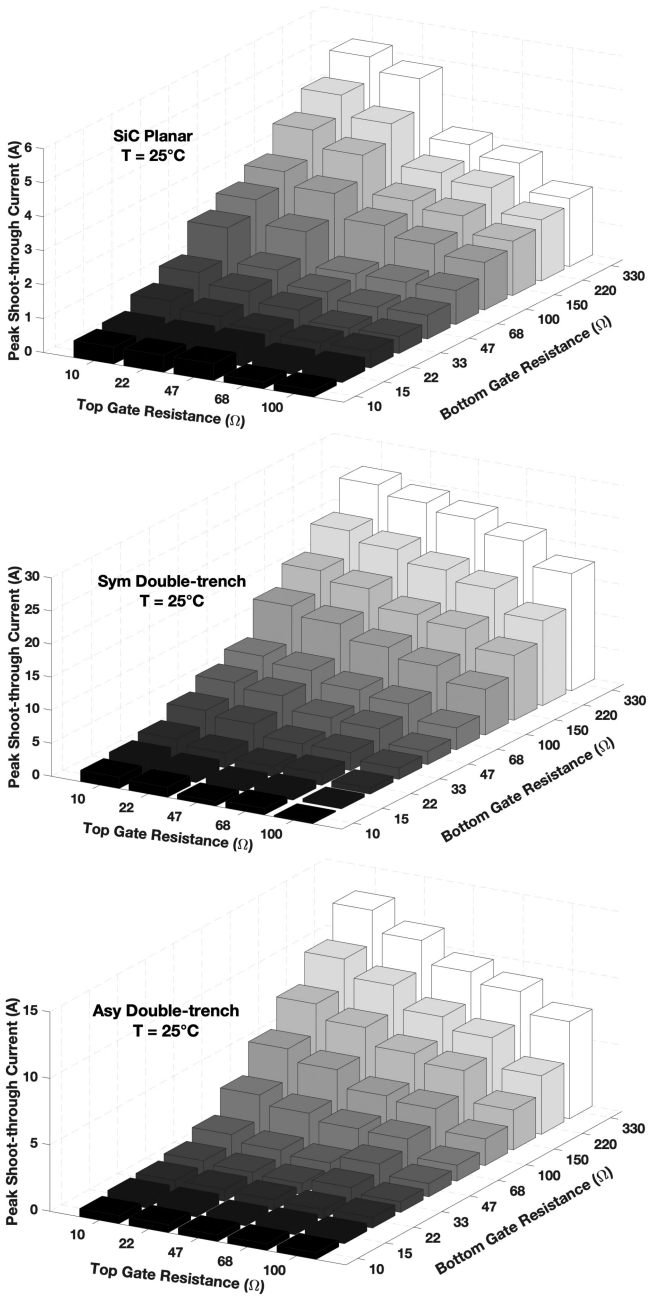

FIG. 16. Peak shoot-through current for three DUTs for a range of R_{G_Top} and R_{G_Bot} under 25 °C.

and shown in Fig. 18 to confirm this statement. Although the planar SiC MOSFET has the lowest V_{TH} for more likelihood of shoot-through current, but this is over-compensated by its particularly large C_{GS}. There is around 1 V drop in V_{TH} for the three DUTs across the full temperature span. However, the μ_n acts adversely on shoot-through since it decreases due to more pronounced scattering at high temperature [27]. Therefore, It can be revealed that, with R_{G_Bot} equal to 330 Ω, μ_n acts as a more dominated factor to shoot-through in SiC double-trench MOSFET whereas it is V_{TH} in SiC planar MOSFET, these two mechanisms almost balance each other out in SiC asymmetric double-trench MOSFET. According to (12), the higher the V_{GS} is, the less impact the V_{TH} has on the term $(V_{GS} - V_{TH})$. As discussed previously, the large value of C_{GS} in SiC planar MOSFET suppressed the induced gate voltage, which makes it more susceptible to the temperature dependence of V_{TH}. The low C_{GS} in SiC symmetrical double-trench MOSFET and asymmetrical double trench MOSFET has the impact of μ_n more outstanding so that it could counterbalance V_{TH} or even outweigh V_{TH}. It also needs to be mentioned that the mobility is also influenced by V_{GS} and an empirical equation to describe such relationship is given by [28] as:

$$\mu_n = \frac{\mu_0}{1 + \theta_1(V_{GS} - V_{TH}) + \theta_2(V_{GS} - V_{TH})^2} \tag{13}$$

where μ_0 is the low-field mobility, θ_1 and θ_2 are coefficient responsible for the first order and second order effect of V_{GS}.

Since the higher induced gate voltage is observed on the symmetrical and asymmetrical double-trench MOSFET, the mobility would experience more degradation according to (13). With R_{G_Bot} replaced by 10 Ω from 330 Ω, the induced gate voltage at crosstalk is effectively reduced, in this case, V_{TH} becomes the most determining factor for all DUTs. Therefore, all DUTs are exhibiting an increasing shoot-through in regard to temperature increase as shown in Fig. 17.

The measured peak shoot-through current in regard to different R_{G_Bot} and temperature for three DUTs are summarized in Fig. 19. The value of 47 Ω is selected as a typical value to demonstrate the trend clearly with minimal oscillations. The trends observed for other R_{G_Bot} demonstrate similar characteristics, albeit with different values. It can be seen clearly

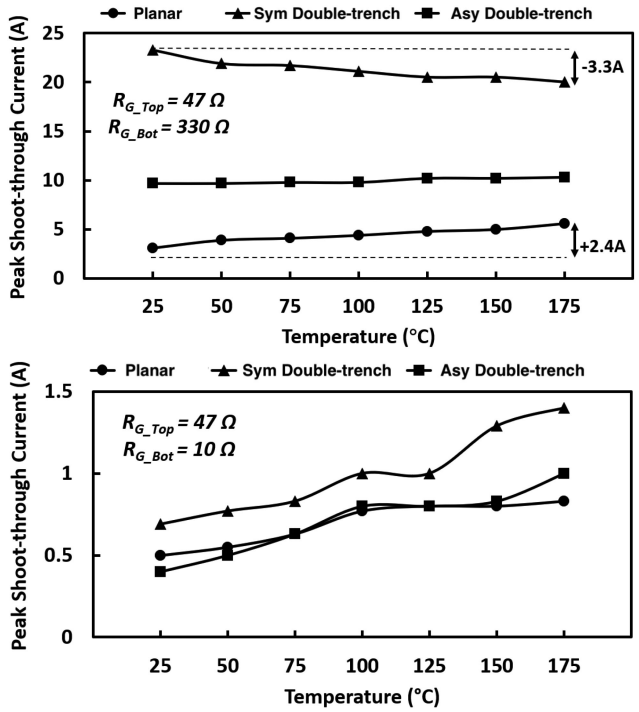

FIG. 17. Peak shoot-through current to R_{G_Top} for each DUT with 330 Ω and 10 Ω R_{G_Bot}.

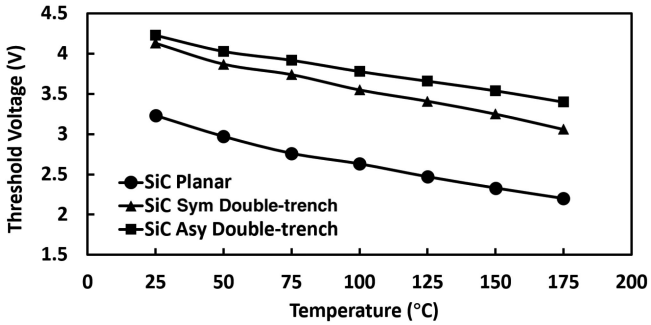

FIG. 18. Threshold voltage against temperature for DUTs measured at $V_{GS} = V_{DS}$, $I_{DS} = 4$ *mA*.

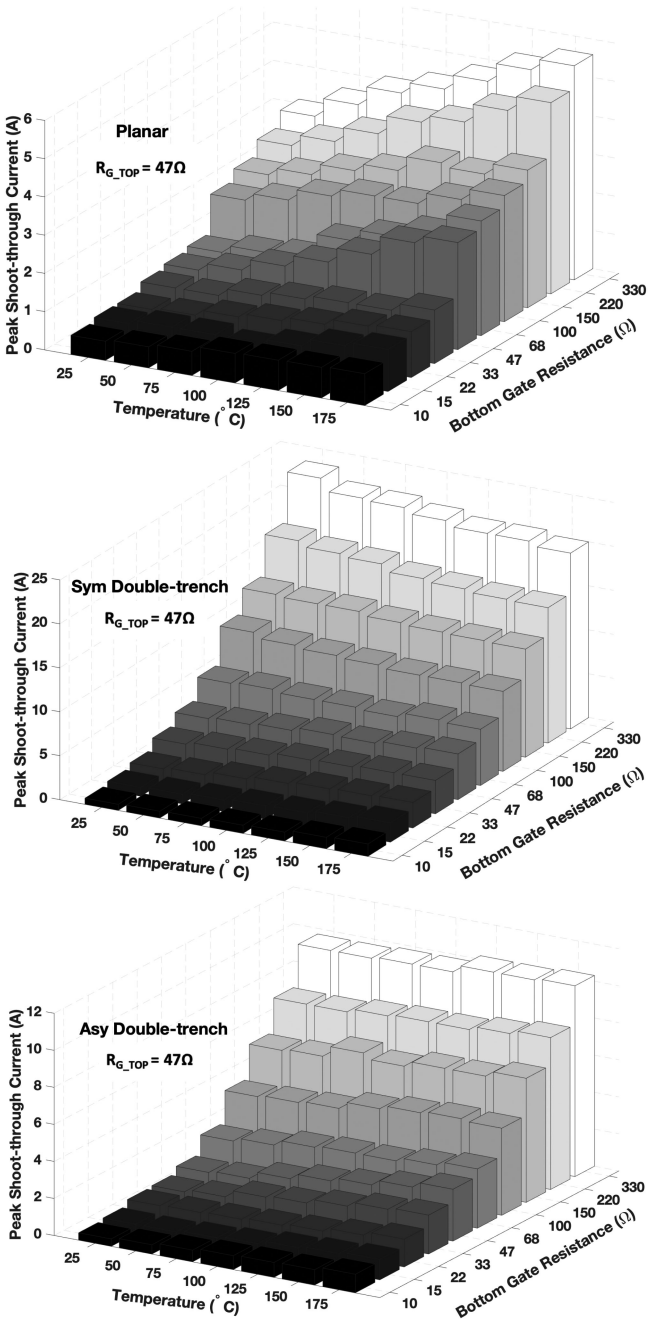

FIG. 19. Peak shoot-through current for three DUTs at different value of R_{G_Bot} and temperature with $R_{G\_Top} = 47$ Ω.

that in diagram of SiC symmetrical double-trench MOSFET, when the bottom gate resistance is around 68 Ω to 150 Ω, the peak shoot-through current nearly levels out which indicates a balance achieved between mobility and threshold voltage.

D. IMPACT OF INDUCTIVE LOAD CURRENT

In common industrial application, devices are working with non-zero load current, therefore, the impact of different load current level is a key point which would reflect the crosstalk performance in real situation. The measurements in this section are performed by replacing the resistive load in Fig. 6 with an inductive load, as an inverted double-pulse test board where the switching transistor is on top and the load inductor is in parallel to bottom device. This inductive load enables maintaining the load current representative of typical loads in industrial applications. At the rising edge of the first pulse, the crosstalk happens with no load current but at the rising edge of the second pulse, crosstalk happens with the presence of load current determined by the first pulse length.

The measurement results of peak shoot-through current are plot on Fig. 20 from no load current to 12 A load current with R_{G_Top} and R_{G_Bot} equal to 47 Ω and 330 Ω respectively. The recorded value at no load current is slightly different from those on the previous figures such as Fig. 8 because the load has different parasitic capacitance. Fig. 20 reveals that

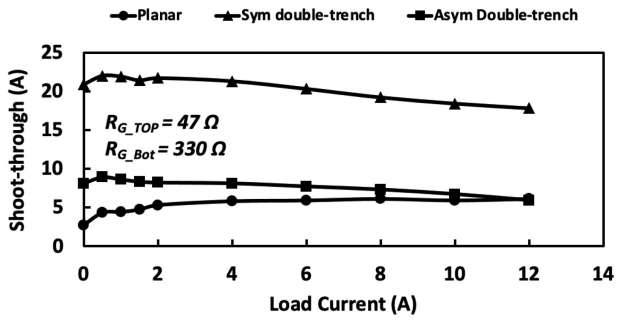

FIG. 20. Peak shoot-through current to load current level for three DUTs.

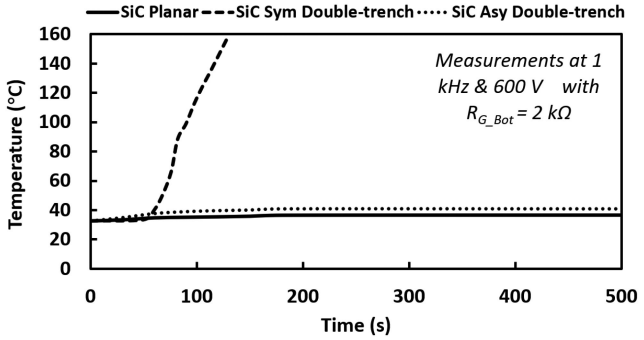

FIG. 21. Temperature rise under continuous crosstalk for DUTs.

symmetrical and asymmetrical double-trench MOSFET has an initial rise immediately non-zero load current appears in the circuit and followed by a continuous drop with the further increase of load current. As for the SiC planar MOSFET, the initial rise of peak shoot-through current lasts much longer until 4 A and then generally hold constant for the subsequent load current increase. It needs to be considered that before the crosstalk with load current happens, the DUT is conducting current via its body diode which is essentially a PiN diode, the conductivity modulation would store extra charge within the body diode [29] and its reverse recovery could also be responsible for the initial rise of measured current compared with the case with no load current. However, this possibility has been ruled out by extracting the reverse recovery current with the gate of DUT being short-circuited to source to prevent its unwanted turn-ON. The results show negligible reverse recovery current on DUTs' body diode which matches those reported in [30], [31] as a result of implementing SiC technology.

It clearly indicate two competing mechanism from load current increase. The load current would impact the crosstalk shoot-through via changing the drain-source voltage transition rate over DUT. The first mechanism that leads to the increase of shoot-through current has been explained as the current overshoot driven by switching of the top device [11]. At current commutation during switching, the additional overshoot current would flow through the C_{DS} of DUT thus accelerate the drain-source voltage transition rate over DUT. It has also been revealed that such current overshoot increases with the load current level [11]. The other mechanism for the decrease of peak shoot-through current is the slow down of V_{DS} transition speed by increasing the Miller plateau on the top switching device and the equation is given by:

$$\frac{dV_{DS}}{dt} = C_{GD}\frac{V_{GD+} - V_P}{R_G} \tag{14}$$

where V_{GD+} is the positive output voltage from gate driver and V_P is the Miller plateau.

When the load current increases from 0 A to 0.5 A, all three DUTs experience a rise on the peak shoot-through current which suggests that the current overshoot initiated by switching is playing the major role. However, in the further increase of load current, the impact of current overshoot only appears to be significant on planar MOSFET. The reason is that the current overshoot is also dependent on the switching rate, faster switching causes more overshoot. By referring to Fig. 13, the drain-source voltage transition rate on symmetrical and asymmetrical double-trench MOSFET is much slower than planar as a result of more shoot-through current. Therefore, on the two double-trench devices, they show decreasing peak shoot-through current because the raised Miller plateau on top switching device becomes dominated.

E. CONTINUOUS SWITCHING

One concern for crosstalk on MOSFET is the heat generated while operating in such short-circuit circumstance, so that the device would soon work above the allowed temperature. To analyse the performance of different device structures in applications, the devices have intentionally been subject to significant electrothermal stress, and the characteristics of the crosstalk under these conditions are observed. Three DUTs are driven continuously at 1 kHz, supply voltage equal to 600 V, room temperature and the temperature rise is recorded using FLIR-63900 thermal camera. The gate resistance is chosen to be 2 $k\Omega$ to amplify the impact of different device characteristics. The results is plotted on Fig. 21 and thermal image corresponding to the highest captured temperature is shown in Fig. 22. It shows that compared with soaring to nearly 160 °C within 2 minute for symmetrical double-trench MOSFET, planar and asymmetrical double-trench MOSFET, after a small rise initially, maintain stable at low temperature though asymmetrical double-trench MOSFET is still higher than planar. Typical options to suppress crosstalk are by the use of bipolar gate drivers to offset the induced voltage by negative gate voltage, active Miller clamp on unipolar gate drivers, separate gate resistance paths for transistor turn-ON/turn-OFF transients, addition of gate-source capacitance or use of snubber capacitance to prevent excessive dV/dt by DC link overshoots [7], [12], [32].

F. IMPACT OF BTI ON SHOOT-THROUGH CURRENT

In [33], it has shown that the crosstalk shoot-through current could be used as a parameter to characterize devices subject

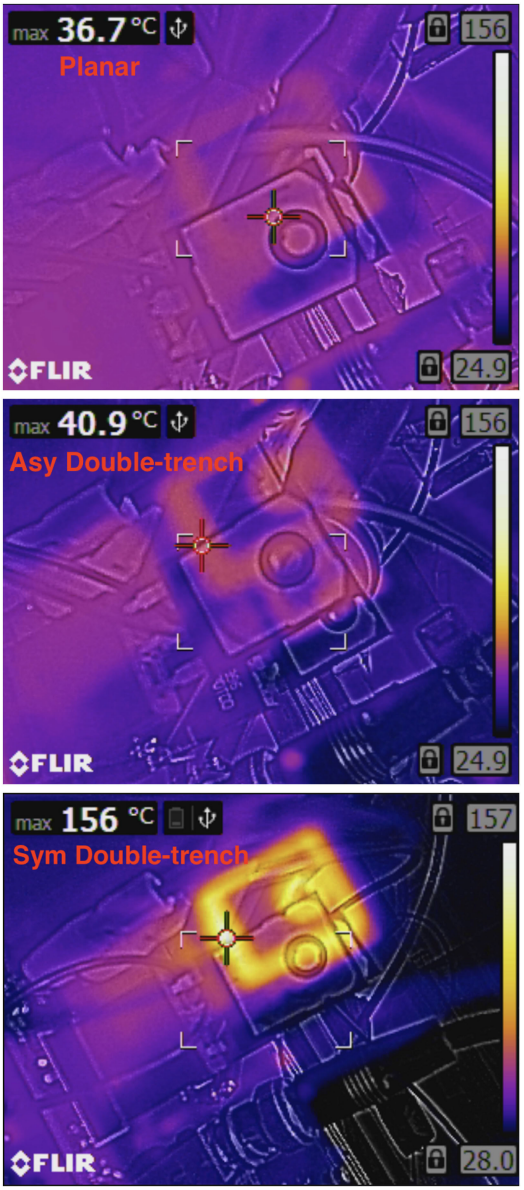

FIG. 22. Maximum temperature recorded under continuous crosstalk in DUTs when switched with $R_{G\_Bot} = 2\ k\Omega$, indicating a temperature rise of almost 37 °C and 41 °C in the Planar and Asymmetrical Double-trench MOSFETs while the temperature rise in the Symmetrical double-trench MOSFET is as high as 156 °C under identical test conditions.

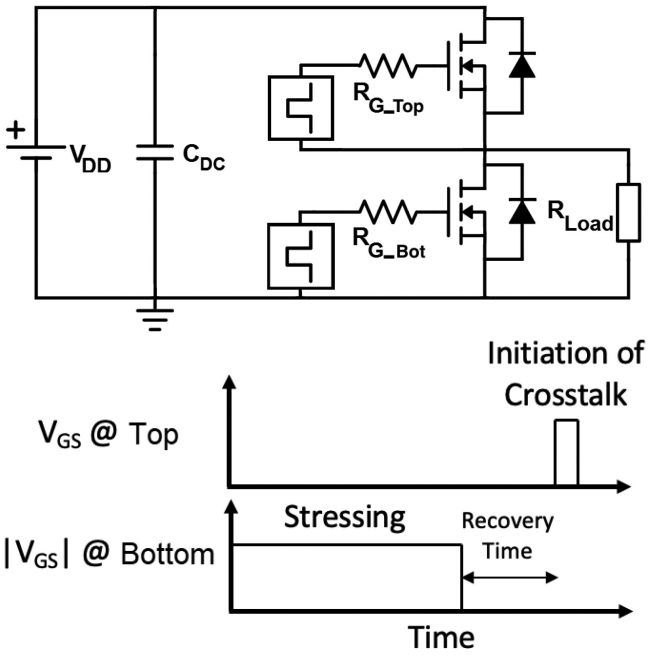

FIG. 23. Test circuit and procedure for experiment of crosstalk after BTI.

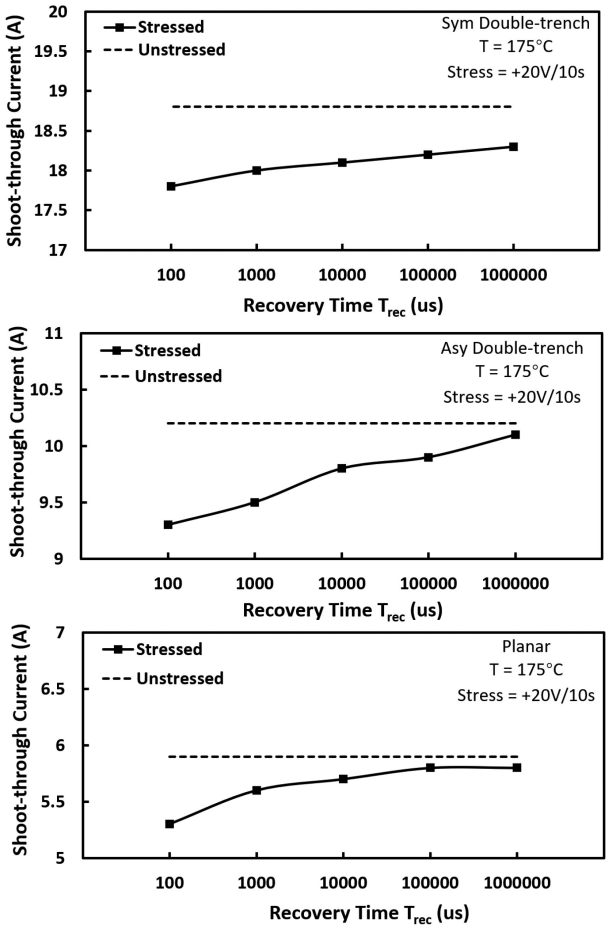

FIG. 24. Post-PBTI shoot-through current with +20 V for 10 sec at 175 °C.

to Bias Temperature Instability (BTI). The experiment is also performed to reveal the impact of BTI on three selected DUTs with the testing circuit and experiment procedure described in Fig. 23. The combination of top and bot gate resistance (R_{G_Top} and R_{G_Bot}) are 47 Ω and 330 Ω, respectively. It is necessary to intentionally have large R_{G_Bot} or the impact of BTI may not be revealed [33]. In this experiment, the DUT at bottom is stressed before the turn-ON of top device to initiate crosstalk. The stressing condition is chosen to be ±20 V for 10 sec at 175 °C which represents both positive and negative BTI (PBTI and NBTI). Between the removal of stress and

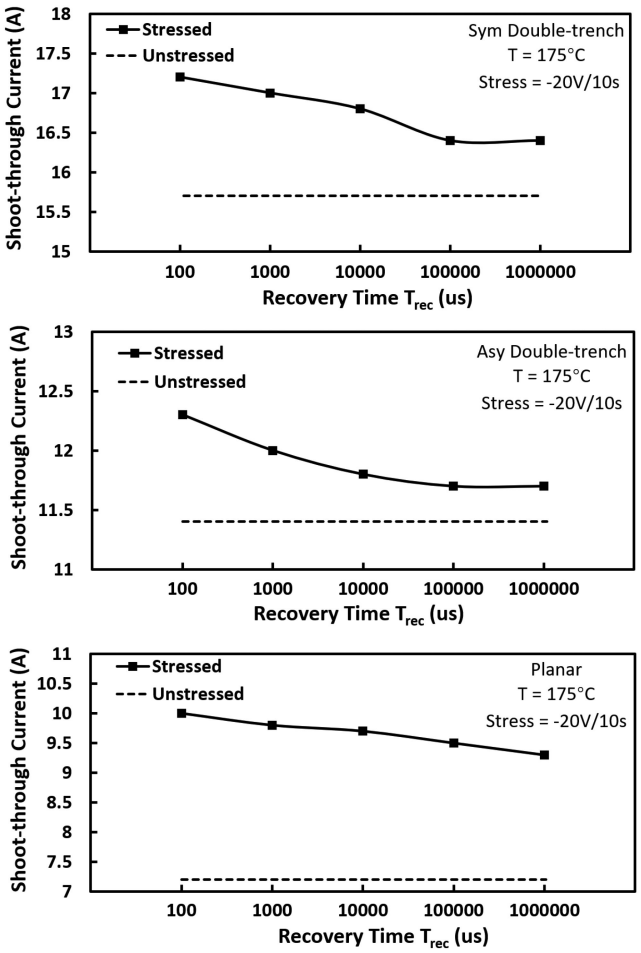

FIG. 25. Post-NBTI shoot-through current with −20 V for 10 sec at 175 °C.

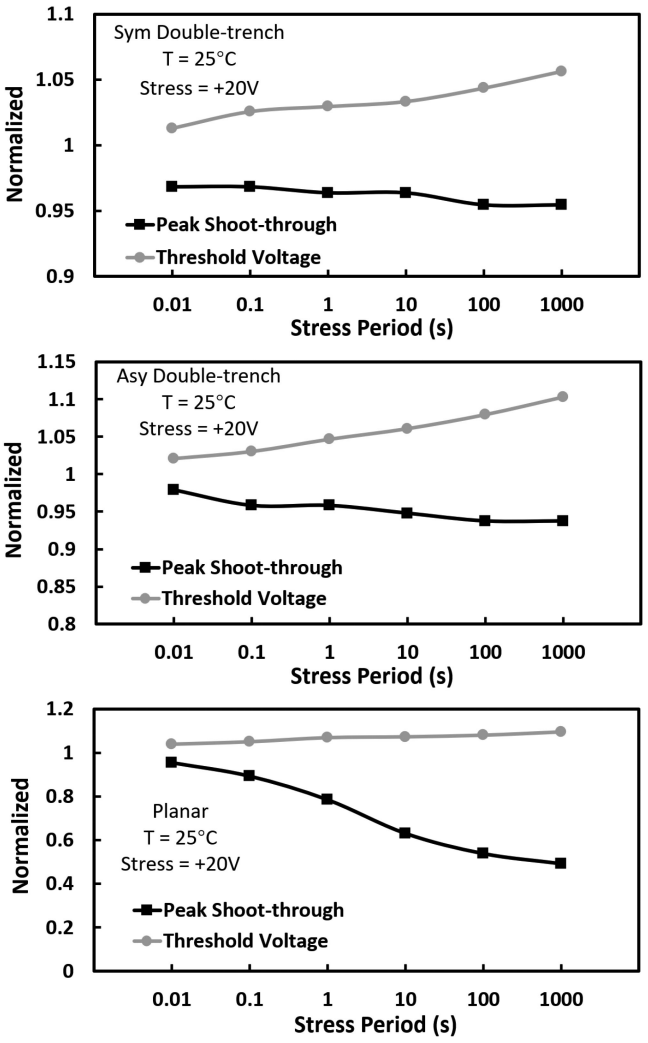

FIG. 26. Normalized threshold and peak shoot-through current for three DUTs under PBTI with +20 V at increase of stressing period at 25 °C with crosstalk initiated with R_{G_Top} of 47 Ω and R_{G_Bot} of 330 Ω.

the start of crosstalk, there is a certain time interval during which the DUT may experience recovery, the relationship of BTI-induced shoot-through current to the recovery time is investigated and shown in Figs. 24 and 25.

In Fig. 25, the dashed line represents the peak shoot-through current in unstressed case. Different gate driver is used to generate two polarities of stress, that is, the gate loop parasitics is different thus is responsible for the different unstressed peak shoot-through in PBTI and NBTI experiment. As can be seen, the peak shoot-through current decreases in PBTI while increases in NBTI. This corresponds to the behaviour of threshold voltage drift under each stressing polarity since electrons tunnel out of oxide to form positively charged oxide traps in NBTI and tunnel back to neutralize positively charged traps in PBTI, resulting in negative and positive threshold voltage drift respectively [34]. As the recovery time increases, the threshold voltage restores and the value of post-BTI shoot-through current is approaching the unstressed case. By comparing the results from PBTI and NBTI, there is generally more residual drift of shoot-through at 1,000,000 μs recovery time because SiC devices could not withstand too negative gate voltage with −20 V stressing far exceeding the recommended operating condition. In terms of the percentage change of shoot-through current, it is the most significant in the planar DUT. One potential reason is that it has smaller threshold voltage as demonstrated in Fig. 18, so it is more likely to have higher percentage change of threshold voltage. It should be mentioned that the variation of shoot-through current after gate stressing does not fully reflect the behaviour of threshold voltage drift (i.e. trapping and de-trapping of oxide traps), because the carrier mobility is also affected during the stressing [35]. The carrier mobility degrades in both PBTI [36] and NBTI [37], hence, there is more threshold voltage drift occurs behind the measurement of shoot-through in NBTI and less in PBTI.

Besides the variation of recovery time, experiment of peak shoot-through in regard to stress time has also been measured as well as the threshold voltage drift which is done by using source measure unit B2902 A. The threshold is defined as the gate-source voltage when the $I_{DS} = 1\ mA$ at

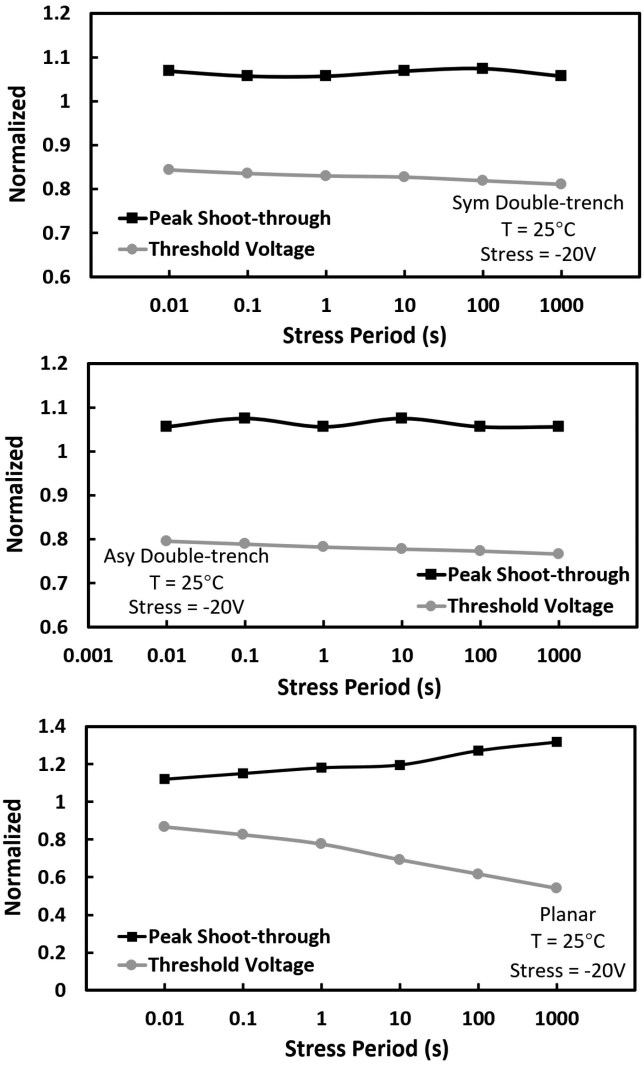

FIG. 27. Normalized threshold and peak shoot-through current for three DUTs under NBTI with −20 V at increase of stressing period at 25 °C with crosstalk initiated with R_{G_Top} of 47 Ω and R_{G_Bot} of 330 Ω.

$V_{DS} = 0.5\ V$. The normalized results of peak shoot-through and threshold are shown in Figs. 26 and 27 at conditions of 25 °C, $t_{Rec} = 0.5\ s$ and subject to ±20 V with 1 representing unstressed case. In the PBTI case, although steady threshold drift has been observed as the stressing time increases for three DUTs, the corresponding change of peak-shoot-through on planar MOSFET is highly massive while the other two DUTs are milder. By referring to the Fig. 9 and (12), this is due to the fact that planar MOSFET has low induced gate voltage at crosstalk so that the shoot-through current will be sensitive to the threshold change. It is noticed that for symmetrical double-trench MOSFET, there is a significant lowering of peak shoot-through upon 0.01 sec stress applied compared with the unstressed one which could be attributed to mobility degradation. In the NBTI case, the threshold voltage of the planar MOSFET shows massive difference from the other two double-trench MOSFET, where it has more steady change with the increase of stressing time while the other two double-trench MOSFET have a much mild slope despite a huge drift upon the 0.01 sec stressing applied. This indicates that the most of traps in the two double-trench DUTs have low emission time constant. As for the peak shoot-through current, the planar MOSFET still exhibits clear correlation while the change in peak shoot-through relative to gate threshold voltage drift for the two double-trench MOSFETs with increase of stress period is minimal.

V. CONCLUSION

The crosstalk characteristics for planar and symmetrical and asymmetrical double-trench SiC power MOSFETs has been modeled and experimentally evaluated. Higher spurious gate voltage is induced at crosstalk for the two double-trench structure MOSFETs and thereby leading to higher shoot-through current compared with the planar MOSFET. This difference in the shoot-through current also impacts the drain-source voltage transition rate which also leads to different characteristics of peak shoot-through current when load current is increased. Different levels of induced spurious gate voltage as a result of different gate-source capacitance on the three devices alters the dominant mechanism in response to temperature variation so that decreasing shoot-through current is observed on symmetrical double-trench, nearly stable on asymmetrical double-trench and an increase on the planar MOSFET. As a consequence of the large shoot-through current on symmetrical double-trench MOSFET, it undergoes rapid temperature rise under continuous operation. Furthermore, minimization of shoot-through by replacing the large top gate resistance for symmetrical double-trench MOSFET is not as effective as that on the planar MOSFET and asymmetrical double-trench MOSFET, especially in the case where a high gate resistance is connected on the bottom side device. In the post-BTI crosstalk experiment, it shows that peak shoot-through characteristics is altered after gate stressing but will recover faster in PBTI than NBTI and for symmetrical and asymmetrical double-trench MOSFET, the peak shoot-through does not response to threshold voltage drift as strongly as planar MOSFET in terms of stress period.

ACKNOWLEDGMENT

All underlying data are provided in full within this article.

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