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Design Optimization Methodology for Planar Transformers for More Electric Aircraft

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This paper is an extension of a conference paper that was presented in ITEC in 2020. The paper title is "Transformer Design Optimization for Power Electronic Converters in Electric Aircraft"

ABSTRACT Isolated DC-DC converters are considered the building blocks of modern aircraft electrical power networks. The high-frequency transformer utilized in such converters is the major contributor to the size and weight besides the thermal management system. In this paper, an optimization design methodology aims to minimize the transformer core size and improve the converter performance through optimized winding configurations. The transformer core selection is based on optimizing the maximum flux density while considering different magnetic materials and number of cores in parallel. The transformer core is selected for an interleaved winding configuration and to keep the windings current density below a certain limit. The trade-offs between the converter efficiency and core weight in selecting an optimum switching frequency are presented. Multi-layer minimum gradient (MLMG) winding configurations are proposed to eliminate the high-frequency oscillations (HFO) caused by the transformer parasitics. The proposed configurations resulted in a reduction of the intra-winding capacitance by 15 times with 20% improvement in the transformer volume as compared to a similar conventional double-layers spiral configurations. Numerical simulations are performed in ANSYS Maxwell to validate the proposed design and the developed analytical models. The effect of the different configurations on the converter performance is verified in the PLECS simulation environment. PLECS simulation results are validated experimentally for the conventional and proposed configurations highlighting the improvements on the performance of the converter.

INDEX TERMS DC/DC converter, more electric aircraft, planar transformer, core selection, winding configurations, finite element analysis.

I. INTRODUCTION

As a step towards more efficient and sustainable aircraft, electric solutions have started to emerge replacing the traditional pneumatic, hydraulic, and mechanical systems in more electric aircraft (MEA) [1]. Efforts have being made in the design of compact, lightweight distribution systems while enhancing efficiency and increasing power handling capabilities. DC/DC converters form one of the main power electronic components in MEA. Fig. 1 shows the high voltage direct current (HVDC) distribution network for the MEA supplied through two main engines and an auxiliary power unit (APU) and having solid state power controllers (SSPC) between the different buses for protection. In the aircraft, two DC link voltages of +/- 135 V and +/- 270 V can be generated from a 115 V or 230 V AC supply, respectively, through a rectifier unit [2]. The +/- 270 V bus such as that adopted on the Boeing 787 provides the standard 540 V also known as the HVDC link of new electric networks in the aircraft. From the 540 V HVDC voltage, the 28 V DC bus is generated, also known as low voltage direct current bus (LVDC). The LVDC bus supplies the electric loads in avionic systems. As seen from Fig. 1, isolated DC/DC converters are required to connect the high voltage bus to the low-voltage network. In a MEA, these converters are used to step the dc bus voltage down to

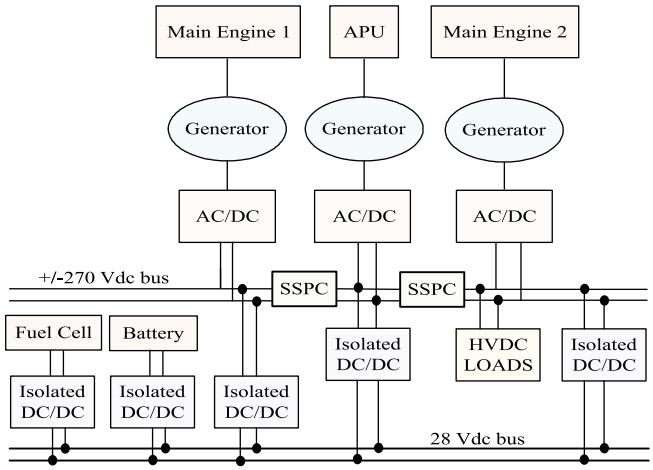


FIGURE 1. MEA electrical distribution system architecture.

the voltage required for other components. In most cases, the voltage range requires high transformer turn-ratio. Therefore, a high-frequency transformer is often used to provide galvanic isolation between the high and low voltage sides. In recent years, design of highly efficient and power dense isolated DC/DC converters have been gaining a lot of attention in industry. One of the most important contributing factors to that efficiency and power density is the transformer design. The transformer must be designed to ensure low weight and volume while optimizing efficiency. A compact and highly efficient transformer is crucial in the design of a power dense high-performance converter. Planar magnetics can be used to increase power density in DC/DC converters. Planar technology allows for power-dense, compact designs and provides homogeneous temperature distribution due to the large surface area of the planar cores [3], [4]. Selecting an optimum switching frequency is the first basic step to optimize the transformer size. A higher switching frequency is associated with reduction of the self-inductance and the core size, resulting in more compact designs [2]. It also increases the switching losses for the power semiconductors in the converter. Core losses also increase at higher frequencies and temperature rise along with proximity and skin effects on the windings. Therefore, the optimization method must be able to choose the optimal frequency while minimizing losses. Based on these factors, an integrated optimization method combining both transformer design and the device switching losses can be beneficial in MEA applications. There have been many attempts in literature for optimizing transformers. One method presented in [5] is based on the integrated leakage inductance of the transformer and its phase shift within a dual active bridge (DAB) converter. One benefit of this strategy is that the core dimensions are optimized and hence are not a limiting factor as discussed in detail in [5]. Other methods consider the switching frequency in the optimization process. The optimal switching frequency is chosen based on the lowest obtained losses with consideration of the transformer volume [6], [7]. Most optimization techniques presented in literature use the area product (AP) method. In this method, the core is selected based on a factor related to the core geometry as well as the power handling capability of the core. Using the AP approach, core loss and thermal limitations dictate the selection of the flux density at a specific frequency. In this paper, an optimization method is developed; this tool considers different materials and cores paralleling with a large planar cores database. The method is based on minimizing the overall transformer losses by selecting an optimum maximum flux density. The algorithm performs a frequency sweep to identify the optimal core material and configuration at each switching frequency point based on the optimization variables. The core optimization results are then integrated with the converter switches loss analysis to obtain the global optimum switching frequency. With the magnetic core geometry defined, the winding design takes place. The winding configurations affect the transformer parasitic elements such as leakage inductance and stray capacitance. The transformer parasitic components directly impacts the converter performance. After selecting an optimum core, the rest of the paper presents a proposed winding configuration to mitigate the issues caused by the transformer parasitic components.

One of the main concerns in MEA DC-DC converters is converter performance and reliability [8]. This is particularly important in high switching speed applications, where the high frequency oscillations (HFO) problem due to the transformer stray capacitance and high dv/dt of the DAB converter is more apparent [9]. The HFO compromises efficiency through increasing AC losses in the transformer at high frequencies. Power density of the converter is impacted due to larger EMI filters required at the input [10]. One method proposed in literature to address the high dv/dt of the DAB is through adding a snubber capacitor in parallel with the power devices [10]. In [11], a detailed analysis in core loss, winding loss, stray capacitance and leakage inductance of planar transformers is investigated with consideration of the trade-offs. As outlined earlier, the DAB converter performance can be enhanced by minimization of the winding capacitance. Most attempts in literature use conventional double layer designs to reduce the transformer winding capacitance and either investigate changing the stacking configuration or the turns arrangement. The double layer approach can compromise the efficiency as well as the power density through increased width of the planar PCB [12]. Different winding configurations were investigated in [12]. The non-overlapping structure has no overlap between turns on both PCB layers, which results in no overlapping area between the layers and hence a significant reduction in the capacitance. The non-overlapping arrangement has high ac losses due to lower transformer utilization factor. Some configurations found in literature, such as the alternating winding configuration, aims to reduce voltage gradient between the layers. [11]–[13] In this paper, a new multilayer minimum gradient (MLMG) configuration is proposed to reduce the transformer stray capacitance while improving the transformer efficiency and power density. The MLMG

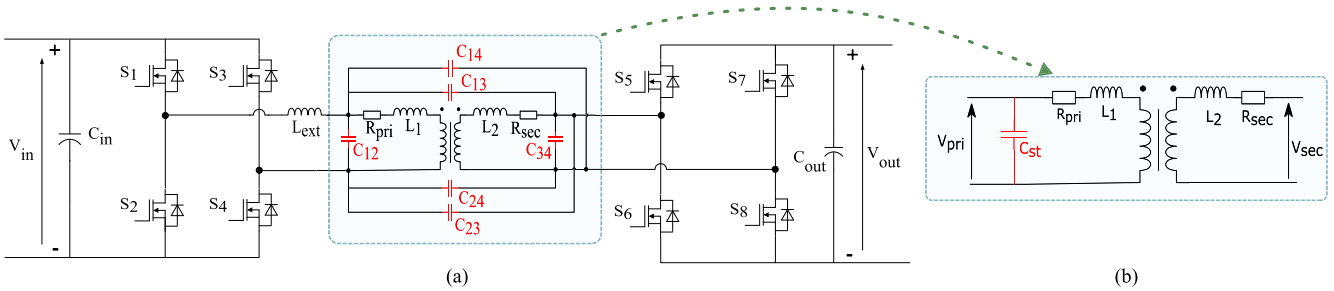


FIGURE 2. **DAB Converter Schematic Considering the Transformer Parasitic Elements: (a) DAB schematic - six capacitors model and (b) Transformer lumped capacitor model.**

configuration aims to reduce the voltage gradient between the layers in the same winding, through a multi-layer arrangement with blind-hole connection between the layers. The capacitance is therefore reduced. With this multi-layer approach, the power density and AC losses are not compromised to reduce the stray capacitance. Simpler assembly is also obtainable with this configuration. The proposed three-layer winding arrangement provides 20% higher power density than a similar double-layer design. This structure has higher power density than the non-overlapping and alternating winding structures proposed in [12] and does not sacrifice efficiency. Converter performance is improved through eliminating HFO caused by the stray capacitance, through reduction of the capacitance.

The paper is presented as follows. Section II presents the developed optimization methodology and the relation between the different tools used in the process. Section III looks at the core optimization procedure and covers the different transformer design methods, and a discussion of the algorithm results. Section IV proposes two MLMG configurations and compares them to the conventional spiral configuration. Finally, Section V validate the PLECS simulation analysis experimentally for both the conventional and proposed configuration.

TABLE 1. **DAB Converter Specifications**

Parameter	Value
Input Voltage	300-540 V (400 V nominal)
Output Voltage	20-28 V
Power	4 kW
Transformer Ratio	22:1
Secondary RMS Current	210 A
Primary RMS Current	10 A

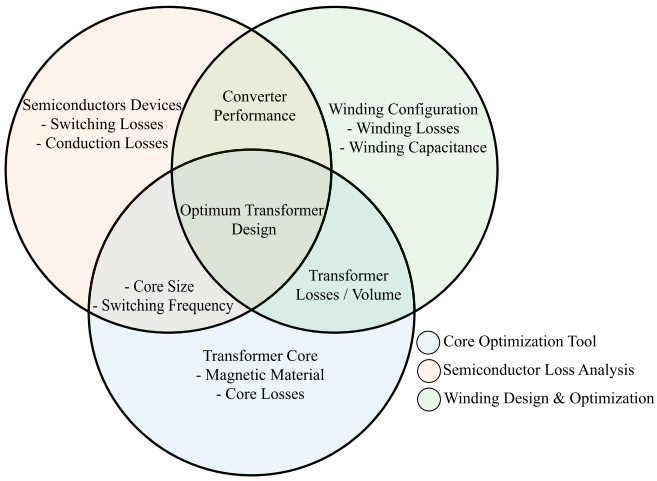


FIGURE 3. **Venn Diagram of the Developed Design Tool.**

II. PROPOSED DESIGN AND OPTIMIZATION PROCEDURE

Isolated DC-DC converters are utilized to supply the low voltage (28Vdc) loads in MEA. The topology that is usually considered in such application, due to good controllability and high efficiency, is the dual active bridge (DAB) converter, discussed in [14]–[16], which will be used as a case study to validate the transformer design tool proposed in this paper. The converter schematic considering the transformer parasitic elements is shown in Fig. 2. An external inductance (L_{ext}) is utilized to control the power flow between the two full bridges connected across the transformer. One of the simplest control strategies utilized to control the DAB converter is phase-shift modulation. Where the voltages across the primary and secondary bridges are phase-shifted with respect to each other. Both the external leakage inductor and the phase shift control the power flow in a bidirectional manner. The DAB transformer specifications are listed in Table 1. In the developed design methodology, both the transformer core and the windings configurations are optimized to minimize the transformer volume and losses and improve the DC-DC converter performance. The procedure is composed of three main tools: an optimization tool to minimize the core weight and volume, a semiconductor loss analysis tool, and an optimization process for the windings configuration.

The Venn diagram, shown in Fig. 3, highlights the overlap between the three tools to reach an optimum transformer design in terms of specific power, volume, efficiency and electromagnetic interference (EMI) performance. The switching frequency and core selection is based on an integration process between the semiconductor loss analysis tool and the core optimization tool. The transformer losses and volume are

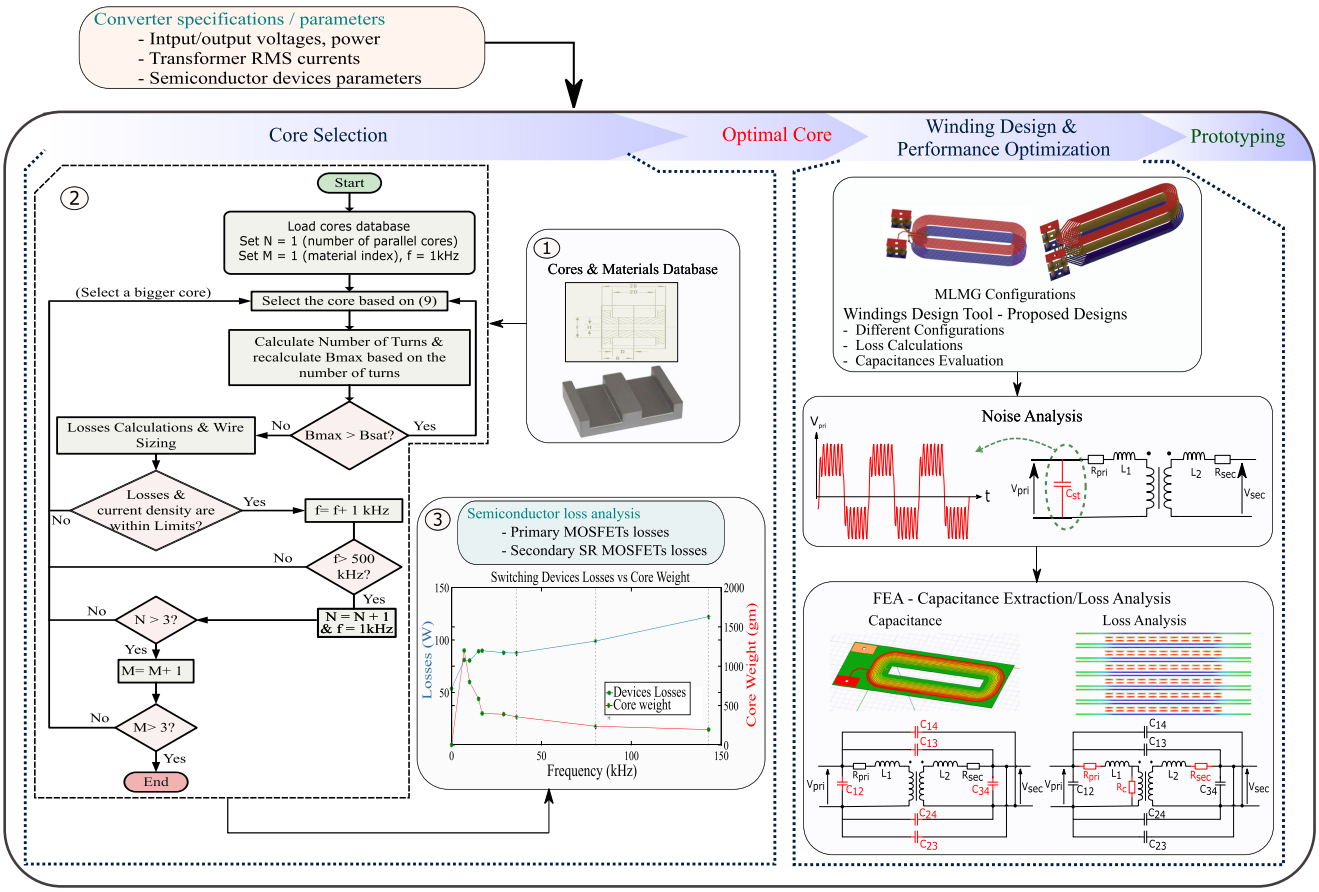


FIGURE 4. Design Methodology Block Diagram.

linked between the optimally selected core and the winding configurations. The converter performance is a function of both the switching frequency and winding configuration.

Fig. 4 illustrates the design flow of the proposed methodology. Based on the converter specifications and semiconductor parameters, the optimal core is selected through the integration process between the core optimization algorithm and the loss analysis tool. The core optimization tool includes the effect of the magnetic material and core paralleling on the transformer power density. The materials properties as well as the cores data are obtained from Magnetics Inc. catalogue [17]. Cores paralleling is considered due to large cores avail ability and to add flexibility to the selection process. The tool outputs the optimal core weight, total losses, and maximum flux density at different frequencies. The total transformer losses are minimized at each frequency point by selecting an optimum flux density. The relationship between the maximum flux density and both copper and core losses is shown in Fig. 5, where the maximum flux density can be selected to minimize the transformer losses [9]. The local optimal frequency points are extracted from the core design tool and passed to the semiconductor loss analysis tool to obtain the overall device losses and plot it against the core weight.

Finally, the global optimum frequency point is obtained with the optimum core material and configuration from the

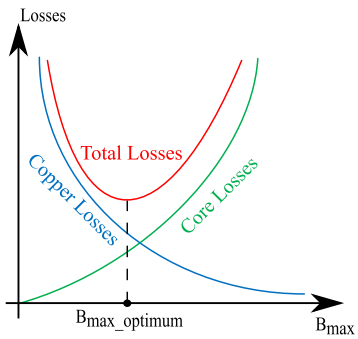


FIGURE 5. Optimum flux density and the total losses relation.

database. The optimal core is then passed to the winding design and optimization tool. Based on the selected core geometry, the transformer windings are automatically designed for different configurations. Two configurations are proposed and compared with two conventional winding configurations highlighting the effect on the transformer performance. The effect of the stray capacitance is usually not considered for most optimization processes in literature, which is a crucial parameter for the performance of planar transformers. There are two types of parasitic capacitance; self capacitance (intra-winding capacitance) which is formed between the same winding

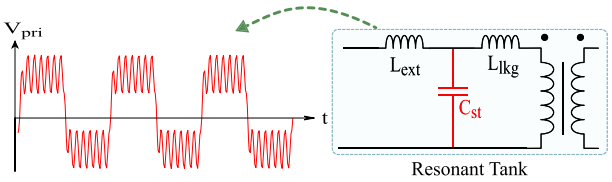


FIGURE 6. **Stray Capacitance Effect on the Transformer Waveforms.**

terminals and mutual capacitance (inter-winding capacitance) which appears between different windings. The effect of the inter-winding and intra-winding capacitances can be modeled using six different capacitors highlighted in Fig. 2(a) [18]. The inherit parasitic capacitances can also be lumped into a single capacitor model as illustrated in Fig. 2(b). HFO on the transformer voltages are the result from the formed resonant tank between the external inductance, stray capacitance, and the leakage inductance as shown in Fig. 6. The amplitude and frequency of oscillations depends on the resonant tank components values, the switching frequency, and the converter phase shift. The high oscillations highly affects the converter performance, power density and releability.

The proposed designs aim to mitigate the HFO issue without sacrificing the transformer power density and efficiency. The single stray capacitance is obtained analytically through the design tool for four different configurations. The values are automatically passed to PLECS to simulate the converter with the obtained parameters. The amplitude and frequency of oscillation are obtained highlighting the effect of the different configurations on the converter performance. The different configurations are simulated in ANSYS Maxwell to extract the capacitances values and evaluate the losses and compare it to the analytical tool results. The proposed design methodology is suitable for planar transformers in most applications to improve the power density and reduce the stray capacitance. However, the MEA application introduces a challenge in the required high turns ratio as well as the high current on the secondary side which must be considered while proposing a specific structure to reduce the transformer capacitance. Being one of the bulkiest elements in the power converters used onboard the aircraft, improving the power density by investigating different materials, cores in parallel, etc. is crucial in such application. The transformer mechanical assembly process of the proposed structures must be suited to the high-current transformers utilized in MEA converters. All the mentioned concerns have been considered in the proposed design methodology in this paper.

III. TRANSFORMER CORE SELECTION

A. TRANSFORMER CORE SELECTION PROCEDURE

The core material selection is the first step in the magnetic design process. The magnetic material highly affect the core losses and hence its temperature rise. Materials that features high permeability and high saturation-density such as nanocrystalline materials have been used lately in high-frequency applications. Such materials allow for size and weight reduction by pushing towards high-frequency operation due to their high saturation flux density and low core losses as compared to ferrite materials [19], [20]. The high cost and core shapes availability are the limiting factors for nanocrystalline materials where custom-made cores are needed for an optimized design. Ferrite materials, on the other hand, are available in many off-the-shelf core shapes and offer low core losses as compared to silicon steel. For these reasons, ferrite materials are still widely utilized in industry for high-frequency magnetics in power electronic converters. Three ferrite materials offered by Magnetics Inc. are considered in the optimization process proposed in this section. The material properties are listed in Table 2. A large planar off-the-shelf cores database is used in the design process.

The AP method is the most common approach to select a transformer core. The method is based on a factor which is the product of the window area and core area which is usually provided by most core manufacturers in their datasheets [21]–[23]. The product factor can be tied to the converter specifications using the following equation:

$$A_p = \frac{P}{K_t J B_{max} f}. \tag{1}$$

where f is the frequency, J is the winding current density, k_t is a factor depending on the converter topology, B_{max} is the maximum flux density and P is the converter power rating.

The maximum flux density in this method is selected, rather than optimized, to limit the core losses for a predetermined switching frequency.

The design method utilized in the optimization process is based on selecting an optimum maximum flux density to minimize the total losses. This optimum value can be obtained by finding the derivative of the total losses with respect to the maximum flux density and equating it to zero as follows:

$$\frac{dp_{tot}}{B_{max}} = \frac{dp_{copper}}{B_{max}} + \frac{dp_{core}}{B_{max}} = 0. \tag{2}$$

where P_{core}, P_{copper}, and P_{tot} are the copper losses, the core loss, and the total losses respectively.

The copper losses can be expressed as follows:

$$P_{Copper} = I_{tot}^2 R_{winding} = \frac{I_{tot}^2 n^2 MLT\, \rho}{w_A K_u}. \tag{3}$$

K_u is the utilization factor, MLT is the mean length per turn, W_A is the window area, n is the number of turns, ρ is the copper resistivity, $R_{winding}$ is the winding resistance, and I_{tot} is the total current referred to the primary side.

Applying Faraday's law, the number of turns can be found as:

$$n = \frac{\lambda}{2B_{max}A_c} 10^{-4} A_c^2. \tag{4}$$

where $\lambda = \mathrm{D} * f_{sw} * v_{in}$ is the voltseconds, D is the duty cycle, f_{sw} the switching frequency, v_{in} is the input voltage, B_{max} is the maximum flux density and A_c is the core area.

TABLE 2. Material Properties - Magnetics Inc

Material	Properties	Permeability @20kHz	$B_{sat}(T)$	Core losses (mW/cm^3)	Density (g/cm^3)	Thermal conductivity (mW.cm^{-1}.$^\circ C^{-1}$)
F	High temperature	3000		110		
P	stability, low losses,	2500	0.47	65	4.8	35-43
R	and high saturation flux	2300		58		

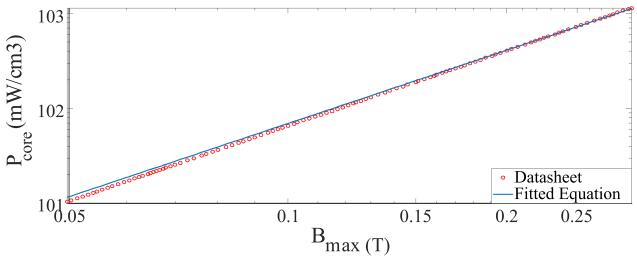


FIGURE 7. Datapoints fitting to Steinmetz equation.

TABLE 3. Extracted Steinmetz Coefficients

Frequency range	Coefficients	F-material	P-material	R-material
100kHz <f < 500kHz	K	27.42	18.092	17.23
	α	1.66	1.63	1.64
	β	2.68	2.62	2.68
f <100kHz	K	32.77	114.461	52.388
	α	1.72	1.36	1.43
	β	2.66	2.86	2.85

The copper losses can then be derived as:

$$P_{Copper} = \frac{I_{tot}^2 \lambda^2 MLT\, \rho}{4 w_A K_u A_c^2 B_{max}^2}. \tag{5}$$

Steinmetz equation is used to obtain the core losses:

$$P_{core} = K_{fe} B_{max}^{\beta} V_{core}. \tag{6}$$

where V_{core} is the core volume, β is the Steinmetz exponent and K_{fe} is a frequency-dependant constant.

An equation relating the core geometry and the converter specifications can the be derived from (2):

$$\frac{w_A A_c^{(2(\beta-1)/\beta)}}{MLT\, l_m^{(2/\beta)}} \left[\frac{\beta}{2}^{-\left(\frac{\beta}{\beta+2}\right)} + \frac{\beta}{2}\left(\frac{\beta}{\beta+2}\right) \right]^{-\left(\frac{\beta}{\beta+2}\right)} = \frac{I_{tot}^2 \lambda^2 \rho K_{fe}^{\frac{2}{\beta}}}{4 K_u P_{tot}^{\frac{\beta+2}{\beta}}}. \tag{7}$$

(7) can be used to select the transformer core. The left-hand side of (7) is related to the core geometry and can be calculated for a specific core, similar to the AP factor, using the dimensions given in the datasheet. The transformer core can then be selected based on K_{gf} in (8):

$$K_{gf} \geq \frac{I_{tot}^2 \lambda^2 \rho K_{fe}^{\frac{2}{\beta}}}{4 K_u P_{tot}^{\frac{\beta+2}{\beta}}}. \tag{8}$$

The core loss plots provided in the materials datasheet are used to obtain the Steinmetz coefficients at different frequencies. This is carried out by fitting the data given to the Steinmetz equation as in Fig. 7. The parameters are extracted for all the materials used in the optimization process and are listed in Table 3.

The design methodology flowchart is illustrated in Fig. 4 under core selection. At first, the geometrical constant K_{gf}, that is the left-hand side of (7), is obtained for all the cores listed in the database. The frequency is initialized as 1 kHz and the number of cores in parallel (N) is set to 1 and the first material is selected. Based on the converter specification, the core is selected based on (8). Using Faraday's law, the number of turns is then calculated. The flux density is reevaluated using (4) based on the number of turns and ensured to be below the core saturation flux (B_{sat}). The transformer losses are then obtained using (5) and (6) and verified not to exceed a predetermined limit set by the designer, based on the required efficincy and the cooling method used. The process selects a larger core in case of flux saturation, or if the losses or the current density are above the limits. The frequency is then incremented by a 1 kHz step and the optimum selection process is repeated up to 500 kHz. The number of parallel cores is then incremented and the process is repeated. The number of cores in parallel is limited to three cores due to mechanical stacking limitations and the average MLT to limit the conduction losses. When a maximum of three paralleled cores is reached, the design process is carried out for the next available material. The results of this design process yields some potential optimum frequency points as will be discussed in the results section. Those frequency points are then passed to the semiconductor loss analysis tool, where the switches losses are calculated for the different frequency point. The optimum switching frequency is then selected based on the integration process and hence the optimum transformer core.

B. CORE SELECTION TOOL RESULTS

A single-core design is considered first to compare between the three materials. Figs. 8 and 9 show the total transformer loss and the core weight for different materials respectively. The power loss changes with frequeny since different optimum flux density is selected at each frequency point and hence different number of turns. As illustrated in Fig. 9, there are limited single cores available to meet the power requirements and hence a multiple parallel core design is required to optimize the core weight. R material shows the best characteristics in terms of losses and transformer weight vs frequency as shown in Figs. 8 and 9. The analysis is then carried out for R material considering cores paralleling. Fig. 10 illustrates the

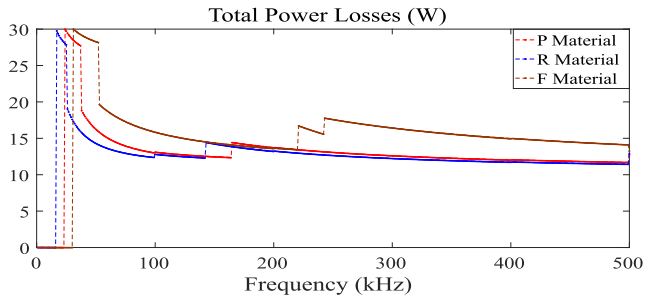


FIGURE 8. Total Transformer Losses against Frequency for Different Materials.

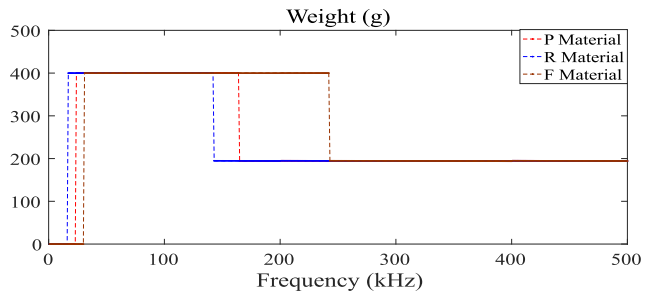


FIGURE 9. Weight against Frequency for Different Materials.

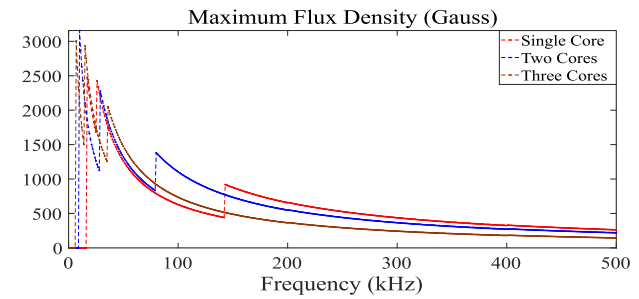


FIGURE 10. Maximum flux density against frequency.

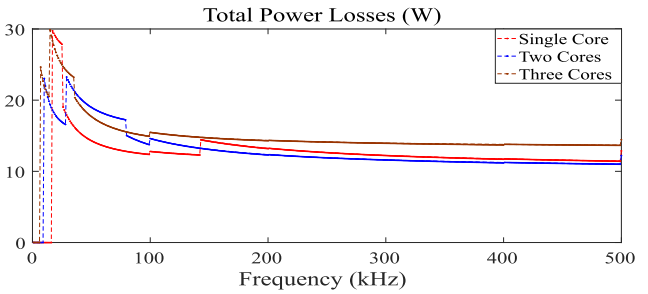


FIGURE 11. Total transformer losses against frequency for parallel cores.

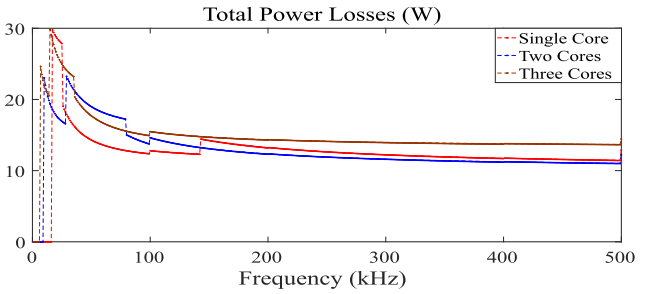


FIGURE 12. Core weight against frequency for parallel cores.

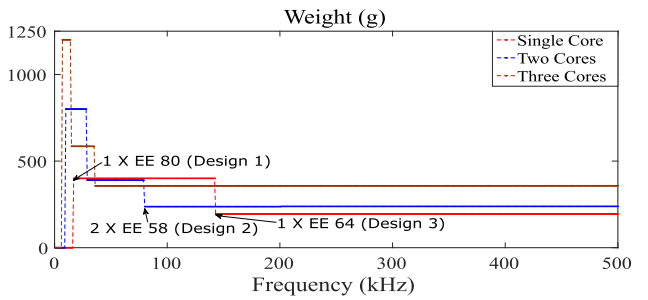


FIGURE 13. Semiconductor losses integration results.

maximum flux density as a function of the frequency for different number of parallel cores for R material. The maximum flux density decreases as the frequency increase to limit the core losses. The core size cannot be lowered after a specific frequency point because of the current density limitation. A minimum copper area for the windings and hence a minimum window area is required based on the current density constraint. The losses and weight considering paralleled cores configuration are shown in Figs. 11 and 12 respectively. As a result, Two EE 58 cores, labeled as Design 2 in Fig. 12., were obtained with a total weight of 238 g, featuring a volume of 49200 mm^3 and 15 W of losses. Design 3, on the other hand, is a single EE 64 core weighting 200 g, featuring a volume of 41400 mm^3 and 14 W of losses. Design 3 seems to be the optimum design from the transformer's perspective since it is 16% lighter and less voluminous and it has 7% lower losses. However, Designs 1 & 2 features lower switchng frequency as compared to Design 3 and hence lower switching losses and better efficiency on the converter level. This calls for an integration between the core selection and the switches loss analysis to ensure an overall optimized design on the converter level. There are local optimum frequency points from the transformer perspective such as the three designs highlighted in Fig. 12. Those points are passed to the switches loss tool and results of the loss analysis are used to get a global optimum switching frequency. The losses of the MOSFETs of the DAB converter are then obtained at the different local frequency points extracted from the transformer tool. The design has been developed with Silicon Carbide (SiC) FETs for the HV bridge (SCT3160KLHRC11) and Silicon (Si) devices for the LV side (IPP023N10N5AKSA1). Two SiC devices are connected in parallel for each primary switch and six Si devices are paralleled for the secondary-side switches. Results of the loss analysis are illustrated in Fig. 13 considering having zero-voltage switching (ZVS) and also in case

TABLE 4. Windings Description

Parameter	Value
Number of secondary turns	1
Number of primary turns	22
Copper thickness	175 μm
Number of secondary layers	12
Number of primary layers	6

of no ZVS. This is to discuss the importance of integrating the loss analysis with the transformer tool results in selecting the optimum switching frequency and hence the optimum transformer core. Fig. 13 shows three design lines, at 35 kHz, 85 kHz and 150 kHz. Considering having a ZVS condition, Design 2 at 85 kHz seems to be better than Design 1 at 35 kHz since the losses have not increased significatly and the weight of the core is reduced by 33%, also the EMI filter size will reduce for Design 2 due to the higher switching frequency. However, if the topology does not have ZVS, it can be seen from Fig. 13 that the losses increase by a large value from Design 1 line to Design 2 and in this case, Design 1 seems to be the optimum design. This indicates that the global optimal switching frequency point depends on the topology as well. As for Design 3, the losses increase compared to Design 2, which results in an increase in the thermal management requirements, and only a reduction in the core weight by 35 g. Weighting factors can be assigned to both the total losses and core weight to select the switching frequency. In this MEA application, the weight assigned to the losses is 40% and 60% to the core weight. Based on the converter design requirements, different weights can be assigned. Design 2 was selected as the optimum frequency point. The developed tool provides guideliness to optimize the core weight considering the overall converter efficiency by optimizing the flux density and selecting and optimum switching frequency.

IV. TRANSFORMER WINDING DESIGN AND OPTIMIZATION

A. TRANSFORMER STRAY CAPACITANCE

Large overlapping area in the conventional winding configurations in planar transformers results in high frequency oscillations limiting their applications in MEA. The HFO resulted from the transformer parasitic capacitances highly impacts the converter reliability. This section proposes a multilayer winding design to mittigate the HFO issue. The optimum core geometry and required number of turns resulted from the transformer core optimization process are used to design the winding stack. Based on the optimal core height, the number of layers are specified and kept the same for all configurations. The copper thickness is selected based on the optimum switching frequency to limit the winding AC losses. The windings information are listed in Table 4. The proposed designs are compared to two conventional configurations highlighting the impact on the converter performance. Fig. 14 shows the parasitic capacitances for the conventional

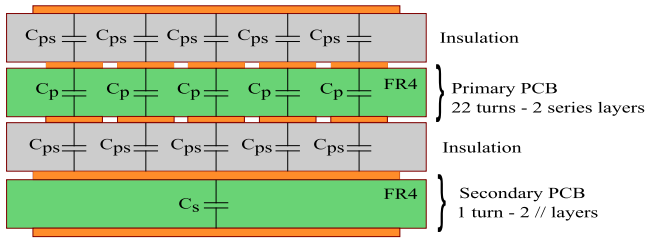


FIGURE 14. Layers capacitances in planar transformers.

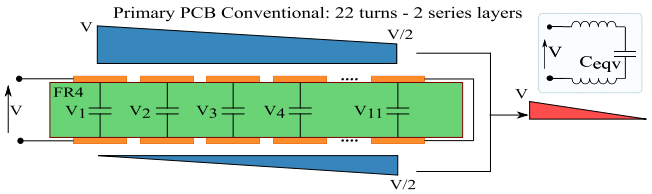


FIGURE 15. Primary winding capacitance for conventional configuration.

interlaved configuration. There are trade-offs between reducing the eddy current effect by interleaving the layers and increasing the mutual stray capacitance. The stray capacitance forms a resonant tank with the leakage inductance and the auxilary inductance added in the DAB converter as well as in resonant converters. For the same winding, the same capacitance is formed between the turns on different layers as shown in Fig. 15. However, the voltage across each capacitance is different due to the voltage drop between the turns. This results in an unequal voltage distribution across the capacitors as illustrated in Fig. 15. The energy stored in each capacitor can be obtained and summed up to represent a single intra-winding capacitor. Since the energy of each capacitor is proportional with the voltage squared across it, the equivalent capacitor of such configuration is large and causes HFO on the transformer voltage waveforms. The winding equivalent capacitance and stored energy can be expressed as follows [11]:

$$V_i = \frac{(n+1)-i}{n} V, (i = 1, 2, 3, \ldots, n). \tag{9}$$

$$E_{tot} = \sum_{i=1}^{n} E_i = \frac{1}{2} C_p V^2 \sum_{i=1}^{n} \left(\frac{(n+1)-i}{n} \right)^2 = \left(\frac{(n+1)(2n+1)}{12n} \right) C_p V^2. \tag{10}$$

$$C_{eqv} = \left(\frac{(n+1)(2n+1)}{6} \right) n C_p. \tag{11}$$

V_i is the voltage across the individual turns between the PCB layers, V is the overall voltage across the winding, C_p and E_i are the individual capacitance and energy respectively, C_{eqv} and E_{tot} are the equivalent capacitance and energy stored respectively.

Changing the way the turns are routed on the planar PCBs can result in an equal low voltage distribution across the turns

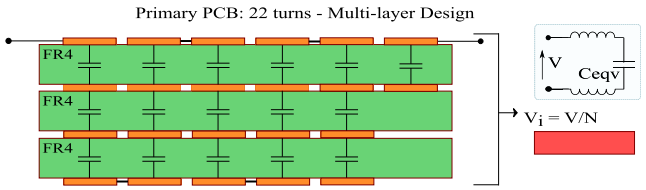


FIGURE 16. **Primary winding capacitance for MLMG configuration.**

capacitance and hence a lower equivalent intra-winding capacitance as illustrated in Fig. 16. The MLMG aims to have an equal voltage distribution across all turns capacitances by utilizing blind crossed vias connections between the layers. Fig. 17 illustrates the conventional and proposed configurations highlighting the winding connections of the proposed design with the equivalent electrical schematic of the turns. The overall transformer power density is kept the same as the conventional configuration. The board thickness, if required, can be kept the same as the double layers design by reducing the copper thickness of the turns on each layer. The current density is maintained low by increasing the width of turns since lower number of turns are routed on each layer. However, the intra-capacitance is lowered by having equal lower voltage distribution across the turns capacitance of $\frac{V_{winding}}{N}$. Based on the same approach of getting the total energy stored between the layers, the equivalent energy stored and winding capacitance of the MLMG configuration can be expressed as follows:

$$E_{tot} = \sum_{n=1}^{N} E_i = \frac{2}{N^2} C_p V^2. \tag{12}$$

$$C_{eqv} = \frac{2}{N^2} C_p. \tag{13}$$

Compared to a similar low-voltage distribution conventional two-layers design, the transformer power density is improved by 20%. As illustrated in Fig. 14, inter-winding capacitances are also formed between the primary and secondary layers. Reducing the interfaces between the different winding turns results in a lower lumped stray capacitance. The second proposed configuration, aims to utilize multi-layer configuration to reduce the interfaces between the primary and secondary layers reducing the inter-winding capacitance. Each layer of the 3-layers board is duplicated and connected in parallel to the original layer so that zero voltage is across them. However, the leakage flux between the layers is increased resulting in higher AC losses. This is the trade-off between the transformer losses and lower stray capacitance previously mentioned. Both proposed configurations are compared to the conventional interleaved and non-interleaved configurations in terms of AC losses and stray capacitance.

Even though the non-interleaved configuration has only one interface between the primary and secondary windings and hence lower inter-winding capacitance, it is usually not considered for its high losses. As highlighted, a loss analysis for the different configuration is crucial in the design process while comparing the stray capacitance of each configuration. The inter-winding capacitance between the primary and secondary boards can be reduced as well by increasing the insulation thickness between them; however, this will result in a lower core window utilization and hence higher copper losses.

The insulation between the primary and secondary layers for MEA applications is limited by the Information Technology Equipment Safety standard IEC 60950-1 for voltages below 600 V. The insulation needs to be at least 0.4 mm, when a single-layer insulation is used. While for reinforced insulation (double layers), no specific minimum thickness is required. The used insulation thickness and material affects the inter-winding capacitance. For instance, air has lower permittivity than other insulation materials such as FR4 or Kapton and hence lower capacitance between the layers; however, the insulation must withstand the breakdown voltage between the layers. A double insulation layers with either FR4 or Kapton as the first layer and air as the second layer will ensure meeting the breakdown voltage requirements as well as MEA standards of using double insulation. This will result in lower capacitance since one of the layers is air instead of FR4 or Kapton. Fig. 18 shows the insulation layer; where FR4 material is utilized as the first insulation layer and hollow Kapton tape is used on top to create an air seperation between the windings acting as a second layer. Each of the two layers is of 0.1 mm thickness which ensures meeting the voltage breakdown requirement. This configurations allows for reducing the inter-winding capacitance without increasing the AC losses.

Fig. 19 compares between the conventional high-capacitance design, the MLMG design and low-capacitance two-layers configuration. The volume is kept the same with the multilayer design. However, for the conventional two-layers design, in order to reduce the transformer capacitance, the volume of the transformer is increased by 20%.

B. TRANSFORMER LOSS ANALYSIS

The windings configuration and operating frequency highly impact the transformer losses due to the eddy losses which calls for an accurate prediction of the transformer losses to optimize its performance. The non-interleaved windings is often omitted due to the high copper losses caused by the proximity effect. On the other hand, the interleaved configuration exhibit lower copper losses. The magnetomotive force (MMF) distribution of the interleaved layout, illustrated in Fig. 20, indicates a low MMF generated in between and inside the layers. This results in a uniform current distribution inside the layers and hence a reduction of the losses caused by the proximity effect [24]. The AC/DC resistance ratio is obtained using Dowell's formula to get the AC losses [25], [26]:

$$F_r = \frac{P_{AC}}{P_{DC}} = \frac{R_{ac}}{R_{dc}} = \Delta \left[\zeta_1 + \frac{2}{3}(M^2 - 1)(\zeta_1 - 2\zeta_2) \right]$$

$$\zeta_1 = \frac{sinh(2\Delta) + sin(2\Delta)}{cosh(2\Delta) - cos(2\Delta)}$$

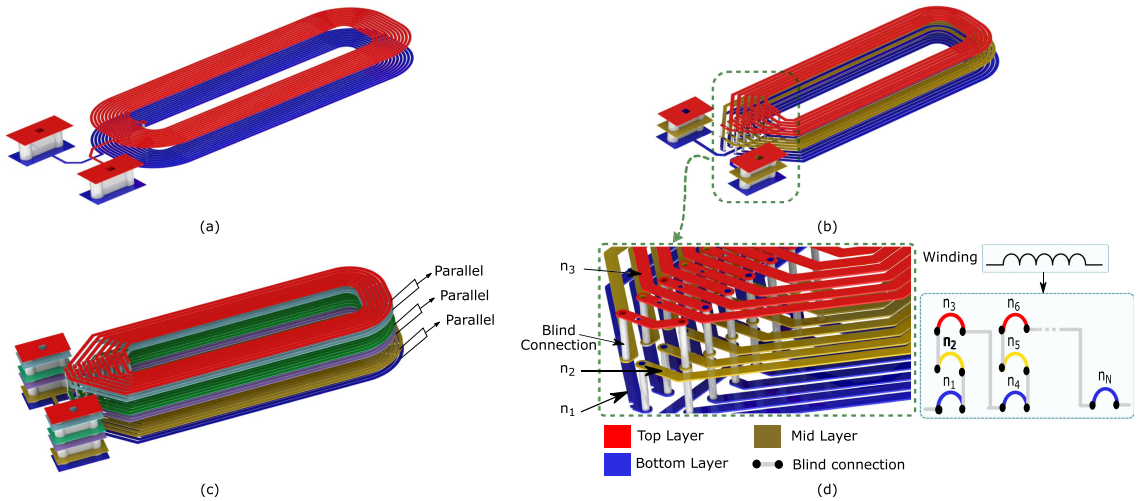


FIGURE 17. Different winding turns configurations: (a) Conventional 2 layers configuration, (b) Proposed MLMG configuration 1 - 3 layers, (c) Proposed MLMG configuration 2 - 6 layers, and (d) Zoomed-in view of the MLMG configuration.

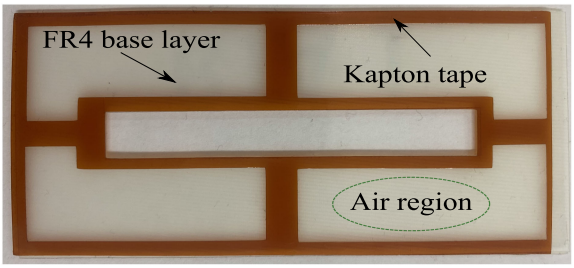


FIGURE 18. Double insulation layers between the primary and secondary windings.

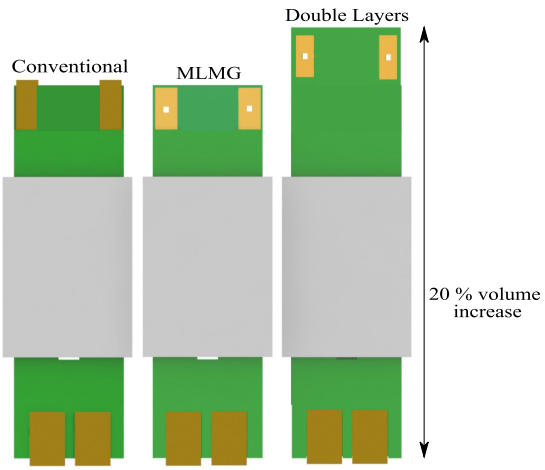


FIGURE 19. Power density comparison - conventional design vs. MLMG configuration.

$$\zeta_2 = \frac{sinh(\Delta)cos(\Delta) + cosh(\Delta)sin(\Delta)}{cosh(2\Delta) - cos(2\Delta)}$$

$$\Delta = \frac{t}{\delta}. \tag{14}$$

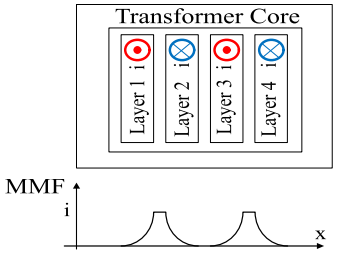


FIGURE 20. MMF diagram of fully interleaved windings.

where F_r, is the AC/DC losses ratio, M is the number of layers, t is the copper thickness, and δ' is the skin depth.

To minimize the winding losses, a copper thickness of equal or less than the skin depth is required [27]. Hence, printed circuit boards (PCB) are considered for both the primary and secondary windings with 5 oz (175 μm) copper thickness. Different stacking structures are investigated considering both the proposed and conventional configurations, as shown in Fig. 21. Layouts (b), (c) and (d) represent a section of the full stack. The proposed 3 layers configuration has the same MMF amplitude as the conventional fully interleaved winding and hence the same AC/DC resistance ratio. However, the 6 layers configuration is similar to the semi-interleaved configuration with less interfaces between the primary and secondary windings and higher MMF amplitude. The non-interleaved structure has the highest MMF amplitude and therfore higher leakage flux between the layers resulting in higher AC losses. The analytical calculations based on the analysis presented are compared with FEA results.

C. FEA VALIDATION AND NOISE ANALYSIS

Three different winding layouts are simulated in ANSYS Maxwell to validate the low capacitance and minimum voltage gradient between layers for the proposed designs for

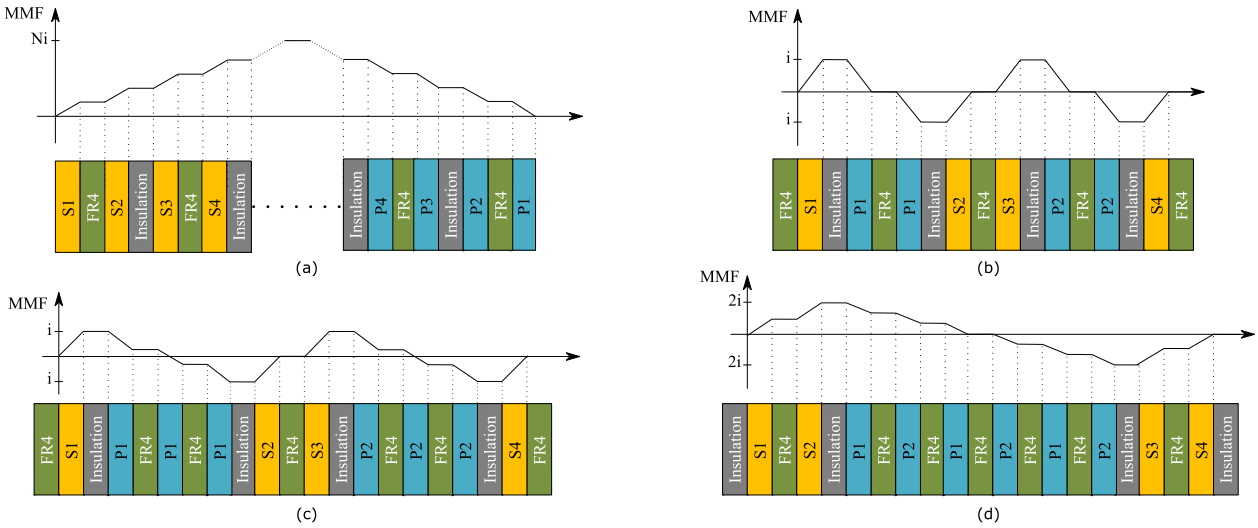


FIGURE 21. **MMF diagram for different stacking structures: (a) non-interleaved configuration SSSS—PPPP, (b) conventional fully interleaved configuration SPPSSPPS, (c) MLMG 3-layers fully interleaved - SPPPSSPPPS, and (d) MLMG 6-layers semi-interleaved SSPPPPPPSS.**

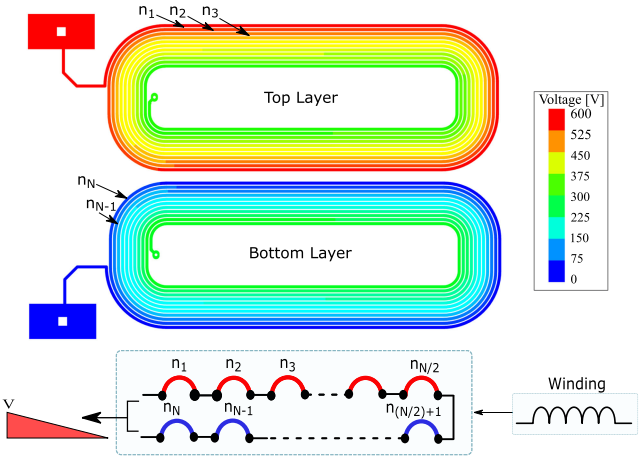


FIGURE 22. **Voltage distribution across the turns - conventional configuration.**

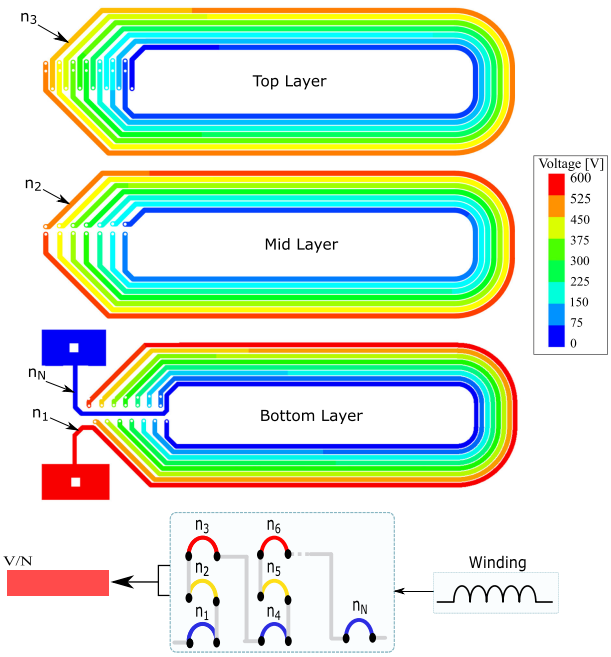


FIGURE 23. **Voltage distribution across the turns - MLMG configuration.**

the primary winding. Since the secondary winding has only one turn, the equivalent intra-capacitance formed between the parallel layers is zero since the voltage across the parallel laters is zero and hence no electric field stored in-between the layers. Fig. 22 shows the voltage distribution for a conventional double layer design for the primary side. Half of the turns are implemented on the top layer and the other half on the bottom layer. Unequal voltage distribution across the turns capacitances results in a non-uniform electric field with high strength towards the outer turns. The electric field magnitude reduces to become minimal at the most inner turns. This results in a high total stored energy between the two layers and therefore a higher intra-capacitance. The voltage distribution of the proposed MLMG design is shown in Fig. 23. The voltage gradient between the overlapping turns across all layers is minimized by alternating the turns between all layers. Since three layers are utilized to route the turns, more space is available to increase the turn width and reduce the DC resistance as compared to the double-layers design. The transformer power density is not compromised either by maintaining the width of the PCB as the conventional double-layers layout. A similar double-layers design would require an increase in the boards width and result in a 20% increase in the transformer volume. The voltage distribution of the MLMG 6-layers layout is the same as that shown in Fig. 23, since its the same layout but with each layer duplicated and connected in

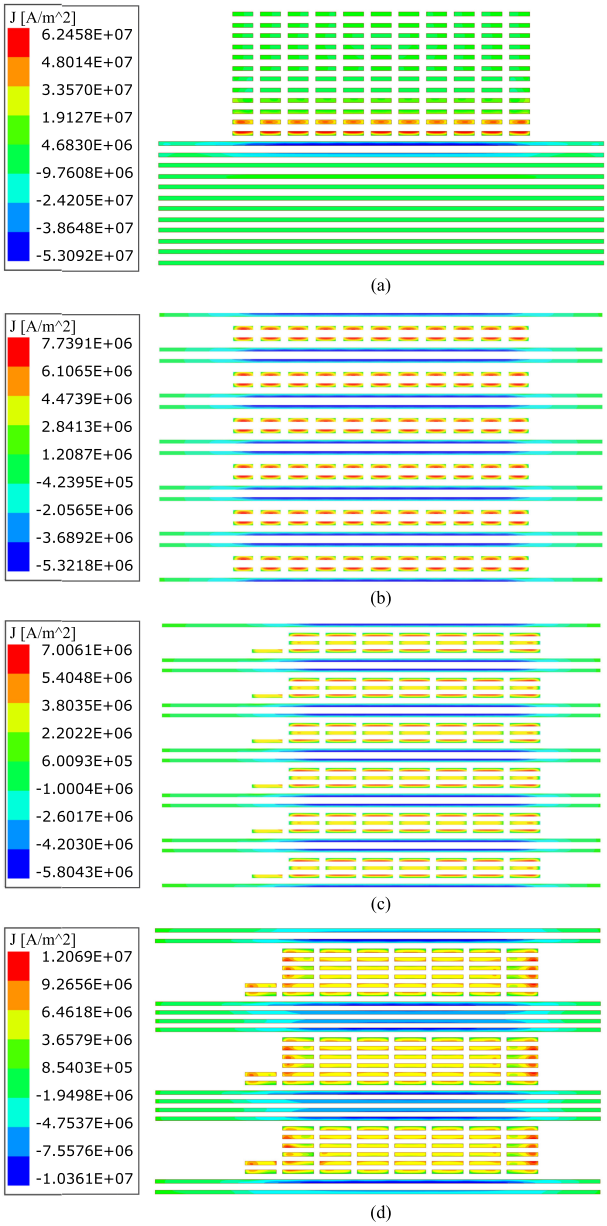


FIGURE 24. Current density plot: (a) non-interleaved configuration SSSS—PPPP, (b) conventional fully interleaved configuration SPPSSPPS, (c) MLMG 3-layers fully interleaved - SPPPSSPPPS, and (d) MLMG 6-layers semi-interleaved SSPPPPPPSS.

parallel to the original three layers. However with a main aim to reduce the intersections between the primary and secondary windings. Table 5 lists the capacitances extracted from the three FEA models and compares the values to the analytical approach. Two conventional interleaved and non-interleaved configurations are compared to one fully-interleaved MLMG 3 layers design and a semi-interleaved MLMG 6-layers stacking layout. The current density plots of the different stacks is shown in Fig. 24. Since the MMF magnitude is highest for the non-interleaved configuration, the layers current density is very high which results in high AC losses. Both the

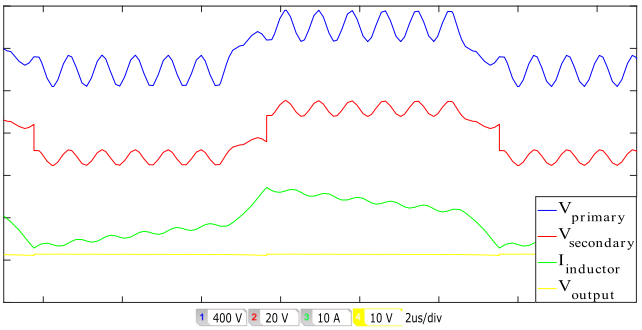
TABLE 5. Simulation Vs. Analytical Results

Configuration	Intra-winding capacitance (pF)		Copper Losses (W)	
	Analytical	FEA	Analytical	FEA
Conventional Non-interleaved	125.4	120	152.57	140.3
Conventional Interleaved	125.4	120	19.93	16.66
MLMG 3-layers	8.29	7.97	15.2	14
MLMG 6-layers	7	6.6	26.26	28.3

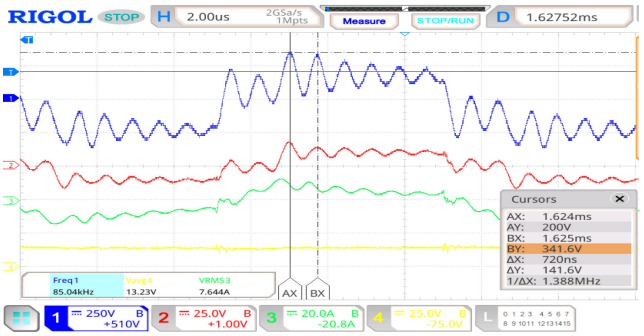
conventional and MLMG interleaved configuration exhibit the lowest current density and ac losses. The MLMG stack has better current distribution compared to the conventional stack since the width of the turns is increase to utilize the board space which results in higher efficiency. For the MLMG 6-layers stack, the current density is higher than the 3-layers layout due to the high AC losses caused by the higher MMF magnitude. Table 5 also lists the total copper losses resulted from the FEA as compared to the analytical approach. Since the MLMG 3-layers layout exibits the highest efficiency and low intra-winding capacitance, its transformer performance is analyzed in PLECS and compared to the conventional configuration highlighting the effect on reducing the HFO. The extracted capacitances and winding AC resistances are imported in PLECS for both configuration. Two series 20 μH inductors, with an 8 mΩ series resistance each, were used in the converter testing. Two (SiC) FETs are used in parallel for the HV bridge switches (SCT3160KLHRC11) and six Si devices in parallel for the LV side switches (IPP023N10N5AKSA1). The output capacitance of the MOSFETs, on both the primary and secondary sides, were modeled along with the parasitic series resistance of the added external inductor. The transformer stray capacitance, leakage inductance and windings resistances were added in the PLECS model as well. Fig. 25 shows the transformer waveforms for the interleaved configuration both in PLECS and experimentally. The analysis shows a close match in terms of the amplitude and frequency of the oscillations. Fig. 26 shows the waveforms in PLECS for proposed configuration. The oscillations are substantially reduced for the proposed design due to the reduction of the parasitic capacitance.

V. EXPERIMENTAL VALIDATION

Three transformers were built to verify the design approach. One of the transformers utilizes the MLMG configuration along with double insulation layers; one of which is an air layer. The two other transformers includes double FR4 insulation stack. The manufacturing cost is almost the same for the three prototypes since the same number of PCB layers are used in each. Despite having higher number of PCB layers, the MLMG board cost is still the same as the conventional configuration since more space (layers) are available to route the turns which allows for lowering the copper thickness as compared to the conventional configuration. The frequency response of a single layer for both the conventional



$V_{overshoot} = 140\ V, f_{osc} = 1.388\ MHz]$
(a)



$V_{overshoot} = 160\ V, f_{osc} = 1.35\ MHz]$
(b)

FIGURE 25. Parasitic capacitances effect - interleaved configuration((a) PLECS simulation) and (b) Experimental waveforms.

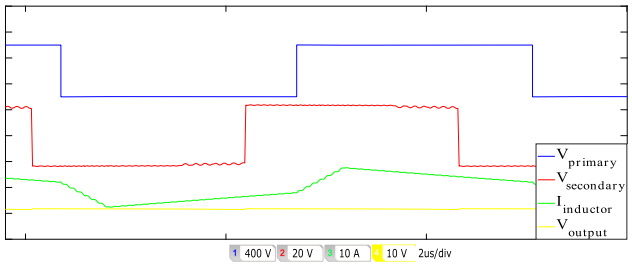


FIGURE 26. Parasitic capacitances effect - MLMG configuration (PLECS simulation).

and MLMG designs is shown in 1 Fig. 28. The resonance frequency of the MLMG configuration is higher than the conventional design due to the lower capacitance. This is the case since both designs have the same number of turns, therefore the same inductance and, for fixed inductance, the capacitance ratio of an LC circuit is the square of the resonance frequency ratio. The experimental results shows 15 times $(6.56/1.713)^2$ less capacitance for the MLMG with a close match to the FEA simulations previously listed in Table 5. Fig. 29 shows the frequency response for the three assembled transformer for a shorted secondary side emulating a rated-load operation. Both MLMG transformers surpassed the conventional design in-terms of the higher resonance frequency and hence

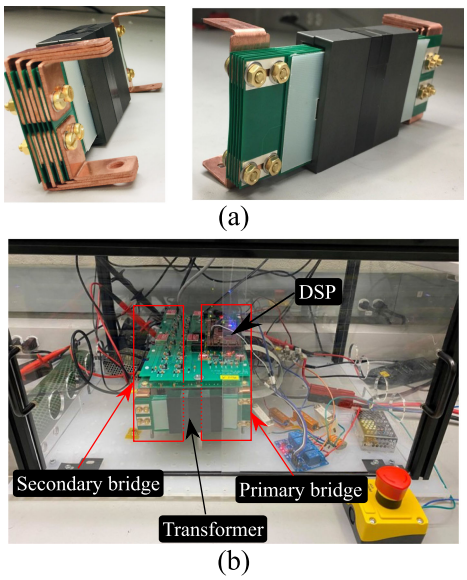


FIGURE 27. Experimental prototype: (a) Transformer prototype and (b) DAB converter platform.

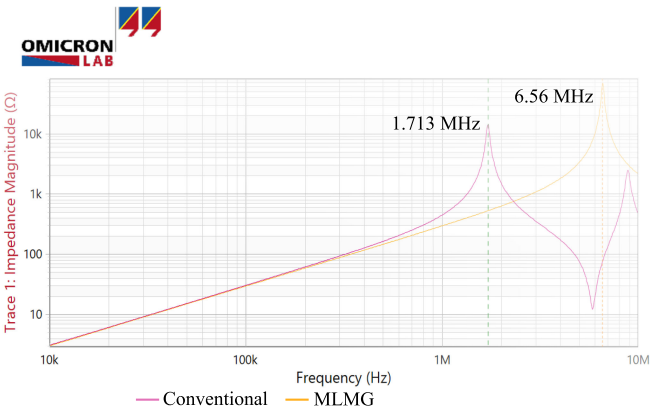


FIGURE 28. Single PCB frequency response - conventional vs. MLMG.

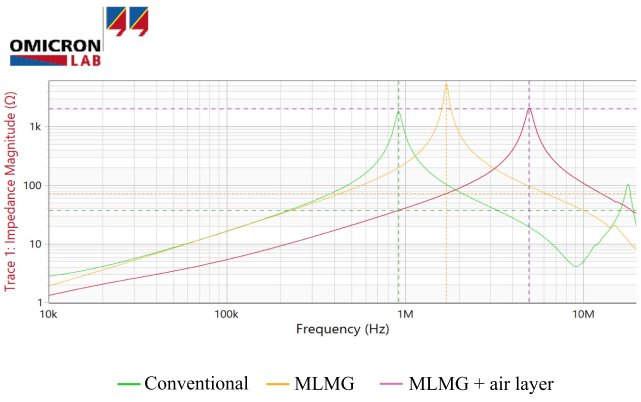


FIGURE 29. Frequency response of transformer stack with shorted secondary.

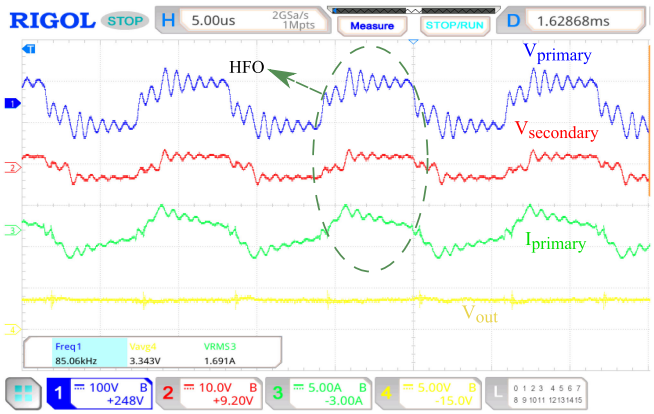


FIGURE 30. Converter performance - conventional structure waveforms.

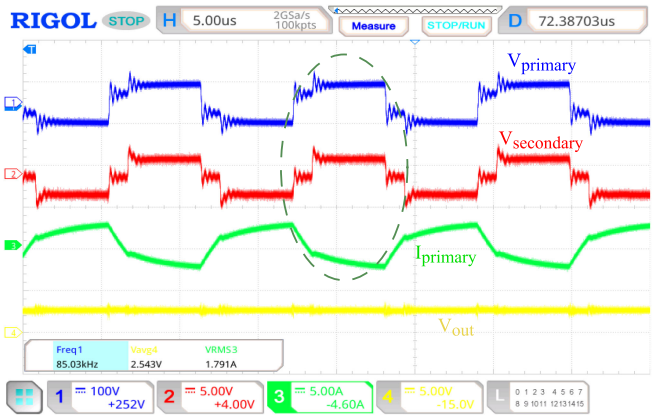


FIGURE 31. Converter performance - conventional structure waveforms.

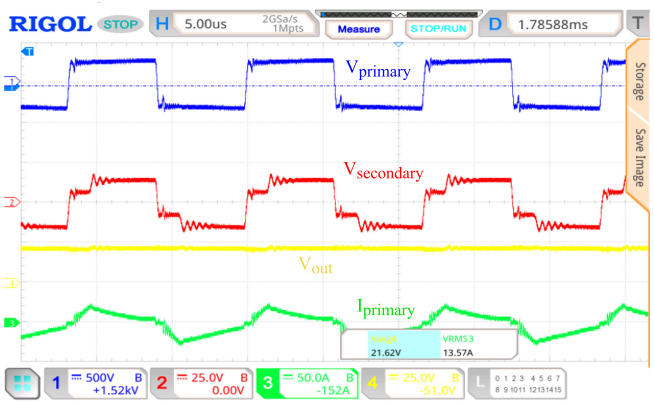


FIGURE 32. Experimental waveforms (4 kW, 300 V input, 22 V output).

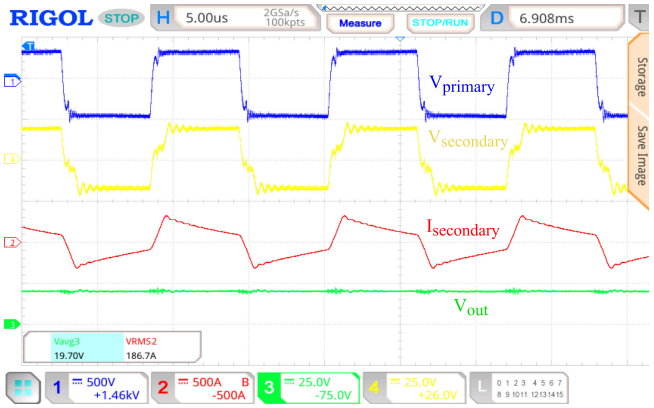


FIGURE 33. Experimental waveforms (3.8 kW, 400 V input, 20 V output).

the lower lumped capacitance. The MLMG transformer utilizing an air layer has the highest resonance frequency due to the low inter-winding capacitance. The transformers parts were designed, manufactured and assembled as illustrated in Fig. 27(a). The transformers were assembled with a DAB platform as illustrated in Fig. 27(b). Fig. 30 and Fig. 31 show the transformer waveforms at light load. By comparing both figures, the HFO are significantly reduced for the proposed design. The power density is the same for both prototypes since no PCB area is added for the MLMG configuration to achieve low-voltage gradient between the layers which is the main advantage of this multi-layer configuration. The converter is tested at full load with the optimized transformer. The resonant tank behaviour is related to the phase shift of the DAB converter. A higher phase shift will cause a high voltage drop across the external and leakage inductances and therefore alter the oscillations magnitude. The converter is tested at full load and different operating points. This is done to ensure high converter performance at different phase shifts across the whole range. Fig. 32 shows the experimental waveforms of transformer primary and secondary voltages as well as the leakage inductance current at 4 kW with 300 V and 22 V as input and output voltages respectively. The transformer was then tested at the second opeating point at 3.8 kW, 400 V at the input, 190 A at the output side, and 20 V. The waveforms of the primary, secondary and output voltages as well as the high secondary current waveforms are shown in Fig. 33.

VI. CONCLUSION

In this paper, a design methodology for planar transformers for MEA was presented with the main focus on the transformer power density and converter performance. The selection of the optimal switching frequency and the transformer core were discussed. The importance of the optimization tool was highlighted considering paralleling of cores and different magnetic materials. The core selection guidelines are combined with the results from the device switching loss analysis. Having such an integrated solution between the transformer and the switching devices ensures an optimum selection of the switching frequency to optimize the size and weight of the transformer core considering the overall converter efficiency. The process of extracting the transformer parasitic components has been discussed highlighting the importance of considering the effect of such parasitics and how the transformer performance can be affected. Two winding

structures were proposed and compared to the conventional spiral double-layer configurations. The proposed structures showed a significant reduction in the transformer capacitance and improvement of the converter performance. By utilizing multi-layers, the transformer power density and efficiency are not compromised. The proposed structures were validated in ANSYS Maxwell 3D and the converter performance was investigated in PLECS. The developed methodology is able to provide reliable results that were experimentally validated with a DAB converter prototype.

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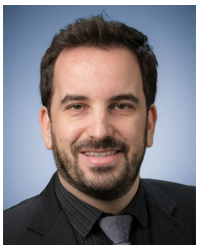

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