A Scalable System Architecture for High-Performance Fault Tolerant Machine Drives

FILIPPO SAVI [1] **(Graduate Student Member, IEEE), DAVIDE BARATER** [2] **(Senior Member, IEEE),**
GIAMPAOLO BUTICCHI [1] **(Senior Member, IEEE), CHRIS GERADA** [1,3] **(Senior Member, IEEE),**
AND PAT WHEELER [3] **(Fellow, IEEE)**

[1]Key Laboratory of More Electric Aircraft Technology of Zhejiang Province, University of Nottingham Ningbo, Ningbo 315100, China
[2]Università degli studi di Modena and Reggio Emilia, 41121 Modena, MO, Italy
[3]University of Nottingham, Nottingham NG7 2NN, U.K.

CORRESPONDING AUTHOR: Filippo Savi (e-mail: filippo.savi@nottingham.edu.cn)

ABSTRACT When targeting mission critical applications, the design of the electronic actuation systems needs to consider many requirements and constraints not typical in standard industrial applications. One of these is tolerance to faults, as the unplanned shutdown of a critical subsystem, if not handled correctly, could lead to financial harm, environmental disaster, or even loss of life. One way this can be avoided is through the design of an electric drive systems based on multi-phase machines that can keep operating, albeit with degraded performance, in a partial configuration under fault conditions. Distributed architectures are uniquely suited to meet these challenges, by providing a large degree of isolation between the various components. This paper presents a system architecture suitable for scalable and high-performance fault tolerant machine drive systems. the effectiveness of this system is demonstrated through theoretical analysis and experimental verification on a six-phase machine.

INDEX TERMS DC-AC power converters, fault tolerance, current control, multiphase machines, resonant control.

LIST OF SYMBOLS

ω_e	Electrical angular speed
ω_m	mechanical angular speed
V_{ph}	Phase Voltage
I_{ph}	Phase current
α_e	electrical angular acceleration
R_{ph}	Per-phase winding resistance
L_{ph}	Per-phase winding inductance
V_{ph}	Per-phase winding inductance
T_E	Electrical Torque
T_A	Acceleration Torque
T_L	Load Torque
J	Rotor moment of inertia
α_m	mechanical angular accelleration
K_e	Back-emf constant

n_p	Number of poles
η	Inverter efficiency
K_p	Proportional gain
K_i	Integral gain
K_r	Resonant gain
ζ	Resonant damping
L_n	n-th winding self inductance
$M_{n,m}$	Mutual inductance from n-th to m-th winding
$I(6)$	Six-by-Six identity matrix
$J(6)$	Six-by-Six ones matrix

I. INTRODUCTION

The great flexibility of electric machines and drives when it comes to fine control has pushed the adoption of electrical actuation in many applications. One of the aspects where

electrical machines and power electronics have historically lagged other technologies is in high reliability and fault tolerance systems. When it comes to mission critical applications, the use of fault tolerant system designs and topologies may be necessary, in order to prevent single faults from causing serious accidents, serious consequences, like environmental disasters, large financial damages or even loss of lives. One of the key principles underpinning this strategy is the tolerance of all the critical components to the system functionality to single and even multiple faults. As an example, in both the offshore marine [1] and aerospace [2], [3] sectors, fault tolerant actuation is seen as of crucial importance, and can consequently be seen as an indispensable precondition needed for widespread adoption of electrical actuation in these mission critical applications.

Much work has already been done in this area, from the electrical machine perspective, where research has proceeded in multiple directions. One of these avenues of research is the advent of multi three-phase machines, where multiple three-phase winding sets are used in the same motor [4], [5]. These motors have the advantage of a large degree of isolation between the partitions, simplifying the system level design. Another complementary approach has also been proposed, with single neutral star connected multi-phase machines [6], [7]. Having a single neutral point gives these machines more degrees of freedom, allowing them to achieve better performance in post-fault operation. In fact, they are always able to operate all remaining phases, as opposed to split neutral designs where two faults in the same set force even the healthy phase offline, requiring a higher degree of thermal and electrical de-rating. Work has also been done on the thermal characterization of the machine, when operating with a reduced number of phases, as depending on the type of fault, the distribution of heat generation in the stator can deviate substantially from nominal [8], [9].

For the power electronic converters several strategies have been proposed, depending on the exact configuration of the electrical machine. The most common solution recommended for multi three-phase systems is the use of an equal number of traditional inverters to feed each one of the machine windings sections [10]–[12]. The only difference between these and the traditional inverters used in industrial automation application, is the addition of either droop based, or master slave, control components. To ensure a balanced power-sharing, making this solution simple and cost-effective. Another possible approach, suggested in [13]–[15], is the use of a separate power converter for each one of the machine phases, making the whole drive system much more impervious to the propagation of faults between adjacent phases due to second order effects from usually negligible couplings. The main downside of this approach is its higher cost and complexity, requiring fully custom hardware and control techniques in order to ensure correct operation.

A common trait between all these architectures, is their extensible construction, where a base unit is repeated multiple times in order to obtain the desired degree of fault

isolation. This suggests the suitability of these topologies in very high-power applications, where modular constructions are needed to deal with the large currents and voltages. The only notable difference between these two applications, is the much higher number of base components used, imposing strict scalability requirements on the overall system architecture.

This paper introduces a novel system architecture, specifically aimed at the implementation of fault tolerant machine drive systems. During the design strong emphasis is placed also on the scaling capabilities of the proposed system, to take better advantage of the modularity of modern fault tolerant multi-phase machine designs. A demonstration platform is also presented for validation. To achieve the stated goals a comprehensive design approach was followed, evaluating the system in its entirety, from Human-Machine Interface (HMI) to power electronics, sensing and control. To tie everything together a custom low latency and deterministic communication protocol is introduced, capable of supporting the development of distributed power electronics real time control systems.

In Section II the system architecture is described. Section III discusses the custom communication network, upon which the architecture is based. In IV,the hardware used in this paper, and fault tolerance of the proposed architecture is examined in more detail for each part of the overall converter. The current control system is then presented in Section V. Finally, the presented architecture is experimentally validated in Section VI.

II. SYSTEM ARCHITECTURE

The proposed system architecture is shown in Figure 1, and is composed of a network of nodes, each one carrying out a specific task depending on its type. Control nodes, denoted by the orange colour, and grouped in a larger, optionally redundant control cluster, are responsible for the calculation of the control actions needed to achieve the desired result. These communicate directly with the HMI, running on either the end-user computer, or on a dedicated machine, through a standard Ethernet link, through which the desired set-points and run-time parameters are set up. For fault tolerance, the individual nodes can be grouped in redundant pairs or groups, where multiple nodes are running in parallel/lockstep mode. Horizontal scaling is achieved by partitioning the network (either at the physical or logical layer) and assigning a redundant group to each sub-section. The sensing nodes, shown in green, are tasked with sensor signal conditioning. For better flexibility, these can be either connected to the control cluster through direct analogue links, for small or cost sensitive reasons, or preferably they can also perform the ADC conversion and be integrated in the digital control network, allowing effortless sharing of the data with multiple control nodes. Finally, the power nodes, depicted in blue, are the element that physically perform the control actions, each one of them is connected with a digital link to the control cluster, fully capable of supporting low latency real-time operations.
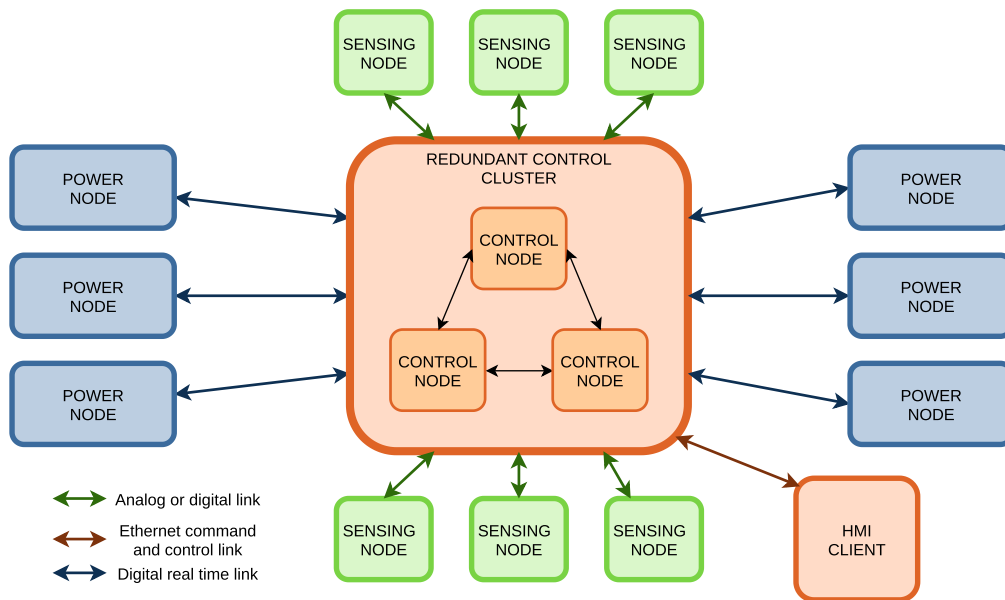
FIGURE 1. Diagram of the proposed Architecture.

From a topology perspective, the flexibility afforded by the digital control coupled with a modulator implementation local to each cell decouples the choice of basic power cell circuit from the overall converter design. Consequently, depending on the system requirements, like DC-link voltage and target switching frequency, different circuits can be used; from a basic half bridge, as used for the experimental results in this paper, to more complex multilevel topologies. It should be noted that the diagram shown in figure 1 shows a six phase system for clarity, because this constitutes the most complete possible configuration, that can be scaled to very large systems. When different requirements allow it, the complexity, and consequently cost, of the system can be reduced by combining multiple functions in a single node. As an example, the analogue sensing and power conversion functions can be combined in a single node, thanks to the versatility of the designed communication protocol. Control node redundancy can also be dropped, to reduce costs and complexity when the reliability of a single node is evaluated to be sufficient to meet the desired requirements.

III. COMMUNICATIONS

While many communication protocols are used in power electronics systems, these are usually primarily designed for other roles, like industrial automation with Modbus and automotive vehicle control in the case of CAN. These, certainly suitable for a monolithic converter, have serious downsides for distributed and fault tolerant systems. The bus topology, while minimizing cabling cost and complexity, is vulnerable to failures, as a single malfunctioning node can bring down the entire network, requiring either a complete replication of the entire network by as many times as fault to be handled, or a substantial increase in complexity with the addition of non-standard compliant partitioning and switching in order to
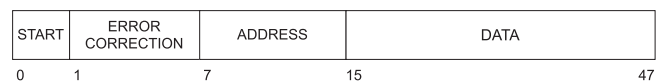

FIGURE 2. Developed protocol message.

cut out damaged sections of line. The real time performance of these standard protocols is also non-ideal, with real world latencies in the range of 10 to $100\,\mu s$ [16].

To address these challenges, a custom communication protocol was introduced, with a primary design focus on low latency fault tolerance. At the physical layer, the network is composed of serial, media independent, point-to-point links. This provides the system greater fault isolation, as a single link failure will not affect the health status of the entire network.

From a logical perspective each message in the developed protocol consists of a fixed structure packet, shown in Figure 2, composed of a header containing a start bit and error correction information with both parity for the data and a global checksum. These are followed by a 40 b payload field, that is conventionally partitioned in a single byte address denoting the message function and a 4 B message data field.

On the data-link layer both star and hierarchical tree topologies are supported, depending on the network size, with the former being more tolerant to failures, while the latter allows much better scaling, as it does not require the central node to have as many IO interfaces as nodes in the network. It should be noted that to avoid the introduction of single points of failure redundancy needs to be considered for the routers, sitting between control cluster and end-nodes.

The small packet size, while somewhat hurting transfer efficiency keeps latency at a minimum, while still allowing a
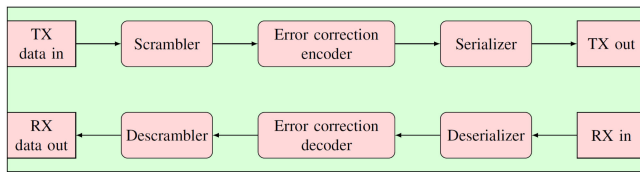
FIGURE 3. Diagram of the overall communication chain.

FIGURE 4. Hardware configuration used for this paper.

complete 32 b word transfer with each message. To guarantee reception an optional acknowledge can be sent back to the sender, allowing the assessment of link health. A periodic automatic heartbeat message is sent by a watchdog timer to guarantee am upper bound in the fault detection time. To decrease its impact on channel capacity and transmission latency the counter is reset after a successful message exchange, making this aspect completely transparent during nominal use.

The overall structure of the transmission and reception chains are shown in Figure 3. A transmission starts with multiplicative scrambling of the message payload, that is feed to the error correction encoder which adds parity and checksum information. A serializer is then used to push the data over the channel. Upon reception the packet will go through the inverse process, with a de-serializing, decoding and de-scrambling. Resulting in the original message being passed to the downstream logic.

A. SYNCHRONIZATION

Two separate solutions are available to achieve clock synchronization between nodes, the use of a clock distribution network and clock recovery. For small systems with few nodes, the first choice is used and preferred, as costs are usually comparable with the latter while allowing for a much lower complexity receiver. In this case a clock signal is generated in the central controller and passed either electrically or optically to all the other nodes in the system. The narrow pass-band characteristic of the signal, coupled with the known and stable frequency allows the use of very high quality factor filters, to reject EM interference even in very noisy environments. When this technique is chosen, the scrambling/descrambling steps can be bypassed as they are not strictly needed. As the size of the system grows, there will be a point where the cost and complexity of distributing a clock signal to dozens or even hundreds of nodes become too large. In these cases, the clock can be recovered directly from the incoming bit stream, provided a large enough density of transitions is present. In this case a hardware Phase Locked loop is locked to the incoming data stream, thus recovering the transmitter clock. The two techniques can even be present in a single system, to better adapt to the physical characteristics of each channel. For a hierarchical tree topology network, where the main controller is linked only with tier two routers, which are in turn connected to the power nodes, explicit clock distribution can be used for the small number of high speed links while clock recovery is used for the other role or vice versa.
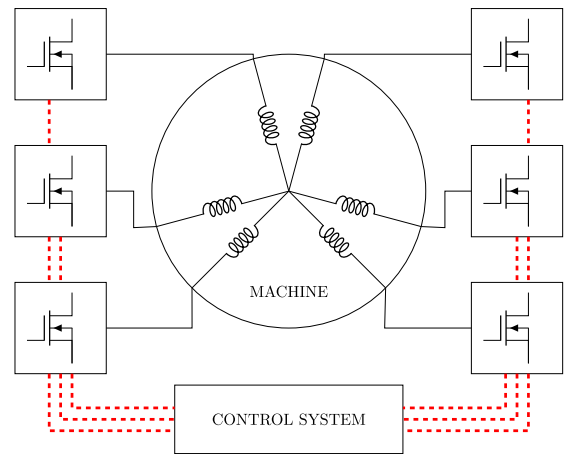
B. ERROR HANDLING

Error handling is a very important area of a communication protocol design that can greatly impact system performance. The traditional approach of error detection and message retransmission can deal with numerous random errors while having minimal impact on the transmission efficiency during nominal operation. The downside of this process is the introduction of a large amount of jitter when a packet needs to be retransmitted, potentially leading to control instability or deadline violations [17]. An alternative strategy, adopted in the designed protocol, is the use of Forward Error Correction (FEC), where enough redundancy is added to the bit stream to enable the receiver to mathematically reconstruct the original bit pattern, completely avoiding the need for retransmission. The main downside of these techniques is the limited number of correctable bits, requiring the designer to evaluate the error probability on the expected channel, allowing the addition of enough redundancy to reduce the probability of an undetected and uncorrected error to acceptable levels. To address this weakness, two error correction techniques can be chosen for the developed protocol, depending on the expected bit error probability. A Hamming single error correction, double error detection (SECDED) code is used for reliable channels, where the probability of more than two errors is small. While a Reed-Solomon code can be used (RS(15,11)) capable of correcting up to 2 symbols, with each symbol containing 4 consecutive bits can be used when operating on a worse channel.

IV. HARDWARE AND FAULT TOLERANCE
A. HARDWARE

The hardware configuration that is used in this paper to evaluate the proposed system architecture, as shown in Fig. 4, consists of a multiphase fault tolerant electric drive. The driven machine, is a six phase asymmetrical permanent magnet synchronous machine, where the stator is composed by two star-connected three-phase winding sets, having a displacement angle of 30° between them, and a common neutral. Each one of the coils is driven by its own power cell, consisting of a

half bridge inverter leg. A central node implements the current control system, with the communication protocol presented in the previous section, linking it to the power nodes. Given the small size of the entire system, the analogue output of the current and rotor position sensing nodes is directly connected to the control system. It should be noted that, while for experimental reasons only this specific configuration is examined, the proposed system architecture is completely general and can be easily adapted to any digitally controlled static power conversion system.

From a control system perspective, even though a monolithic block is shown in the diagram, it could be partitioned in multiple sub units, each one responsible of controlling the current in only a sub-set of phases, thanks to the independence of current regulators between each phases, that only need information relative to the controlled winding to function.This grants an additional degree of freedom to the system architect, especially when dealing with large systems. As it avoids the need for any interconnection between control units, which would be critical from both a performance and a reliability perspective.

B. FAULT TOLERANCE

The first step in the evaluation of a system architecture fault tolerance, is the study of the possible failure modes it can be affected from. The power section in a machine drive can suffer from short circuits, open circuits and loss of supply. The control system on the other hand can suffer from logic faults due to external effects like cosmic radiations, loss of supply, or communication failure, in case of a distributed architecture. Lastly, external sensors can also be lost, or return corrupted reading.

In the system considered in this paper, open or short circuits in the machine, cable, or power nodes, can be addressed by excluding the affected portion of the system, either at the controller level, when sufficient control authority is retained, or through external isolation devices, like fuses, contactors or thyristors. The fault tolerant current control algorithm will than reconfigure the references for the healthy phases to minimize post-fault operation disruption. It should be noted that there are specific fault conditions, like a short circuit between the machine neutral point and the system ground, where the whole system needs to be shut down to avoid potential shock hazards. The loss of supply events are another class of events that are not directly handleable by the system shown in Fig 4, due to the lack of an alternative power source. From a high level perspective however, the architecture delineated in Section II can handle any power system failure, thanks to its distributed nature, provided that enough redundancy is present in the hardware itself.

A problem that can affect distributed control architectures, is the loss of communication, which can cut off the power nodes form the centralized control system. The designed architecture can respond to this challenge by either continue operating by switching to a spare communication link, if some
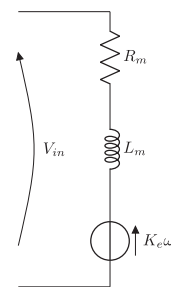

FIGURE 5. Machine phase equivalent circuit.

degree of redundancy is present. If only a single communication link is available, the entire power node is considered inoperable, triggering a reconfiguration of the remaining portion of the system, to work without the affected phase. Another issue that can plague static converters in general, and machine drive systems in particular, is sensor failure. Two scenarios are possible for these components. The first, complete disconnection, is easily detectable, both for analogue or digital links. While the second, inaccurate reading communicated by the sensor itself, can be detected through specific algorithms [18]. Finally, the control system itself can become inoperable, occurrence that is prevented through redundancy.

V. CURRENT CONTROL
A. MACHINE MODELLING

The standard machine modelling techniques, using the rotating reference frame with *d* and *q* axes, can not be applied as the whole control is performed in the *abc* space. An additional challenge, not normally present with more traditional architectures, is the fact that the frequency of the current, and consequently the rotational speed, is not a constant but one of the controller inputs, leading to a Multiple Inputs Single Output characteristic.

The starting point to derive a plant model that is compatible with the aforementioned constraints was the RLE equivalent circuit of a machine phase, shown in Fig. 5. This was coupled with mechanical inertia and torque-power relationships, forming the system of equations shown in (1).

$$\begin{cases} V_{ph} = (R_{ph} + sL_{ph})I_{ph} + K_e\omega_e \\ \omega_e = \frac{P_E}{T_E} = \frac{V_{ph}I_{ph}}{T_E} \\ T_E = T_A + T_L = J\alpha_m + T_L = J\frac{d\omega_m}{dt} + T_L \end{cases} \quad (1)$$

While the process to extract a suitable plant transfer matrix is fairly straightforward, few simplifying assumptions have been considered. Machine losses have been neglected, making electrical and mechanical power equivalent; unity power factor was also considered. These factors, while decreasing the absolute accuracy of the mathematical model, do not fundamentally change the behaviour of the plant as seen by the controller, especially when considering its stability. Even with these assumptions in place the Back-emf term still needs some processing, as it is still non-linear. In fact, the plant has one of the two input, the angular speed, in the denominator while
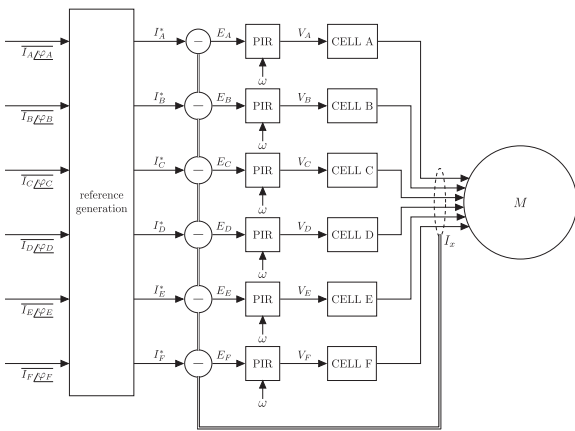
FIGURE 6. System level control architecture.

FIGURE 7. PIR controller diagram.

the other, the current, is directly multiplied by the output, the voltage. To deal with these challenges this factor has been linearized around the (V_0, I_0) equilibrium point by using a first order Taylor series approximation, leading to equation (2).

$$V_{BEMF} = K_e V_{ph} I_{ph} g(x) \longrightarrow K_e \nabla (V_{ph} I_{ph} g(x))$$
$$= K_e(\dot{V}_{ph} I_0 g(0) + V_0 \dot{I}_{ph} g(0) + V_0 I_0 \dot{g}(x)) \quad (2)$$

where

$$g(x) = \frac{1}{J\alpha_e \frac{2}{n_p} + T_L} \longrightarrow \frac{1}{T_L} - \frac{J\frac{2}{n_p}\alpha_e}{T_L^2} \quad (3)$$

Finally, combining (1), (2) and (3) together leads to an equation in two variable associated to the MISO system that needs to be controlled. From this the extraction of a transfer matrix, shown in (4) is relatively straightforward.

$$I = \begin{bmatrix} \frac{1 - I_0 \frac{K_e\eta}{T_L}}{R_{ph} + sL_{ph} + V_0 \frac{K_e\eta}{T_L}} & \frac{J\frac{2}{n_p}s}{T_L(R_{ph} + sL_{ph} + \frac{V_0}{T_L})} \end{bmatrix} \begin{bmatrix} V_{IN} \\ \omega_e \end{bmatrix} \quad (4)$$

B. CURRENT CONTROL

1) OVERVIEW

While current control is not strictly the focus of this paper, it is still fundamental for fault tolerant operation, the current control system must be able to position each current vector independently of the others. This decouples torque control, that is inherently linked to the machine structure, and health state of the system, from each single phase current control, which can be effectively performed by each phase power cell independently, as long as they form a balanced set, whose sum is zero, to respect Kirchhoff's current law at the isolated machine neutral point.

To achieve this goal, the current controllers themselves must be moved from the $d - q$ or VSD space, back to the regular *abc* space, as shown in the system diagram in Fig. 6, where there is a one to one correspondence between controller and physical machine phase.

To allow the control to happen in a static frame an appropriate set current of references must be generated capable of
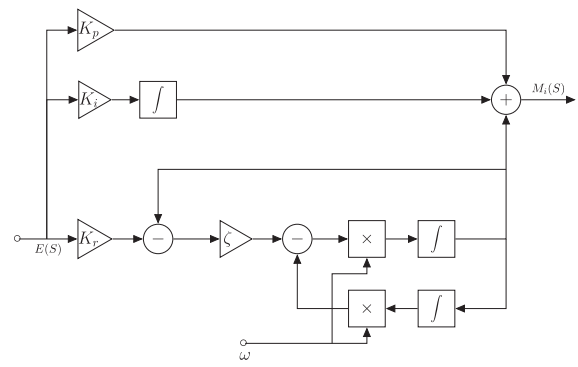
delivering the current required by the upstream speed controller. A bank of direct-quadrature sinusoidal generators is used to perform this task, while at the same time allowing the use of the field weakening region of operation on machines that support it. The phase angle of each current is chosen depending on the machine layout and the state of health of the system [19], [20]. A set of multiplicative coefficients is also used to individually adjust the amplitude of each current with respect to the requested value, in order to compensate for the lack of torque from one or more windings in a post-fault scenario.

In case of fault, the ensuing disturbance will affect all controllers equally and only as long as the references remain unchanged. As opposed in a more traditional architecture where the controllers are placed in a transformed vector space where not all controllers might be affected, leading to a much more problematic unbalance.

The most difficult aspect of performing the control in a static frame is the need to track a sinusoidal reference. The technique most widely used for current control, PI regulation, has been used for static reference frame fault tolerant control of machine phase currents [21], however it can struggle with steady state error, making it not ideally suited for this application. To help counteract this problem, the use of a per phase vector space transformation have been proposed [22], allowing PI controllers to be used in this application, at the expense of higher complexity of the implementation, requiring two controllers and four transformation steps for each phase. Another technique, which has been chosen for this paper, that can be suited for static reference frame control consists in the use of resonant controllers. This has been widely explored for various applications, both in grid connected applications [23] in motor control [24], [25]. In addition to the classical Proportional Resonant (PR) controller an integral term is used in this work (PIR controller), shown in Fig. 7; this adds DC gain, removing any steady state offsets, rejecting disturbances, and facilitating machine alignment and startup where DC currents need to be injected. PIR extends the regular PI controller with a resonant element, the Second Order Generalized Integrator (SOGI), which guarantees some amount of gain, up to infinite, depending on the implementation. This allows the tracking

of a sinusoidal signal at a specific frequency through the introduction of two complex conjugate poles at the desired frequency.

2) CONTROLLER DESIGN

The PIR controller, whose transfer function is shown in (5), while having a fixed structure, needs to be tuned to achieve both stability and desired performance.

$$PIR(s) = K_p + K_r \frac{\omega \zeta s}{s^2 + \omega \zeta s + \omega^2} + \frac{K_i}{s} \tag{5}$$

Several methods have been used to this effect, from a modified version of the popular Ziegler-Nichols heuristic [26], to optimal tuning or PR controllers based on the target machine model [27], to optimal LQR based control techniques [28], to global optimizations based on genetic algorithms [29]. Most of these methods rely however on an extremely precise model of the plant, as it is crucial in the whole tuning process, and poorly handle disturbances, which can result in instability under non-ideal conditions. To address these issues the several techniques have been introduced in the field of robust controls, that aim to analyse and synthesize controllers in presence of disturbances of model uncertainty, to maximize stability and evaluate their impact on the closed loop system performance.

H_∞ control theory in particular has been used to both analyze power electronics systems [30], synthesize [5] or tune controllers [31], [32] The μ-synthesis [33] approach based on structured singular values (SSV) allows to tune a fixed structure controller through H_∞ methods to achieve a final set of parameters that can minimize the effects of disturbances, such as model uncertainty or external noise on the closed loop performance. The method employed to tune a fixed structure controller to minimize the impact of disturbances is called D-K Iteration, presented in [34]. In the fist step of this iterative process, a regular H_∞ synthesis is used to tune the controller, following the method delineated in [35], minimizing the overall gain of the system.

Then the robust performance of the system is evaluated, obtaining a scaled norm, this is the D step. Subsequently, in the K step, a new synthesis is performed minimizing this norm. These two steps are then repeated until a desired convergence criterion is met.

In order to guide the synthesis process toward the desired system behaviour, a set of weight functions are selected and applied to the inputs (W_i for the current set-point and W_w for the angular velocity), to the outputs (W_o) and to the control variables (W_v for the voltage); in a process called H_∞ loop shaping. Creating a set of virtual outputs, four in this case, only used during the controller synthesis process. The only constraints placed to the optimization process used for these steps, are upper and lower bounds for the tuned parameters, to speed up the computational process by limiting the search space and ensure a solution with reasonable values (neither too small nor too large) to avoid potential numerical problems.

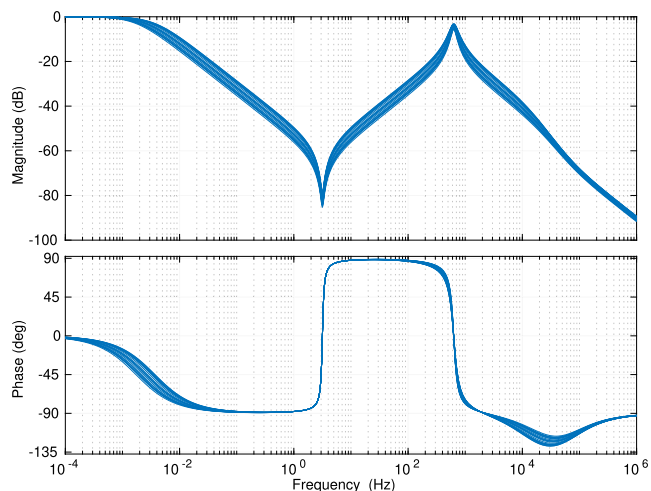An advantage of the chosen tuning method is the ability to take into account and quantify the effects of modeling

FIGURE 8. Closed loop transfer function from set-point to output current of the uncertain system.

TABLE 1 Controller Parameters

parameter	value
K_p	0.8
K_i	0.5
K_r	1000
ζ	0.0591

uncertainties on the system closed loop transfer function. To this effect, a $\pm 30\%$ uncertainty range was defined for both moment of inertia and rotor magnet flux linkage as direct measurement of these quantities is not often practical. The results of the tuning procedures are shown in the bode diagrams in Fig. 8, where each one of the multiple lines corresponds to a specific set of values for the aforementioned properties, within the specified variability range. This can help visualize the effect of model uncertainties on the controllers response.

The exact controller gain values obtained through this process, used in the experimental section are shown in Table 1. The first two coefficient represent the proportional and integral term gains, also present in the traditional PI controllers, with the same stability and performance consideration applying to both regulator structures. The K_r gain regulates the strength of the resonant action, and constitutes a fundamental contribution to a control system in a static reference frame, as it greatly reduces the steady state tracking error typical of PI regulators when tracking sinusoidal signals. Finally ζ is a damping coefficient that, while not strictly necessary, is very often added to limit the resonant gain of the controller that would otherwise be infinite, making the implementation of the controller numerically challenging. The value of this parameter, consequently defines width and height of the peak in the transfer function at the resonant frequency.

3) FAULT MODE OPERATION

While the proposed architecture is able to gracefully handle failure of one or more phases without immediate stability

challenges, it is still desirable to perform fault detection, which is now fairly insensitive to delay, and it can be done through one of the many approaches published in literature [36], [37]. In order to minimize performance loss, the drive operation should then be reconfigured to achieve optimal performance. In the case of the proposed architecture, this operation is extremely simple, and can be easily performed online. It only consists in a simple reference signal change, to produce the new set of sinusoidal references, thanks to the controller ability track arbitrary current phasors.

First and foremost, it is important to determine the type of fault experienced by the system. Without delving into excessive detail two large classes can be easily identified, open and short circuit faults. From a drive operating perspective, these two must be treated differently. To deal with short circuit faults, the affected part of the system needs to be isolated, in order to interrupt the flow of current, transitioning to a more easily dealt with open type fault. Several techniques have been proposed to do so [38], [39], and they fall broadly in two groups, active, where thyristors or relays are used to open the affected path, or passive, where fuses are added to the circuit and react to the current spike following the short. In case of an open circuit fault, either direct, or induced, the offending phase is completely cut off making it unable to generate torque, while the rest of the system is unaffected, making it possible, for multiphase machines, to carry on working.

To achieve optimal post fault behaviour the remaining phases current vectors should be reconfigured to still generate a smooth rotating MMF. The easiest way to calculate the phase angles needed by the reference signal generators in hardware, is by using a Vector Space Decomposition (VSD) approach as shown in [19], [20], optimization the resulting set of phasors to either minimize stator losses or maximize the produced torque.

C. STABILITY ANALYSIS

To prove stability of the proposed architecture, in both pre- and post-fault configurations, stability analysis needs to be performed, to mathematically guarantee that the system is well-behaved in all situation. While several tools can be utilized to this effect, the choice was made to use a state-space approach due to its simplicity, especially for higher order models. As a fist step in its derivation process the dynamics of the complete system need to be described with one or more differential equations. This can be done by equating the voltage at each machine terminal phase with the controller output, considering also the interactions between different phases given by mutual inductance, as shown in equation (6) where I_s is the current in the examined phase, while I_x is the one in the others, L is the winding self inductance, while $M_{s,x}$ is the mutual inductance to the other relevant winding and V_B is the Back-EMF voltage. This last term will be processed similarly to when extracting the machine transfer function, with the only difference being that the angular speed can be considered constant, for this analysis that is aimed strictly

electrical domain phenomena.

$$\left(K_p + K_r \frac{\zeta \omega' s}{s^2 + \zeta \omega' s + \omega^2} + \frac{K_i}{s}\right)(I_s^* - I_s)$$
$$= RI_s + sLI_s + sM_{s,x}I_x + V_B \qquad (6)$$

$$X = \begin{bmatrix} I_x \\ \dot{I}_x \\ \ddot{I}_x \\ \dddot{I}_x \\ \ddddot{I}_x \end{bmatrix} \qquad U = \begin{bmatrix} I_x^* \\ \dot{I}_x^* \\ \ddot{I}_x^* \\ \dddot{I}_x^* \\ \ddddot{I}_x^* \end{bmatrix} \qquad (7)$$

After elimination of the denominator from the left-hand side and expansion/collection of all relevant terms, an Ordinary Differential Equation (ODE) with several fourth order terms. The state and input vector choice is shown in equation (7) where I_x represent a vector of the six phase currents and I_x^* is a vector of the six current references. A state space model for the nominal system can now be extracted and is shown in equations (8) to (18) where the overlined quantities define the relevant 6x6 matrix (ie. $\bar{R}$ for Resistance, $\bar{L}$ for inductances, etc.)

$$A = \begin{bmatrix} 0 & I(6) & 0 & 0 & 0 \\ 0 & 0 & I(6) & 0 & 0 \\ 0 & 0 & 0 & I(6) & 0 \\ (K_i/\bar{L}_n)I(6) & A_2 & A_3 & A_4 & A_5 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \qquad (8)$$

$$A_2 = \left(\frac{K_p + \bar{R}}{\bar{L}_n}\omega^2 + \frac{K_i}{\bar{L}_n}\zeta\omega + \frac{K_e V_0 \omega^2}{\bar{L}_n T_L}\right) \cdot I(6) \qquad (9)$$

$$A_3 = \left(\frac{K_p + K_r + \bar{R}}{\bar{L}_n}\omega\zeta + \frac{K_i}{\bar{L}_n} + \omega^2 + \frac{K_e V_0 \omega \zeta}{T_L \bar{L}_n}\right) \cdot I(6)$$
$$+ \left(-\frac{M_{n,m}}{\bar{L}_n}\omega^2\right) \cdot [J(6) - I(6)] \qquad (10)$$

$$A_4 = \left(\frac{K_p + \bar{R}}{\bar{L}_n} + \omega\zeta + \frac{K_e V_0}{T_L \bar{L}_n}\right) \cdot I(6)$$
$$+ \left(\frac{M_{n,m}}{\bar{L}_n}\omega\zeta\right) \cdot [J(6) - I(6)] \qquad (11)$$

$$A_5 = \frac{\bar{M}_{n,m}}{\bar{L}_n}\omega\zeta[J(6) - I(6)] \qquad (12)$$

$$B = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ B_1 & B_2 & B_3 & B_4 \\ 0 & 0 & 0 & 0 \end{bmatrix} \qquad (13)$$

$$B_1 = \frac{K_i}{\bar{L}_n}\omega^2 I(6) \qquad (14)$$

$$B_2 = \left(\frac{K_p}{\bar{L}_n}\omega^2 + \frac{K_i}{\bar{L}_n}\zeta\omega\right) I(6) \qquad (15)$$
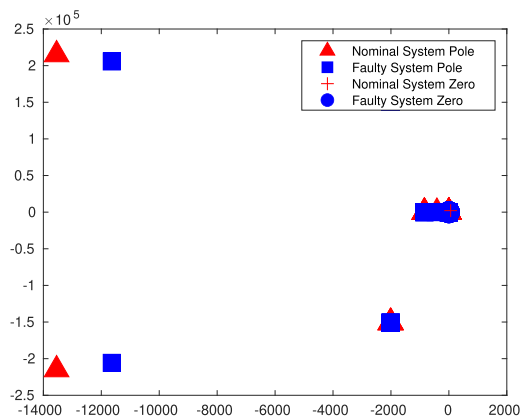
FIGURE 9. Pole zero map of the current control system in both pre (blue marks) and post (orange marks) fault scenarios.

$$B_3 = \left(\frac{K_p + K_r}{\bar{L}_n} \omega\zeta + \frac{K_i}{\bar{L}_n} \right) I(6) \tag{16}$$

$$B_4 = \frac{K_p}{\bar{L}_n} I(6) \tag{17}$$

$$C = [111100\ldots0] \quad D = [0\ldots0] \tag{18}$$

The stability analysis, once the system behaviour is described with this representation can be easily guaranteed through analysis of the eigenvalues of the A matrix, that corresponding with the poles of the system, must have zero or negative real part. To then re-asses stability of the system in a post open circuit fault state, it is sufficient to zero out all the components of the A matrix related to the faulty phase, as the fault cause all current flow to stop. The eigenvalues of this new model can be inspected to prove stability even in this configuration. The results of these two analyses are shown in the pole-zero map at Fig. 9. And while, as expected poles and zeros move between the two configurations, stability is still guaranteed.

VI. EXPERIMENTAL RESULTS

A. COMMUNICATION PROTOCOL

Before proceeding with full scale system testing, the designed communication protocol is been experimentally characterized. To measure the additional end-to-end latency, a physical loopback optical fibre is used, connecting transmitter and receiver, both implemented in the same FPGA fabric. Additional infrastructure is inserted alongside the regular communication logic to support the measurements. All tests are run with a system clock frequency of 100 MHz, and optical transceivers with a 40 MHz bandwidth.

To measure the latency associated with the designed communication protocol a simple counter is started by the packet generator as a new transmission is requested, and stopped when the receiver makes the data available to downstream logic.

The results of the test are shown in Table 2, where the first column shows the utilized forward error correction (FEC)

TABLE 2 Latency Test Results

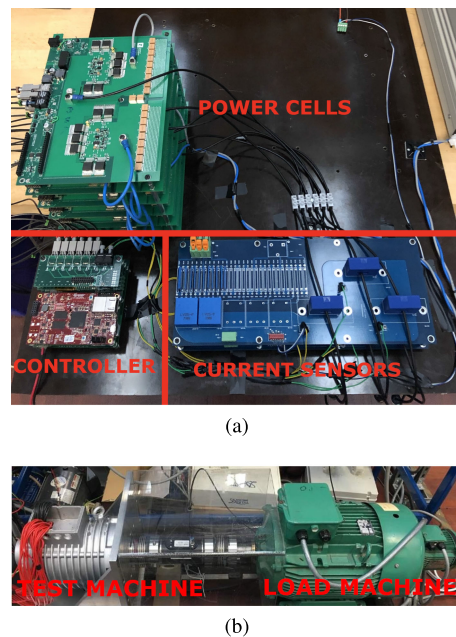| FEC Technique		Absolute Latency	Added latency
None	TX	460 ns	910 ns
	RX	450 ns	
Hamming	TX	540 ns	1.11 µs
	RX	570 ns	
Reed Solomon	TX	750 ns	1.82 µs
	RX	1070 ns	

(a)

(b)

FIGURE 10. Converter (a) and machine(b) setup pictures.

technique, while the subsequent ones show: the absolute amount of latency added by the transmission and reception steps and the total end to end latency. When forward error correction is not needed, namely when an optical physical medium is used, the total amount of latency added to a communication is 910 µs. If some error correction is desired, like when part of the wiring run consists of electrical cabling, the hamming SECDED method can be used with a minimal amount of added latency while still being able to correct single bit errors and detect two bit ones. When heavy interference is expected, the Reed-Solomon error correction algorithm can be employed, allowing the correction of a much longer error sequence, at the cost of a significantly higher added latency. It should be noted that due to the short cabling run typical of power electronics application these latencies are dominated by the transmission time, which is limited by the channel bandwidth, as opposed to the signal phase or group delay.

B. COMPLETE SYSTEM

In order to validate performance, the proposed architecture has been prototyped and a setup built for experimental validation. The distributed drive, shown in Fig. 10(a), was assembled by six identical power cells, each one consisting of a single PCB. From a topology perspective, each power cell
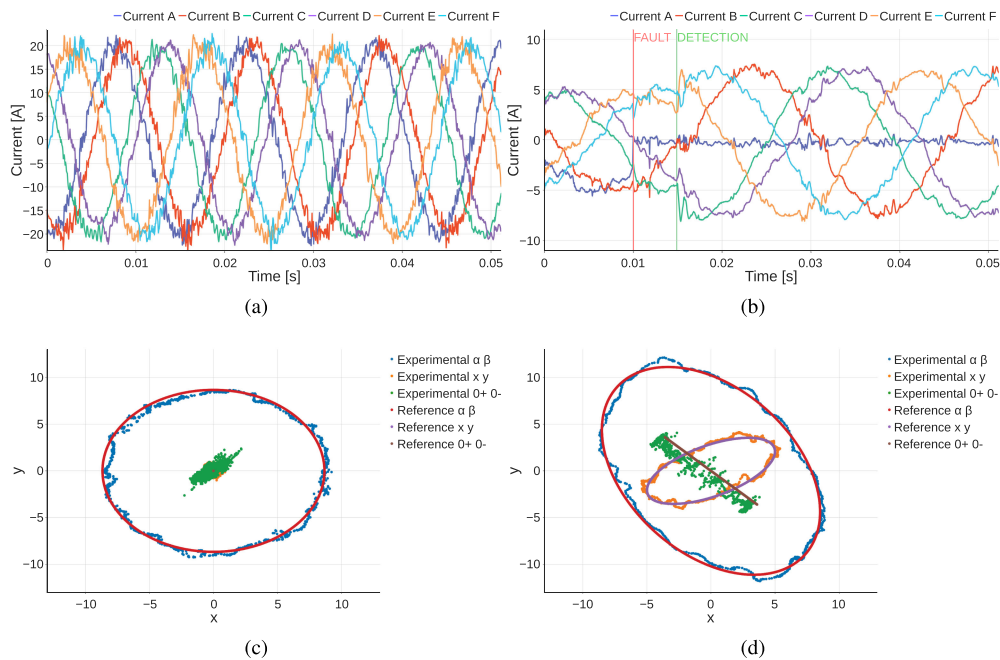
FIGURE 11. Experimental current captures: time plots in nominal operation (a) and during the fault transition (b), as well as VSD space trajectories in pre (c) and post (d) fault state, along with relative references.

TABLE 3 Experimental Setup Parameters

parameter	value
Motor rated Power	18 kW
stator inductance	0.125 mH
stator resistance	8.5 mΩ
flux linkage	0.0923 Wb
pole pairs	4
Rated speed (test rig limited)	1500 rpm
Rated current	50 A
Switching frequency	60 kHz
DC link voltage	270 V

contains two switch clusters connected to form a two level half bridge. While more advanced cell designs, like multi-level arrangements (i.e. NPC or flying capacitor) are possible, the chosen one still allows achieving sufficient performance while keeping complexity to a minimum; especially when coupled with the high operating frequencies that can be reached by wide bandgap semiconductors. A Maximum allowable DC link voltage of 600 V was considered for the design, making 900 V class Silicon Carbide MOSFETs (Wolfspeed C3M0065090), a good trade-off between safety margin and performance. A Switching frequency of 60 kHz was chosen as a compromise between output current quality and efficiency, in terms of switching losses. A small FPGA (Xilinx XC7S61FTGB196) was used to implement the communication protocol receiver, as well as the PWM modulator responsible for the generation of the various required gate signals.

A single centralized main controller, used for simplicity, handled current control, as well as sensor acquisition. A resolver, paired with a monolithic Resolver to Digital Chip (AD2S1210) sampled both shaft angle, and true mechanical speed. The output currents are sensed for feedback through closed loop hall effect sensors (LEM LA55P-SP1), digitized simultaneously with six 14 b ADC (LTC2313-14) at 240 kSps and finally down-sampled to 60 kHz. The controlled machine, was mounted on a machine test rig, and coupled with an induction machine, as shown in Fig. 10(b). The main parameters of the whole experimental setup are shown in Table 3.

All tests have been conducted with the load machine spinning and maintaining a constant speed through the test rig drive system, while the controlled machine followed the desired current profile, producing torque, in the motoring mode. For all tests the machine currents have been captured and saved directly after ADC conversion at the higher sample rate, before downsampling.

The first test, whose results are shown in Fig. 11(a), consisted in a simple capture of the steady state current waveform, when the complete system is running in its healthy configuration. here the system performed in line with expectations, and while some noise is present in the graphs, this is caused to poor signal to noise ratio in the current sensing and digitization circuitry, due to the drive having a much larger current rating than the machine. The harmonic distorison on the other hand is acceptable, falling in the range of 2.5% to 3%,. This is also highlighted from the load step test, whose results are shown in Fig. 12, where the current does not increase when going from 5 A to 20 A.

The next test carried out is a fault simulation, specifically designed to show the fault tolerant potential of the proposed architecture. The type of fault chosen is the single phase open circuit that could be caused by issues in either machine,
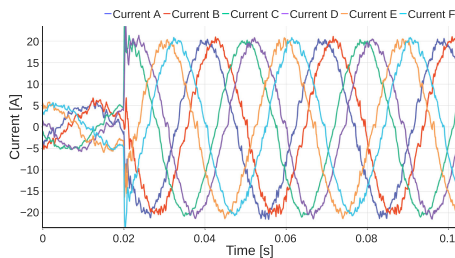
FIGURE 12. Experimental current waveforms during a Load Step.

drive or interconnecting cables. To be able to repeat the test safely, reliably and without risk of damage to the experimental equipment an emulated fault was injected into one of the otherwise healty power nodes. To do so, one of the six phases was completely turned off, asynchronously with respect to the control, in order to cut the current to zero in the most realistic way possible. After a 5 ms wait, representing the delay of a real world, software implemented, fault detection algorithm, the references are reconfigured, with all other controller and test parameter remaining equal. As shown in Fig. 11(b), faulty phase currents immediately drops to zero, while the others, show close to no impact. Showing no sign of oscillation or instability. After the reference reconfiguration, the remaining phases start following the new reference without any additional problems.

To assess the dynamic performance of the proposed control strategy, a load step test was performed with amplitude 20 A. From the analysis of the current waveforms, shown in Fig. 11(b), a current rise of about 300 μs can be measured. In order to judge the quality of the control system tracking in both healthy and faulty running modes, the captured data, is plotted in the VSD space in Fig. 11(c) and 11(d) along with the commanded references. These show excellent tracking performance in both scenarios. It should be noted that, in contrast with other control methods proposed in literature [40], when running in five phases mode the currents in all the VSD space sub-planes are actively controlled and can achieve adequate tracking of the required references, all the while still retaining passive fault tolerance, as no controller changeover is needed.

VII. CONCLUSIONS

This paper proposes a novel system architecture able to achieve scalable and fault tolerant operation in multi-phase machine drive systems. The presented demonstrator platform confirmed the potentiality of the suggested comprehensive approach to system design. Scalability is guaranteed by the modular, fully digital, distributed and networked design, which greatly simplifies system extension and reconfiguration. A proof-of-concept setup showed that the proposed architecture allows fault tolerant operation in a six-phase electric machine with independent current control, the custom digital communication protocol developed to allow distributed close loop controls was tested, showing minimal added latency, even when implementing Reed-Solomon forward error correction.

The control system demonstrated good tracking performance of the requested reference both during the normal and post-fault operation regimes. A fault transient test helped highlight the correct behaviour of the system, even during this challenging event, with the currents always under control.

REFERENCES

[1] Z. Jin, G. Sulligoi, R. Cuzner, L. Meng, J. C. Vasquez, and J. M. Guerrero, "Next-generation shipboard dc power system: Introduction smart grid and dc microgrid technologies into maritime electrical netowrks," *IEEE Electrific. Mag.*, vol. 4, no. 2, pp. 45–57, Jun. 2016, doi: 10.1109/MELE.2016.2544203.

[2] J. Harikumaran *et al.*, "Failure modes and reliability oriented system design for aerospace power electronic converters," *IEEE Open J. Ind. Electron. Soc.*, vol. 2, pp. 53–64, 2021, doi: 10.1109/OJIES.2020.3047201.

[3] G. Buticchi, S. Bozhko, M. Liserre, P. Wheeler, and K. Al-Haddad, "On-board microgrids for the more electric aircraft-technology review," *IEEE Trans. Ind. Electron.*, vol. 66, no. 7, pp. 5588–5599, Jul. 2019, doi: 10.1109/TIE.2018.2881951.

[4] Y. Demir and M. Aydin, "A novel dual three-phase permanent magnet synchronous motor with asymmetric stator winding," *IEEE Trans. Magn.*, vol. 52, no. 7, pp. 1–5, Jul. 2016, doi: 10.1109/TMAG.2016.2524027.

[5] G. Zhang, W. Hua, and P. Han, "Quantitative evaluation of the topologies and electromagnetic performances of dual-three-phase flux-switching machines," *IEEE Trans. Ind. Electron.*, vol. 65, no. 11, pp. 9157–9167, Nov. 2018, doi: 10.1109/TIE.2018.2808908.

[6] T. Zhao, S. Wu, and S. Cui, "Multiphase PMSM with asymmetric windings for more electric aircraft," *IEEE Trans. Transport. Electrific.*, vol. 6, no. 4, pp. 1592–1602, Dec. 2020, doi: 10.1109/TTE.2020.2997609.

[7] Q. Chen, G. Liu, W. Gong, and W. Zhao, "A new fault-tolerant permanent-magnet machine for electric vehicle applications," *IEEE Trans. Magn.*, vol. 47, no. 10, pp. 4183–4186, Oct. 2011, doi: 10.1109/TMAG.2011.2146238.

[8] M. Popescu, D. G. Dorrell, L. Alberti, N. Bianchi, D. A. Staton, and D. Hawkins, "Thermal analysis of duplex three-phase induction motor under fault operating conditions," *IEEE Trans. Ind. Appl.*, vol. 49,, no. 4, pp. 1523–1530, Jul./Aug. 2013, doi: 10.1109/TIA.2013.2258392.

[9] N. Bianchi, E. Fornasiero, and S. Bolognani, "Thermal analysis of a five-phase motor under faulty operations," *IEEE Trans. Ind. Appl.*, vol. 49, no. 4, pp. 1531–1538, Jul./Aug. 2013, doi: 10.1109/TIA.2013.2258452.

[10] A. Galassini, A. Costabeber, C. Gerada, G. Buticchi, and D. Barater, "A modular speed-drooped system for high reliability integrated modular motor drives," *IEEE Trans. Ind. Appl.*, vol. 52, no. 4, pp. 3124–3132, Jul./Aug. 2016, doi: 10.1109/TIA.2016.2540608.

[11] S. Rubino, R. Bojoi, A. Cavagnino, and S. Vaschetto, "Asymmetrical twelve-phase induction starter/generator for more electric engine in aircraft," in *Proc. IEEE Energy Convers. Congr. Expo.*, pp. 2016, 1–8, doi: 10.1109/ECCE.2016.7854889.

[12] W. Cao, B. C. Mecrow, G. J. Atkinson, J. W. Bennett, and D. J. Atkinson, "Overview of electric motor technologies used for more electric aircraft (MEA)," *IEEE Trans. Ind. Electron.*, vol. 59, no. 9, pp. 3523–3531, Sep. 2012, doi: 10.1109/TIE.2011.2165453.

[13] L. de Lillo *et al.*, "Multiphase power converter drive for fault-tolerant machine development in aerospace applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 2, pp. 575–583, Feb. 2010, doi: 10.1109/TIE.2009.2036026.

[14] T. M. Jahns, "Improved reliability in solid-state ac drives by means of multiple independent phase drive units," *IEEE Trans. Ind. Appl.*, vol. IA-16, no. 3, pp. 321–331, May 1980, doi: 10.1109/TIA.1980.4503793.

[15] J. Haylock, B. Mecrow, A. Jack, and D. Atkinson, "Operation of a fault tolerant pm drive for an aerospace fuel pump application," in *Proc. 8th Int. Conf. Elect. Mach. Drives*, 1997, pp. 133–137, doi: 10.1049/cp:19971053.

[16] F. Savi, G. Buticchi, C. Gerada, P. Wheeler, and D. Barater, "Information technologies for distributed machine drives: An overview," in *Proc. IEEE Int. Electric Mach. Drives Conf.*, 2019, pp. 1805–1809, doi: 10.1109/IEMDC.2019.8785232.

[17] V. Bianchi, F. Savi, I. De Munari, D. Barater, G. Buticchi, and G. Franceschini, "Minimization of network induced jitter impact on fpga-based control systems for power electronics through forward error correction," *Electronics*, vol. 9, no. 2, p. 281, 2020, doi: 10.3390/electronics9020281, [Online]. Available: https://www.mdpi.com/2079-9292/9/2/281

[18] G. H. B. Foo, X. Zhang, and D. M. Vilathgamuwa, "A sensor fault detection and isolation method in interior permanent-magnet synchronous motor drives based on an extended Kalman filter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 8, pp. 3485–3495, Aug. 2013, doi: 10.1109/TIE.2013.2244537.

[19] A. Mohammadpour and L. Parsa, "Global fault-tolerant control technique for multiphase permanent-magnet machines," *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 178–186, Feb. 2015, doi: 10.1109/TIA.2014.2326084.

[20] J. Fu and T. A. Lipo, "Disturbance free operation of a multiphase current regulated motor drive with an opened phase," in *Proc. Conf. Record IEEE Ind. Appl. Conf. 28th IAS Annu. Meeting*, 1993, pp. 637–644, doi: 10.1109/IAS.1993.298884.

[21] Z. Sun, J. Wang, G. W. Jewell, and D. Howe, "Enhanced optimal torque control of fault-tolerant PM machine under flux weakening operation," in *Proc. 18th Int. Conf. Elect. Mach.*, doi: 10.1109/ICELMACH.2008.4800114, 2008, pp. 1–6.

[22] A. Tani, M. Mengoni, L. Zarri, G. Serra, and D. Casadei, "Control of multiphase induction motors with an odd number of phases under open-circuit phase faults," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 565–577, Feb. 2012, doi: 10.1109/TPEL.2011.2140334.

[23] A. Timbus, M. Liserre, R. Teodorescu, P. Rodriguez, and F. Blaabjerg, "Evaluation of current controllers for distributed power generation systems," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 654–664, Mar. 2009, doi: 10.1109/TPEL.2009.2012527.

[24] R. Bojoi, F. Farina, A. Tenconi, F. Profumo, and E. Levi, "Dual three-phase induction motor drive with digital current control in the stationary reference frame," *Power Engineer*, vol. 20, no. 3, pp. 40–43, 2006, doi: 10.1049/pe:20060308.

[25] H. S. Che, E. Levi, M. Jones, W. Hew, and N. A. Rahim, "Current control methods for an asymmetrical six-phase induction motor drive," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 407–417, Jan. 2014, doi: 10.1109/TPEL.2013.2248170.

[26] L. F. A. Pereira and A. S. Bazanella, "Tuning rules for proportional resonant controllers," *IEEE Trans. Control Syst. Technol.*, vol. 23, no. 5, pp. 2010–2017, Sep. 2015, doi: 10.1109/TCST.2015.2389655.

[27] D. G. Holmes, T. A. Lipo, B. P. McGrath, and W. Y. Kong, "Optimized design of stationary frame three phase ac current regulators," *IEEE Trans. Power Electron.*, vol. 24, no. 11, pp. 2417–2426, Nov. 2009, doi: 10.1109/TPEL.2009.2029548.

[28] S. Silwal and M. Karimi-Ghartemani, "On the design of proportional resonant controllers for single-phase grid-connected inverters," in *Proc. 12th IEEE Int. Conf. Control Automat.*, 2016, pp. 797–803doi: 10.1109/ICCA.2016.7505376.

[29] W. Lenwari, M. Sumner, and P. Zanchetta, "The use of genetic algorithms for the design of resonant compensators for active filters," *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 2852–2861, Aug. 2009, doi: 10.1109/TIE.2009.2018535.

[30] R. Rosso, J. Cassoli, G. Buticchi, S. Engelken, and M. Liserre, "Robust stability analysis of LCL filter based synchronverter under different grid conditions," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5842–5853, Jun. 2019, doi: 10.1109/TPEL.2018.2867040.

[31] A. Bouzid, A. Chériti, and P. Sicard, "H-infinity loopshaping controller design of micro-source inverters to improve the power quality," in *Proc. IEEE 23rd Int. Symp. Ind. Electron.*, 2014, pp. 2371–2378, doi: 10.1109/ISIE.2014.6864990.

[32] S. Cobreces, E. J. Bueno, F. J. Rodriguez, D. Pizarro, and F. Huerta, "Robust loop-shaping h_∞ control of LCL-connected grid converters," in *Proc. IEEE Int. Symp. Ind. Electron.*, 2010, pp. 3011–3017, doi: 10.1109/ISIE.2010.5637614.

[33] S. Sumsurooah, M. Odavic, and S. Bozhko, "μ approach to robust stability domains in the space of parametric uncertainties for a power system with ideal CPL," *IEEE Trans. Power Electron.*, vol. 33, no. 1, Jan. 2018, doi: 10.1109/TPEL.2017.2668900.

[34] R. Lind, G. Balas, and A. Packard, "Evaluating DK iteration for control design," in *Proc. Amer. Control Conf.*, 1994, vol. 3, pp. 2792–2797, 10.1109/ACC.1994.735077.

[35] P. Apkarian and D. Noll, "Nonsmooth h_∞ synthesis," *IEEE Trans. Autom. Control*, vol. 51, no. 1, pp. 71–86, Jan. 2006, doi: 10.1109/TAC.2005.860290.

[36] M. J. Duran, I. Gonzalez-Prieto, N. Rios-Garcia, and F. Barrero, "A simple, fast, and robust open-phase fault detection technique for six-phase induction motor drives," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 547–557, Jan. 2018, doi: 10.1109/TPEL.2017.2670924.

[37] M. Riera-Guasp, J. A. Antonino-Daviu, and G. Capolino, "Advances in electrical machine, power electronic, and drive condition monitoring and fault detection: State of the art," *IEEE Trans. Ind. Electron.*, vol. 62, no. 3, pp. 1746–1759, Mar. 2015, doi: 10.1109/TIE.2014.2375853.

[38] M. Naidu, S. Gopalakrishnan, and T. W. Nehl, "Fault-tolerant permanent magnet motor drive topologies for automotive x-by-wire systems," *IEEE Trans. Ind. Appl.*, vol. 46, no. 2, pp. 841–848, Mar./Apr. 2010, doi: 10.1109/TIA.2009.2039982.

[39] B. A. Welchko, T. A. Lipo, T. M. Jahns, and S. E. Schulz, "Fault tolerant three-phase ac motor drive topologies: A comparison of features, cost, and limitations," *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 1108–1116, Jul. 2004, doi: 10.1109/TPEL.2004.830074.

[40] I. G. Prieto, M. J. Duran, P. Garcia-Entrambasaguas, and M. Bermudez, "Field-oriented control of multiphase drives with passive fault tolerance," *IEEE Trans. Ind. Electron.*, vol. 67, no. 9, pp. 7228–7238, Sep. 2020, doi: 10.1109/TIE.2019.2944056.

FILIPPO SAVI (Graduate Student Member, IEEE) received the M.Sc. degree in electronic engineering from the University of Parma, Parma, Italy, in 2017. He is currently working toward the Ph.D. degree with the University of Nottingham, Nottingham, U.K.

His research interests include high speed drives, modular and fault tolerant power electronics for transportation electrification and digital communications for high performance, low latency and jitter for high bandwidth feedback control.

DAVIDE BARATER (Senior Member, IEEE) received the master's degree in electronic engineering and the Ph.D. degree in information technology from the University of Parma, Parma, Italy, in 2009 and 2014, respectively. In 2012, he was an Honorary Scholar with the University of Nottingham, Nottingham, U.K., and in 2015, a Visiting Researcher with the University of Kiel, Kiel, Germany. He is currently an Associate Professor with the Department of Engineering "Enzo Ferrari", University of Modena and Reggio Emilia, Modena and Reggio Emilia, Italy. He is the author or coauthor of more than 60 international papers. His research focuses on power electronics for e-mobility and motor drives. He is the Coordinator of two European Project: RAISE, to evaluate the impact of the high voltage gradients, introduced by the fast commutations of new wide bandgap power devices (SiC, GaN), on the life time of electrical motor insulation systems. AUTO-MEA that aims to develop electrical motors and drives for next generation of electrical mobility. In particular, novel solutions for windings structures and cooling systems for improved power density, efficiency and increased frequency operation. He is an Associate Editor for the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS.

GIAMPAOLO BUTICCHI (Senior Member, IEEE) received the master's degree in electronic engineering and the Ph.D. degree in information technologies from the University of Parma, Parma, Italy, in 2009 and 2013, respectively. In 2012, he was a Visiting Researcher with The University of Nottingham, Nottingham, U.K. Between 2014 and 2017, he was a Postdoctoral Researcher and Von Humboldt Postdoctoral Fellow with the University of Kiel, Kiel, Germany.

He is currently a Professor of electrical engineering with The University of Nottingham, Ningbo, China and the Head of Power Electronics of the Nottingham Electrification Center. He is the author or coauthor of more than 200 scientific papers. His research focuses on power electronics for renewable energy systems, smart transformer fed micro-grids, and dc grids for the more electric aircraft. He is an Associate Editor for the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS and IEEE TRANSACTIONS ON TRANSPORTATION ELECTRIFICATION.

He is the Chair of the IEEE Industrial Electronics Society Technical Committee on Renewable Energy Systems.

PAT WHEELER (Fellow, IEEE) received the B.Eng. (Hons) degree from the University of Bristol, Bristol, U.K., in 1990 and the Ph.D. degree in electrical engineering for his work on matrix converters from the University of Bristol, in 1994. In 1993, he moved to the University of Nottingham, Nottingham, U.K., and was a Research Assistant with the Department of Electrical and Electronic Engineering. In 1996, he became a Lecturer with the Power Electronics, Machines and Control Group, University of Nottingham. Since January 2008, he has been a Full Professor with same research group. From 2015 to 2018, he was the Head of the Department of Electrical and Electronic Engineering, University of Nottingham. He is currently the Head of the Power Electronics, Machines and Control Research Group and is the Li Dak Sum Chair Professor of electrical and aerospace engineering with the University of Nottingham Ningbo China, Ningbo, China. He has authored or coauthored 500 academic publications in leading international conferences and journals. He is a Member of the IEEE PELs AdCom and was an IEEE PELs Distinguished Lecturer from 2013 to 2017.

CHRIS GERADA (Senior Member, IEEE) received the Ph.D. degree in numerical modelling of electrical machines from the University of Nottingham, Nottingham, U.K., in 2005. He subsequently was a Researcher with the University of Nottingham on high-performance electrical drives and on the design and modelling of electromagnetic actuators for aerospace applications. In 2008, he was appointed Lecturer of electrical machines, in 2011, an Associate Professor, and in 2013, a Professor. He has secured major industrial, European, and U.K. grants, and authored more than 200 papers. His core research focuses on the design and modelling of high-performance electric drives and machines. He is an Associate Editor for the IEEE TRANSACTION ON INDUSTRY APPLICATIONS. He was awarded a Royal Academy of Engineering Research Chair to consolidate research in the field.