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Discontinuous Conduction Mode Analysis of High Gain Extended-Duty-Ratio Boost Converter

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ABSTRACT A typical non-isolated photovoltaic (PV) microinverter requires a high conversion ratio in the dc-dc stage as well as needs to support a wide range of input-output voltage operation accommodating partial shading scenario. An extended-duty-ratio (EDR) boost converter is a good candidate for such application as it provides a high efficiency solution with a hybrid of interleaved inductor and switched capacitor configuration significantly lowering the switch voltage stress, switching losses, and providing inherent equal current sharing among the input phases. However, these advantages of EDR boost converter in continuous conduction mode (CCM) is only true for a limited duty ratio range. On the contrary, it is observed that the discontinuous conduction mode (DCM) can support a wider range of duty ratio operation, maintaining lower voltage stress on the devices and ensuring inherent equal current sharing among the boost inductors. Nevertheless, even in the DCM, the operation in the region with least voltage gain becomes very complex and requires a thorough understanding. This paper presents an extensive analysis of an EDR boost converter for DCM operation for all the operating regions. The operating characteristics of an EDR boost converter in DCM is analysed and its gain is derived. The detailed analysis presented in this paper enables in designing the components and judiciously deciding the operating range of EDR boost converter in DCM operation for any application. In order to verify the analysis, the simulation and experimental results from a 300 W EDR boost hardware prototype are also provided.

INDEX TERMS Extended duty ratio converter, high gain conversion, high voltage step up, interleaved boost, multi-phase converter, discontinuous conduction mode, switched capacitor.

I. INTRODUCTION

A photovoltaic (PV) inverter is a key power processing unit to tap in the solar energy which interfaces the PV-generated power to the consumer loads or utility grid. Among different PV inverter configurations, microinverter has emerged as a prominent choice given its modularity, plug-and-play feature, and increased module level maximum power extraction capability [1]. As a microinverter is directly connected to individual PV panel with input voltage in the range of 40 V, a high conversion ratio is required to step it up to the grid voltage level (120/230 V) requiring an appropriate high dc-link voltage [2]. Another objective with PV inverters is to support a wide range of input voltage to accommodate partial shading conditions.

One of the major focuses of the research efforts on microinverters is geared towards implementation of non-isolated dc-dc stage [3]–[5]. An extended duty ratio (EDR) boost converter is a good candidate for the high gain dc-dc stage of a non-isolated two-stage microinverter [6]. It is a hybrid of interleaved inductor and switched capacitor configuration significantly lowering the switch voltage stress (decreases by a factor of the number of phases), switching losses and

offers inherent input current sharing among different phases [7], [8]. However, in its continuous conduction mode (CCM) of operation, these advantages exist only for a small operating range characterized by duty ratio D span of $\frac{M-1}{M} \leq D \leq 1$, where M is the number of interleaved phases [9]. Thus, for an EDR boost converter designed to operate over a wide range of conversion ratio, as is required for microinevrter operation to support partial shading condition, the feature of inherent current sharing is lost. Few duty ratio modification schemes to ensure equal current sharing in all operating zones in CCM are proposed [9]–[12], but these approaches increase the control complexity. More importantly with different duty ratio for each phase, EDR converter looses the capability to operate with a common pulse width modulator (PWM). Also, switches with higher voltage rating and thus higher $R_{DS(ON)}$ is required, which would impact the over-all converter efficiency. The converter operation in critical conduction mode (CRM) is discussed in [13], however, even in this mode the converter has limited range of conversion ratio.

The above limitation of wide conversion ratio operation in CCM/CRM is removed if the EDR boost converter is operated in discontinuous conduction mode (DCM). This is because, DCM can support a wider range of duty ratio operation with $\frac{1}{M} \leq D \leq 1$ while simultaneously maintaining lower voltage stress on the devices (voltage stress is $1/M$ of the output voltage) and ensuring inherent equal current sharing among the boost inductors. Also compared to CCM, the inductors are smaller providing higher converter power density. Because of these reasons, for microinverter requiring high power density, high gain, and a wide conversion ratio, EDR boost converter in DCM is a better alternative than operation in CCM.

Further in DCM operation, the diode reverse recovery problem can be avoided and right-half plane (RHP) zero problem encountered in buck-boost and boost derived topologies is solved [14]. Also, as the switching devices would turn ON under zero current switching in DCM, the switching losses will be minimized [15]. Power factor correction (PFC) circuits are sometimes purposefully made to operate in DCM to achieve zero-current switch turn ON as well as no reverse recovery of diode [16]. Operation in DCM also simplifies PFC control implementation [17] though the device stresses are higher. Additionally, inductor current ripple and conduction loss are higher in DCM than in CCM operation [18].

DCM operation of interleaved boost converter is presented in [19], [20] while authors in [21] investigated a 2-phase interleaved boost converter with coupled inductors in DCM. DCM operation is proposed for the input-series and output-series connected modular single-switch flyback to achieve self-balance of the input and output voltages across the individual modules [22], while [23] studied the DCM operation of dc-dc converters feeding constant power loads. This paper presents the analysis and results of the DCM operation of an EDR boost converter by investigating all its possible operating modes. Analysis for boost [9], buck [24], or bidirectional [25] versions of EDR converter are available in literature, however, because of the interleaving of phases and its hybrid operation, the operation of EDR is quite involving, and these works are primarily focused only on its one operation mode, i.e., CCM. [26] presents an efficiency improvement technique of a 2-phase EDR buck converter in light load operation, however, an exhaustive study considering all the operating zones and modes of EDR boost converter in DCM condition remains unexplored.

In conventional boost converter, DCM will experience higher ripple on the inductor current. However, for the EDR converter (similar to other interleaved converters), even though the inductor in individual phases will have high current ripple, the ripple in the combined current drawn from the input source is considerably lower than the individual inductor current ripple due to the effective interleaving and partial ripple cancellation [27], [28]. Since EDR results in significant reduction in the input current ripple due to interleaving and ripple cancellation, in many applications, power density considerations may favor use of very small filter inductances and high ripple currents in individual inductors, which can lead to DCM operation under light load conditions. Other than front-end dc-dc converter in microinverter supporting operation in partial shading condition, point-of-load (POL) regulators and 48/1 V power converters for data centers at high switching frequency supporting wide power range are some other typical applications of high gain EDR converter in DCM.

In this paper, the DCM operation of EDR boost converter is studied in detail. It is to be noted that for the operation in DCM in the least gain region (characterized by duty ratio $D < \frac{1}{M}$), all the inductors except phase 1 will conduct negative current even for non-synchronous converter arrangement. Though this negative current conduction is for a small fraction of the switching cycle, yet it leads to additional circulating current inducing additional power loss in the converter. Further, the converter operation in this region (for $D < \frac{1}{M}$) is very complex and it is not straightforward to derive the expression for converter voltage gain. In this work, a curve fitting technique is implemented to obtain the converter's gain over the complete duty ratio range. As the analysis of EDR converter in DCM remains unexplored in previous literature, this paper focuses on an extensive analysis of its DCM operating characteristic. This is essential to design the converter parameters and components for any practical application requiring high gain as well wide range of input-output voltage operation in DCM.

The rest of the paper is arranged as follows. Section II discusses the operating principles in DCM of a 3-phase EDR boost converter in Zones I and II. The operation in Zone III is more involved and is discussed in following Section III. The next Section IV studies in detail the converter gain in each of the operating zones. A curve fitting technique to determine the voltage gain expression for Zone III DCM operation is elaborated here. In the subsequent Section V the design methodology for a 3-phase EDR boost converter is presented along with the details of the hardware prototype. Finally, the operation and its analysis of the converter in DCM is validated with experimental results, detailed loss analysis, and gain curve.

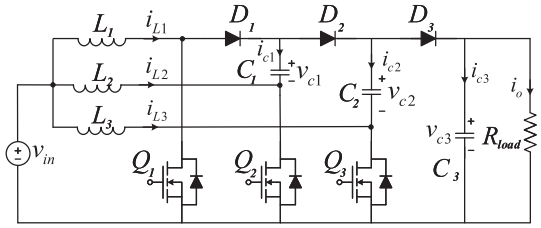

FIGURE 1. Topology for 3-phase extended duty ratio (EDR) boost converter.

II. OPERATING PRINCIPLES

EDR boost converter is a hybrid of interleaved boost inductors and switched capacitor concept. An M-phase EDR boost converter comprises of M coupled phases, each of which consists of an inductor L_i, a capacitor C_i, and a pair of switching devices (D_i-Q_i). A diode D_i and a MOSFET Q_i are considered for non-synchronous version (where $i = 1, 2, \ldots M$). Each boost phases is interleaved and are phase shifted by $(360/M)^\circ$. M operating zones can be identified for M-phase EDR, characterized by the operating duty ratio range as given by $\frac{M-m}{M} \leq D \leq \frac{M-m+1}{M}$ for all $m \in [1, M]$. This is true for both the CCM and DCM operation of the converter.

Inherent current sharing in the interleaved input inductors of M-phase EDR boost converter is possible for $(M-1)$ number of zones unlike in CCM operation which sees inherent current sharing for only Zone I operation [9]. Further for Zone M, there exists multiple operating cases with different combination of operating modes in DCM condition.

A 3-phase EDR boost converter is considered here to study the DCM operation of the EDR boost converter as shown in Fig. 1. With equal duty ratio D for each phase and a phase shift of 120° between them, the input current is shared between the interleaved phases for operating Zones I and II, while for Zone III it is still not shared. Moreover, Zone III operation has multiple cases depending on the duty ratio and the average input current of the converter with different combination of operating modes as discussed shortly.

It is to be noted that the operation of the converter in Zone III is not desired as in this operating region the voltage stress on the switching devices are higher than in other two operating zones. However, for the closed loop operation of the converter, it might operate in Zone III, specifically for applications supporting wide range of input/output voltage like dc-dc optimizer in PV microinverter with different range of insolation and partial shading condition.

The boundary between CCM and DCM operation can be derived in a similar way as the conventional boost converter. For DCM operation, the average inductor current for each phase $i_{Li_{avg}}$ should be less than one-half of its corresponding peak-peak ripple current Δi_{Li} (where $i = 1, 2, 3$) which leads to the following condition (1) for DCM.

$$\frac{2L}{RT_s} < \frac{DD'^2}{3} \tag{1}$$

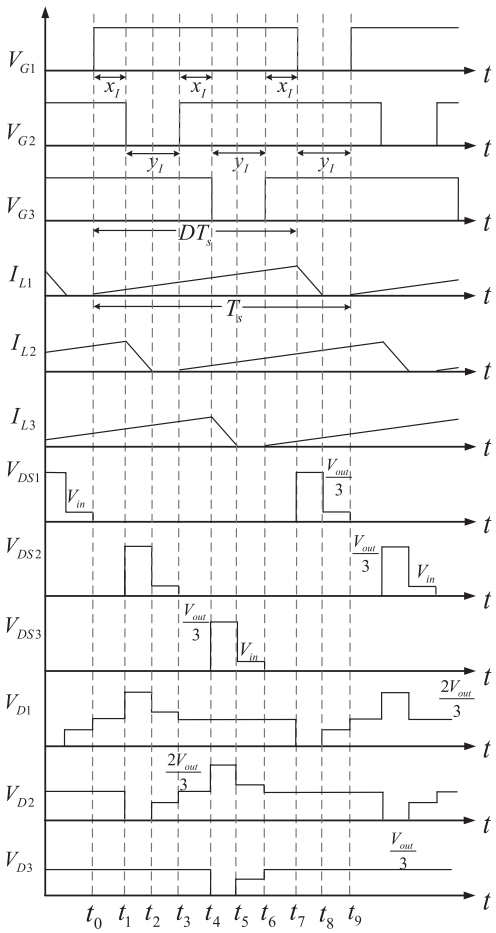

FIGURE 2. Gate signal, inductor current, and device voltages for DCM operation in Zone I ($2/3 \leq D < 1$) for 3-phase EDR boost; unlike in CCM, the waveforms for Zone I and II remain similar in DCM operation.

where, D' is defined as complementary to the duty D, mathematically it is expressed as $D' = 1 - D$. A factor of 3 in (1) for the 3-phase EDR boost w.r.t. a conventional boost converter is consistent with the voltage gain expression obtained for the CCM operation. The voltage gain of an M-phase EDR boost converter in CCM is M times that of a regular boost converter ($\frac{M}{1-D}$) [9]. A dimensionless parameter k is defined by $k = \frac{2L}{RT_s}$ and its critical value $k_{crit} = \frac{DD'^2}{3}$ for DCM can be identified from (1) indicating that any value of $k < k_{crit}$ leads to the discontinuous operation of the EDR boost converter.

A. ZONE I OPERATION

Zone I corresponds to the duty ratio range $2/3 \leq D < 1$. For DCM operation, Fig. 2 shows the typical gate signal and corresponding inductor current. This also shows the voltage stress of the diodes (denoted by V_{Di}) and MOSFETs (denoted by V_{DSi}) in this zone of operation, where $i = 1, 2, 3$ representing each of the three phases. Here, $x_I = (D - 2/3)T_s$, $y_I = (1 - D)T_s$, and T_s is the switching time period. x_I corresponds to operation where all the three devices (Q_1, Q_2,

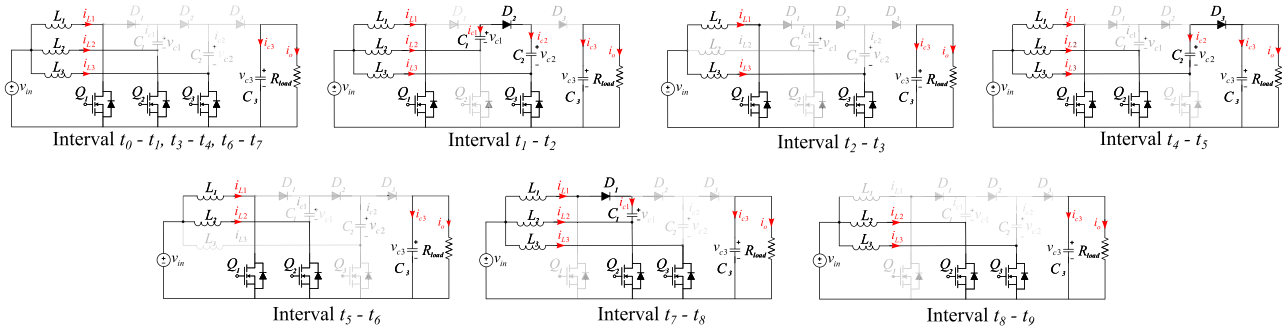

FIGURE 3. Current path corresponding to each of the operating intervals for DCM operation of 3-phase EDR boost in Zone I.

Q_3) are ON, while y_I corresponds to time interval where any two of the three devices are ON. At t_0 when Q_2 and Q_3 are already conducting, Q_1 is turned ON and L_1 starts charging until t_7 when Q_1 is turned OFF. At t_1, Q_2 is turned OFF, D_2 starts conducting and L_2 is discharged until t_2. At t_2, i_{L2} reaches zero and D_2 stops conducting. This interval ends at t_3 when Q_2 is turned back ON. Interval $t_2 - t_3$ corresponds to the zero current operation region for phase II. Similar operation is repeated for the other two phases, the corresponding current paths in each of the intervals are shown in Fig. 3 (the shaded components are not conducting).

The maximum voltage stress for each device has been marked in the analytical waveforms. It can be seen that all the switches experience a voltage stress of $v_{out}/3$, while it is $2v_{out}/3$ for the diodes of first two phases and $v_{out}/3$ for the third one. Also, the inductor currents are equal in all three phases with similar slope, peak, and average values with a phase shift of 120°. These are similar to the characteristics observed for Zone I operation in 3-phase EDR boost converter in CCM.

B. ZONE II OPERATION

For Zone II, the duty ratio range is given as $1/3 \leq D < 2/3$. It is interesting to note that for Zone II operation in DCM, the waveforms are similar to that of Zone I with $x_{II} = (D - 1/3)T_s$ and $y_{II} = (2/3 - D)T_s$, and thus, are not repeated here. This is different than the CCM operation, where Zone II has different combination of operating modes, higher device voltage stress, and unequal phase inductor current, which is a disadvantage of CCM operation intended for wide voltage gain application.

Zone III operation in DCM is more involved with multiple slope for each of the inductor currents in a switching cycle and is discussed in a separate section.

III. ZONE III OPERATION

Zone III corresponds to the duty ratio range $0 \leq D < 1/3$. In this zone, individual inductor current has negative current excursion even for non-synchronous circuit implementation. It is to be noted that in a conventional boost converter, the inductor current goes to negative (conducts in opposite direction) only when the diode is replaced by a synchronous device in DCM operation. However for EDR boost converter, due to the coupling between the interleaved phases with the switched capacitors, in Zone III the inductor current can conduct in negative direction even in the non-synchronous version of the converter. The negative current path can be appreciated by noting the conducting devices during each of the operating interval as discussed below. The presence of the negative phase current leads to circulating current in the converter accounting to additional conduction loss. It also has limited impact on the converter's gain as discussed in next Section. Depending on the converter duty ratio D, DCM parameter k, and the negative conduction of the MOSFETs, Zone III can further have different operating cases, analyzed below.

A. CASE I

For DCM operation, Fig. 4(a) shows the typical gate signal, corresponding inductor current, and switch voltage stress of both the diode (denoted by V_{Di}) and MOSFETs (denoted by V_{DSi}) for Case I operation in Zone III, where $x_{III} = DT_s$, $y_{III} = (1/3 - D)T_s$ and $i = 1, 2, 3$. This operating condition is characterized by no negative conduction of the MOSFETs. The maximum voltage stress for all the devices is shown in the analytical waveforms. As can be seen from this switching diagram, Q_1, Q_2, and Q_3 conduct in the time intervals $t_0 - t_1$, $t_2 - t_3$, and $t_4 - t_5$ respectively. Different operating intervals are marked in Fig. 4(a), based on which Table 1 gives the conducting devices, inductor voltages, and capacitor current expressions. Current paths for each of these intervals are shown in Fig. 5 where the shaded components are not conducting.

The inductor voltages in these intervals are obtained by applying KVL. Additionally, the conditions $v_{L1} + v_{L2} + v_{L3} = 0$ and $v_{L1} + v_{L2} = 0$ are respectively applied for interval b and c to derive the corresponding voltages in these intervals. Capacitor currents are obtained by applying KCL at appropriate nodes. The final column in Table 1 describes the condition of transition from one interval to its subsequent one.

Denoting i_{L1a} as the inductor current of boost phase I at the end of the interval a, and by noting its slope from Table 1 at that interval, i_{L1a} can be obtained as

$$i_{L1a} = \frac{v_{in}}{L} DT_s + \frac{v_{in} - v_{out}}{L} aT_s \tag{2}$$

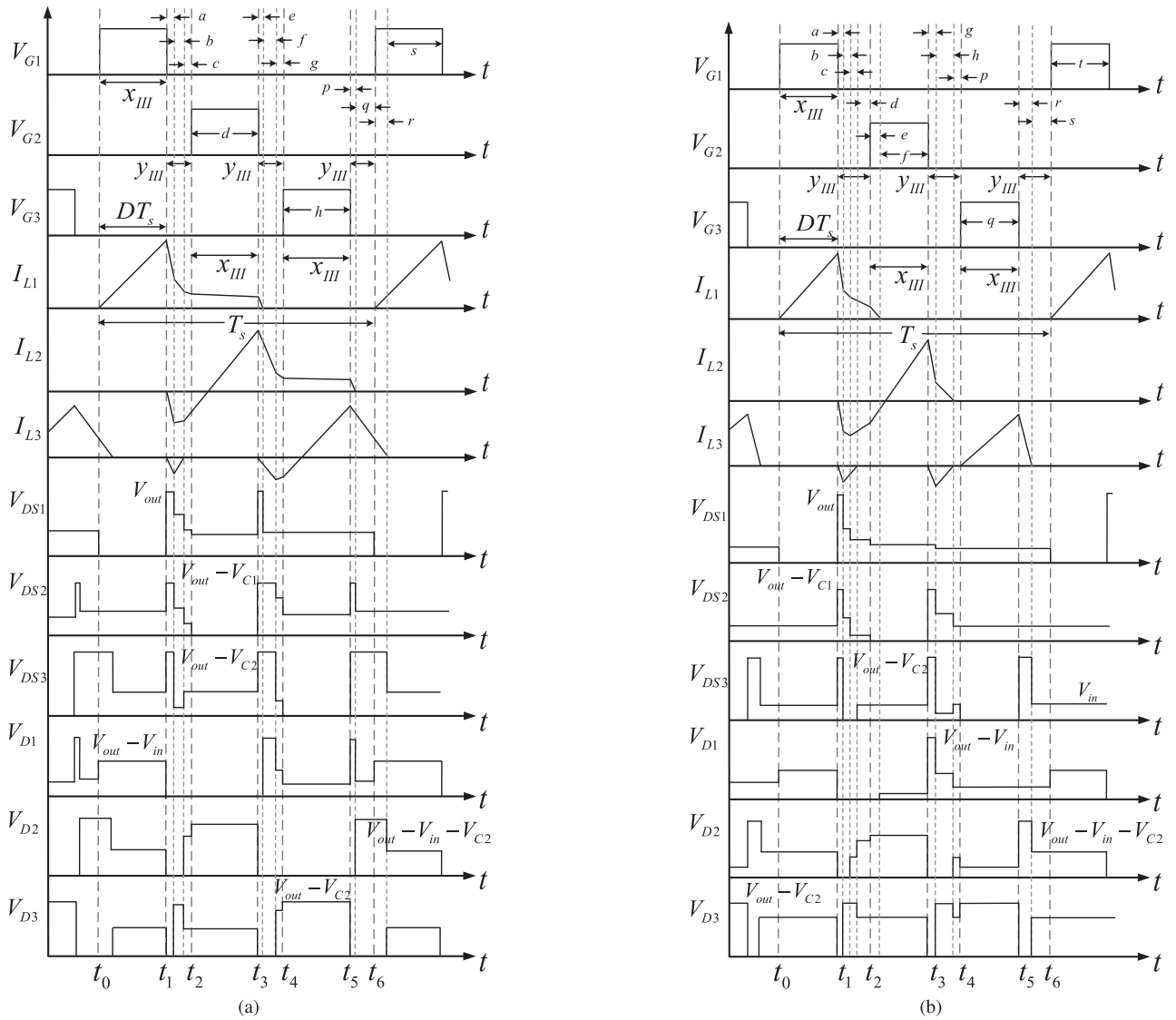

FIGURE 4. Gate signal, inductor current, and device voltages for DCM operation in Zone III for 3-phase EDR boost (a) Case I (no negative conduction of any MOSFET), (b) Case II (negative conduction of Q_3).

Similarly, each of the phase currents can be obtained at the end of each operating interval (representation similar to i_{L1a} is followed for all others). Subsequently, the mathematical expression of these intervals can be obtained by applying the condition which marks the end of the interval (given in the final column of Table 1). For example, interval a ends when condition $i_{L1a} + i_{L2a} + i_{L3a} = 0$ is satisfied, which is used to derive the expression for a as

$$a = \frac{v_{in}D}{3v_{out} - 3v_{in} - v_{c1} - v_{c2}} \tag{3}$$

The expression for all other intervals can be similarly obtained and are given in Table 2.

B. CASE II

Case II is characterized by the conduction of the diode of Q_3, i.e., negative current flows through it for certain intervals ($b + c$) as shown in Fig. 4(b). The analytical waveforms showing the typical gate signal, corresponding inductor current, and switch voltage stress of both the diodes (denoted by V_{Di}) and MOSFETs (denoted by V_{DSi}) for Case II operation in Zone III is given in Fig. 4(b), where $i = 1, 2, 3$. Similar to Case 1, Q_1, Q_2, and Q_3 conduct in the time intervals $t_0 - t_1$, $t_2 - t_3$, and $t_4 - t_5$ respectively as shown in Fig. 4(b). It is worth noting that the negative conduction of Q_3 happens only if the condition $3v_{in} < 2v_{c2} - v_{c1}$ is satisfied.

The intervals x_{III} and y_{III} is similar to that of the previous case. The maximum switch voltage stress is also marked in the figure, the voltage stress for all the intervals can be found by referring to Table 3. Different operating intervals are marked

TABLE I **Zone III ($0 \le D \le 1/3$) Case I**

Interval	Conducting device(s)	v_{L1}	v_{L2}	v_{L3}	i_{c1}	i_{c2}	i_{c3}	Comment
a	D_1, D_2, D_3	$v_{in} - v_{out}$	$v_{in} - v_{out} + v_{c1}$	$v_{in} - v_{out} + v_{c2}$	$-i_{L2}$	$-i_{L3}$	$i_{L1} + i_{L2} + i_{L3} - i_o$	ends when $i_{L1} = -i_{L2} - i_{L3}$
b	D_1, D_2	$\frac{-v_{c1} - v_{c2}}{3}$	$\frac{2v_{c1} - v_{c2}}{3}$	$\frac{2v_{c2} - v_{c1}}{3}$	$-i_{L2}$	$-i_{L3}$	$-i_o$	ends when $i_{L1} = -i_{L2}$ and $i_{L3} = 0$
c	D_1	$-v_{c1}/2$	$v_{c1}/2$	0	i_{L1}	0	$-i_o$	ends when Q_2 starts conducting
d	D_1, Q_2	$v_{in} - vc1$	v_{in}	0	i_{L1}	0	$-i_o$	ends when Q_2 stops conducting
e	D_1, D_2, D_3	$v_{in} - v_{out}$	$v_{in} - v_{out} + v_{c1}$	$v_{in} - v_{out} + v_{c2}$	$-i_{L2}$	$-i_{L3}$	$i_{L1} + i_{L2} + i_{L3} - i_o$	ends when $i_{L1} = 0$
f	D_2, D_3	0	$v_{in} - v_{out} + v_{c1}$	$v_{in} - v_{out} + v_{c2}$	$-i_{L2}$	$-i_{L3}$	$i_{L2} + i_{L3} - i_o$	ends when $i_{L2} = i_{L3}$
g	D_2	0	$\frac{v_{c1} - v_{c2}}{2}$	$\frac{-v_{c1} + v_{c2}}{2}$	$-i_{L2}$	$-i_{L3}$	$-i_o$	ends when Q_3 starts conducting
h	D_2, Q_3	0	$v_{in} + v_{c1} - v_{c2}$	v_{in}	$-i_{L2}$	i_{L2}	$-i_o$	ends when Q_3 stops conducting
p	D_2, D_3	0	$v_{in} - v_{out} + v_{c1}$	$v_{in} - v_{out} + v_{c2}$	$-i_{L2}$	$-i_{L3}$	$i_{L2} + i_{L3} - i_o$	ends when $i_{L2} = 0$
q	D_3	0	0	$v_{in} - v_{out} + v_{c2}$	0	$-i_{L3}$	$i_{L3} - i_o$	ends when Q_1 starts conducting
r	Q_1, D_3	v_{in}	0	$v_{in} - v_{out} + v_{c2}$	0	$-i_{L3}$	$i_{L3} - i_o$	ends when $i_{L3} = 0$
s	Q_1	v_{in}	0	0	0	0	$-i_o$	ends when Q_1 stops conducting

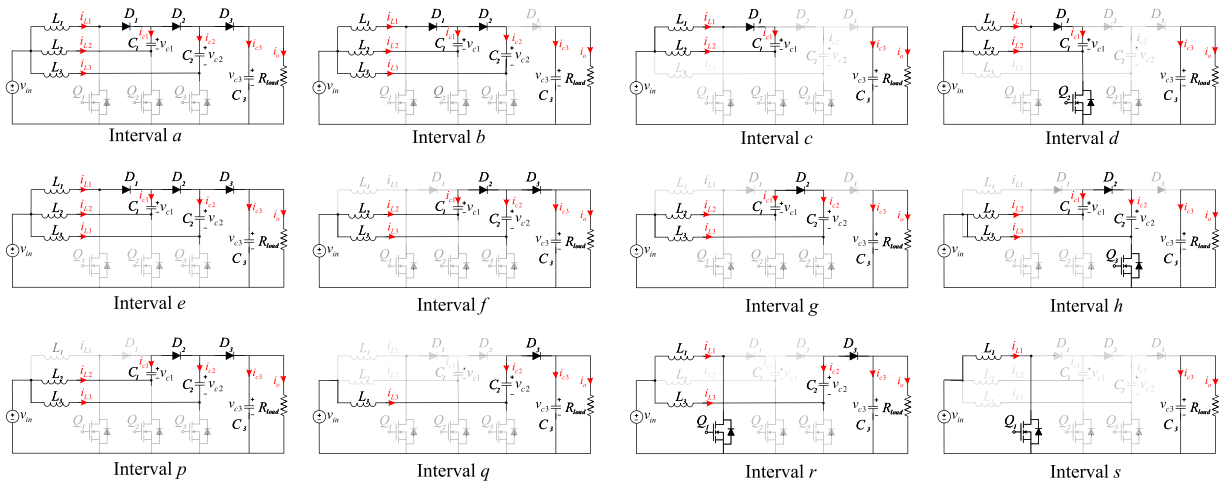

FIGURE 5. **Current path corresponding to each of the operating intervals for DCM operation of 3-phase EDR boost in Zone III Case 1.**

in Fig. 4(a), based on which Table 3 gives the conducting devices, inductor voltages, and capacitor currents. Similar to Case I, the final column in the table describes the condition of transition from one interval to its next. Current paths for each of these intervals are shown in Fig. 6 where the shaded components are not conducting.

Following the same procedure as above, the expression for each of the operating interval is derived as given in Table 4.

C. CASE III

Case III is characterized by the negative conduction of both Q_2 and Q_3. The operating intervals can be similarly derived as Cases I and II and are not shown here to avoid lengthy repetition.

Also it is to be noted that apart from the presented waveforms in Figs. 4(a) and 4(b), there can exists variation in the combination of operating intervals. However, these additional cases have very similar operating characteristics as the basic ones discussed here with limited differences in the operating intervals. In fact, the new ones would constitute a sub-set of these three operating cases. For example, a variant of Case II has no p interval, though it retains the basic operating principles of Case II.

IV. CONVERTER GAIN IN DCM

Similar to the concept used in conventional boost converter, for computing the converter gain in DCM, the inductor switching current ripple cannot be neglected while the ripple

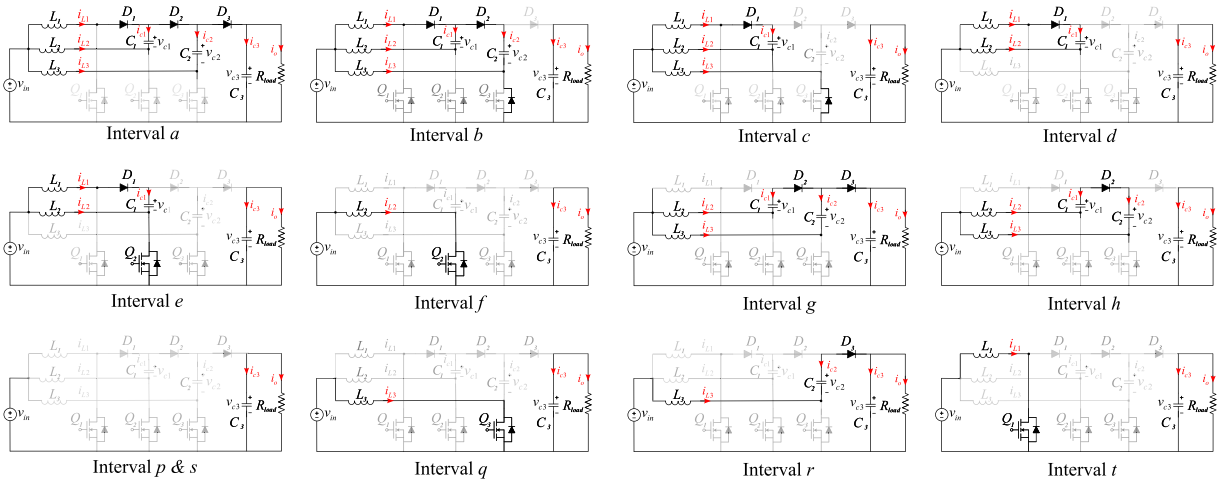

FIGURE 6. Current path corresponding to each of the operating intervals for DCM operation of 3-phase EDR boost in Zone III Case 2.

TABLE II Computing Operating Interval for Case I Operation in Zone III

Condition applied	Expression of interval
$i_{L1a}+i_{L2a}+i_{L3a}=0$	$a=\dfrac{v_{in}D}{3v_{out}-3v_{in}-v_{c1}-v_{c2}}$
$i_{L3b}=0$	$b=\dfrac{(v_{out}-v_{in}-v_{c2})3a}{2v_{c2}-v_{c1}}$
$a+b+c=\frac{1}{3}(1-3D)$	$c=\frac{1}{3}-D-a-b$
$d=D$	$d=D$
$i_{L1e}=0$	$e=\dfrac{i_{L1d}}{v_{out}-v_{in}}\dfrac{L}{T_s}$
$i_{L2f}+i_{L3f}=0$	$f=\dfrac{i_{L2e}+i_{L3e}}{2v_{out}-2v_{in}-v_{c1}-v_{c2}}\dfrac{L}{T_s}$
$g+e+f=\frac{1}{3}(1-3D)$	$g=\frac{1}{3}-D-e-f$
$h=D$	$h=D$
$i_{L2p}=0$	$p=\dfrac{i_{L2h}}{v_{out}-v_{in}-v_{c1}}\dfrac{L}{T_s}$
$p+q=\frac{1}{3}(1-3D)$	$q=\frac{1}{3}-D-p$
$i_{L3r}=0$	$r=\dfrac{i_{L3q}}{v_{out}-v_{in}-v_{c2}}\dfrac{L}{T_s}$
$r+s=D$	$s=D-r$

on the intermediate and output capacitors can be neglected. The converter gain in each of the zones can be derived by applying the volt-second balance and charge balance for each of the phase inductors and capacitors respectively. The voltage gain is a function of both the converter duty ratio D and the dimensionless parameter k, analogous to any dc-dc converter operation in DCM.

With zero average current through all the capacitors over a switching cycle, the average current through each diode $< i_{Di} >$ (where $i=1,2,3$) is equal to the output current i_o as given below

$$< i_{D1} >=< i_{D2} >=< i_{D3} >= i_o = \frac{v_{out}}{R} \tag{4}$$

By invoking the condition in (4), the intermediate and output capacitor voltages for each of the operating zones are derived and discussed subsequently.

A. ZONE I AND II

The operating characteristic being similar for both the Zones I and II, the converter gain can be represented by one general expression for these zones as given in (5). As the input current is shared equally among all the interleaved inductors and the intermediate capacitor voltages are integer fraction of the output voltages, it is straightforward to obtain the voltage expressions in these regions. The capacitor voltages are given in (6).

$$v_{out} = 1.5v_{in}\left(1+\sqrt{1+\frac{4D^2}{3\,k}}\right) \tag{5}$$

$$v_{c1}=\frac{v_{out}}{3};\quad v_{c2}=\frac{2v_{out}}{3} \tag{6}$$

B. ZONE III

As discussed in the previous section, each of the diode current in Zone III has multiple slopes over one switching cycle. So finding its average value is quite involving. By studying the inductor current waveforms from Figs. 4(a) and 4(b) and noting the conducting devices from Tables 1 and 3 corresponding to each operating intervals for Cases I and II respectively, the diode current waveforms can be constructed and its average is evaluated.

For Case I, the diode average current expressions $< i_{D1} >$, $< i_{D2} >$, and $< i_{D3} >$ are given by the following sets of equations (7)–(9), where each of the interval expressions is referred from Table 2.

$$< i_{D1} >= (i_{L1s}+i_{L1a})\frac{a}{2}+(i_{L1a}+i_{L1b})\frac{b}{2}+(i_{L1b}+i_{L1c})\frac{c}{2}$$
$$+(i_{L1c}+i_{L1d})\frac{d}{2}+i_{L1d}\frac{e}{2} \tag{7}$$

TABLE III Zone III ($0 \le D \le 1/3$) Case II

Interval	Conducting device(s)	v_{L1}	v_{L2}	v_{L3}	i_{c1}	i_{c2}	i_{c3}	Comment
a	D_1, D_2, D_3	$v_{in} - v_{out}$	$v_{in} - v_{out} + v_{c1}$	$v_{in} - v_{out} + v_{c2}$	$-i_{L2}$	$-i_{L3}$	$i_{L1} + i_{L2} + i_{L3} - i_o$	ends when $i_{L1} = -i_{L2} - i_{L3}$
b	D_1, D_2, Q_{D3}	$v_{in} - v_{c2}$	$v_{in} + v_{c1} - v_{c2}$	v_{in}	$-i_{L2}$	$-i_{L3} + i_{QD3}$	$-i_o$	ends when $i_{L1} = -i_{L2}$ and $i_{L3} \neq 0$
c	D_1, Q_{D3}	$-v_{c1}/2$	$v_{c1}/2$	v_{in}	$-i_{L2}$	0	$-i_o$	ends when $i_{L3} = 0$
d	D_1	$-v_{c1}/2$	$v_{c1}/2$	0	$-i_{L2}$	0	$-i_o$	ends when Q_2 starts conducting
e	D_1, Q_2	$v_{in} - vc1$	v_{in}	0	i_{L1}	0	$-i_o$	ends when D_1 stops conducting and $i_{L1} = 0$
f	Q_2	0	v_{in}	0	0	0	$-i_o$	ends when Q_2 stops conducting
g	D_2, D_3	0	$v_{in} - v_{out} + v_{c1}$	$v_{in} - v_{out} + v_{c2}$	$-i_{L2}$	$-i_{L3}$	$i_{L2} + i_{L3} - i_o$	ends when $i_{L2} = -i_{L3}$
h	D_2	0	$\frac{v_{c1} - v_{c2}}{2}$	$\frac{-v_{c1} + v_{c2}}{2}$	$-i_{L2}$	$-i_{L3}$	$-i_o$	ends when $i_{L2} = i_{L3} = 0$
p	–	0	0	0	0	0	$-i_o$	ends when Q_3 starts conducting
q	Q_3	0	0	v_{in}	0	0	$-i_o$	ends when Q_3 stops conducting
r	D_3	0	0	$v_{in} - v_{out} + v_{c2}$	0	$-i_{L3}$	$i_{L3} - i_o$	ends when D_3 stops conducting i.e., $i_{L3} = 0$
s	–	0	0	0	0	0	$-i_o$	ends when Q_1 starts conducting
t	Q_1	v_{in}	0	0	0	0	$-i_o$	ends when Q_1 stops conducting

TABLE IV Computing Operating Interval for Case II Operation in Zone III

Condition applied	Expression of interval
$i_{L1a} + i_{L2a} + i_{L3a} = 0$	$a = \frac{v_{in} D}{3v_{out} - 3v_{in} - v_{c1} - v_{c2}}$
$i_{L1b} + i_{L2b} = 0$	$b = \frac{i_{L1a} + i_{L2a}}{2v_{c2} - 2v_{in} + v_{c1}} \frac{L}{T_s}$
$i_{L3c} = 0$	$c = \frac{i_{L3c}}{v_{in}} \frac{L}{T_s}$
$a + b + c + d = \frac{1}{3}(1 - 3D)$	$d = \frac{1}{3} - D - a - b - c$
$i_{L1e} = 0$	$e = \frac{i_{L1d}}{v_{c1} - v_{in}} \frac{L}{T_s}$
$e + f = D$	$f = D - e$
$i_{L2g} + i_{L3g} = 0$	$g = \frac{i_{L2f}}{2v_{out} - 2v_{in} - v_{c1} - v_{c2}} \frac{L}{T_s}$
$i_{L2h} = 0$	$h = \frac{2i_{L2g}}{v_{c1} - v_{c2}} \frac{L}{T_s}$
$g + h + p = \frac{1}{3}(1 - 3D)$	$p = \frac{1}{3} - D - g - h$
$q = D$	$q = D$
$i_{L3r} = 0$	$r = \frac{i_{L3q}}{v_{out} - v_{in} - v_{c2}} \frac{L}{T_s}$
$r + s = \frac{1}{3}(1 - 3D)$	$s = \frac{1}{3} - D - r$
$t = D$	$t = D$

$$< i_{D2} >= (i_{L2d} + i_{L2e})\frac{e}{2} + (i_{L2e} + i_{L2f})\frac{f}{2} + (i_{L2f} + i_{L2g})\frac{g}{2} + (i_{L2g} + i_{L2h})\frac{h}{2} + i_{L2h}\frac{p}{2} + \zeta_1 \quad (8)$$

$$< i_{D3} >= \frac{1}{2} i_{L3h}(p + q + r) + \zeta_2 + \zeta_3 \quad (9)$$

where $\zeta_1 = (i_{L1s} + i_{L1a} + i_{L2a})\frac{a}{2} + (i_{L1a} + i_{L2a} + i_{L1b} + i_{L2b})\frac{b}{2}$, $\zeta_2 = i_{L1s}\frac{a}{2}$, and $\zeta_3 = (i_{L1d} + i_{L2d} + i_{L2e} + i_{L3e})\frac{e}{2} + (i_{L2e} + i_{L3e})\frac{f}{2}$. ζ_1 corresponds to the negative conduction of the phase II and ζ_2 and ζ_3 corresponds to negative conduction of phase III inductor currents.

Likewise, the diode average current expressions for Case II can be obtained as given by the following sets of equations (10)-(12) and each of the intervals can be referred from Table 4.

$$< i_{D1} >= (i_{L1s} + i_{L1a})\frac{a}{2} + (i_{L1a} + i_{L1b})\frac{b}{2} + (i_{L1b} + i_{L1d})\frac{c + d}{2} + i_{L1d}\frac{e}{2} \quad (10)$$

$$< i_{D2} >= (i_{L2f} + i_{L2g})\frac{g}{2} + i_{L2g}\frac{h}{2} + \zeta_1 \quad (11)$$

$$< i_{D3} >= i_{L3q}\frac{r}{2} + \zeta_2 + \zeta_3 \quad (12)$$

where $\zeta_1 = (i_{L1s} + i_{L1a} + i_{L2a})\frac{a}{2} + (i_{L1a} + i_{L2a})\frac{b}{2}$, $\zeta_2 = i_{L1s}\frac{a}{2}$, and $\zeta_3 = i_{L2f}\frac{g}{2}$. Identically to Case I, ζ corresponds to the negative conduction of phase II and III inductor currents.

(7)–(12) can be alternatively expressed in terms of v_{c1}, v_{c2}, and v_{out} and clubbing (4) with these, three sets of equations are formulated for each operating case. Finally, the expression of each of the capacitor voltages in terms of v_{in}, converter duty D, and DCM parameter k can be obtained by solving these

equations. However, it is clear that these are quite involved expressions and a direct numerical solution is difficult to achieve manually from the above equations. Thus, these are numerically solved in MATLAB using Levenberg-Marquardt (LM) algorithm over a range of operating conditions and multiple solution sets for each of the voltage variables are computed. By using these solution sets, the voltage expressions are then obtained through least square curve fit method as discussed next.

C. LEAST SQUARE CURVE FIT

Observing that the converter voltages are directly proportional to the input voltage, before applying the curve fit the voltage variables are normalized w.r.t. v_{in}. Subsequently, these normalized converter voltages are fitted with rest of the two variable parameters D and k in MATLAB. To formulate the curve fit problem, the variable vector is defined as $\boldsymbol{x} = [D,\ k]^T$ and the output vector is defined as $\boldsymbol{y_{data}} = [v_{c1},\ v_{c2},\ v_{out}]^T$. Please note that all the elements of $\boldsymbol{y_{data}}$ have been obtained for different combinations of D and k as mentioned in Section IV.B. The fitted function is $\boldsymbol{y_{fit}} = \boldsymbol{f(x, B)}$, where $\boldsymbol{B}$ is a matrix comprising of coefficients used to obtain the fit.

Further it is observed that the voltages are quadratic function of D and either linear (Case I) or inverse (Case II) function of k. This trend is obtained by fixing one variable and sweeping the other over a specified range. Considering this, the basis function of $\boldsymbol{f}$ is formulated as $\boldsymbol{u} = [1,\ D,\ D^2,\ k,\ \frac{1}{k}]^T$ and $\boldsymbol{B}$ is a 3×5 matrix. Thus, (13) is obtained.

$$\boldsymbol{y_{fit}} = \boldsymbol{f(x, B)} = \boldsymbol{Bu} \tag{13}$$

Consequently, the Norm 2 of error vector $\boldsymbol{E}$ is obtained as (14).

$$\boldsymbol{E} = \sum_{n=1}^{N_{data}} (\boldsymbol{y_{fit,n}} - \boldsymbol{y_{data,n}})^2 \tag{14}$$

where, $\boldsymbol{y_{fit,n}}$ and $\boldsymbol{y_{data,n}}$ are respectively the fitted and original values of the voltages at n^{th} data point, and N_{data} is the total number of data points for curve fit. Finally, the equations can be cast as unconstrained minimization problem as given in (15) which is set to minimize $\boldsymbol{E}$. The non-linear least square solver in MATLAB is used to implement the least square curve fit for both the cases. The robust LM algorithm is implemented for this purpose.

$$\min \sum_{n=1}^{N_{data}} (f(\boldsymbol{x_n}, \boldsymbol{B}) - \boldsymbol{y_{data,n}})^2 \tag{15}$$

As mentioned, for Case I operation, it is independently observed that the best fit is achieved for quadratic variation of D and linear variation of k. (16)-(18) give the voltage expressions as obtained from the curve fit solution for this case (normalized voltage is multiplied by v_{in} to obtain the actual value).

$$v_{c1} = v_{in}(21.53D^2 - 37.09\,k + 0.48) \tag{16}$$

$$v_{c2} = v_{in}(38.92D^2 - 78.89\,k + 1.13) \tag{17}$$

$$v_{out} = v_{in}(57.65D^2 - 213.54\,k + 4.04) \tag{18}$$

The rms of the error (normalized by their respective actual values v_{c1}, v_{c2}, and v_{out}) for each of the voltages and the fitted data are found to be 0.053%, 0.06%, 0.059% respectively indicating an excellent fit.

Before applying the 2-D curve fit for Case II operation in Zone III, it is first independently observed that the best fit is achieved for quadratic variation of D and is inversely proportional to k. (19)–(21) give the corresponding voltage expressions.

$$v_{c1} = v_{in}(-9.87D^2 + 10.06D + 0.0013/k - 0.78) \tag{19}$$

$$v_{c2} = v_{in}(-21.6D^2 + 18.23D + 0.0026/k - 1.14) \tag{20}$$

$$v_{out} = v_{in}(-18.97D^2 + 21.95D + 0.012/k - 0.74) \tag{21}$$

The rms of the error (normalized by their respective actual values v_{c1}, v_{c2}, and v_{out}) for each of the voltages and the fitted data are found as 0.053%, 0.057%, 0.044% respectively demonstrating that the fit is very useful for prediction of the voltage values for this operating condition. Similar analysis can be applied to compute these variable for the converter operation in Case III region and is not presented here to avoid repetition.

Within the limitation of the residual error, the empirical expressions for the capacitor voltages shown are good for the designers intending to implement EDR boost converters in DCM. Moreover, the curve fit method outlined here can also be used in other converter topologies with complex operating states. Figs. 7 and 8 show the variation of all the voltages with change of two variables D and k for Case I and II respectively. The 3-D surface plot gives the fitted function, whereas actual voltage values obtained from numerical solutions are shown in dots as 3-D discrete sequence data. It is to be noted that for clarity the variation in height of the 3-D plots has also been color coded with blue being the minimum and yellow indicating the maximum values. From the plots it can also be seen that the functions represent excellent fits.

V. SIMULATION AND EXPERIMENTAL RESULTS

A. COMPONENT DESIGN

In DCM operation the inductance for each of the three input boost inductors is calculated based on (1), which is a function of switching frequency, duty ratio, and load on the converter. The worst case scenario for inductor design in DCM would be for the lowest load resistance and for $D = 1/3$ when the converter is operating in Zone III. This would ensure DCM operation over the whole operating region of the converter. An inductance of 13.2 μH is used in this work for DCM analysis.

The intermediate switched capacitors are selected based on the maximum voltage stress over all the operating conditions as well as the rms current flowing through them. For the output capacitor, an additional criteria of selection is the desired ripple in the output voltage. Based on the operating range of

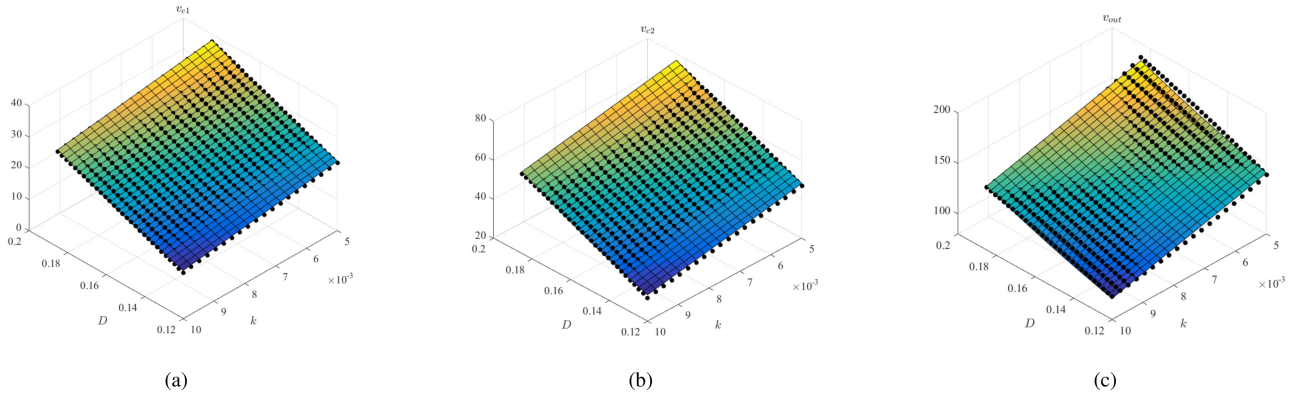

FIGURE 7. 3-D surface plot showing variation of voltages for different values of *D* and *k* obtained from MATLAB curve fit for Zone III, Case I operation (a) v_{c1}, (b) v_{c2}, (c) v_{out} for $v_{in} = 37\,V$. The variation in height of the 3-D plots has been color coded (blue and yellow correspond to minimum and maximum respectively). The black dots represent 3-D discrete sequence data showing the actual voltage values.

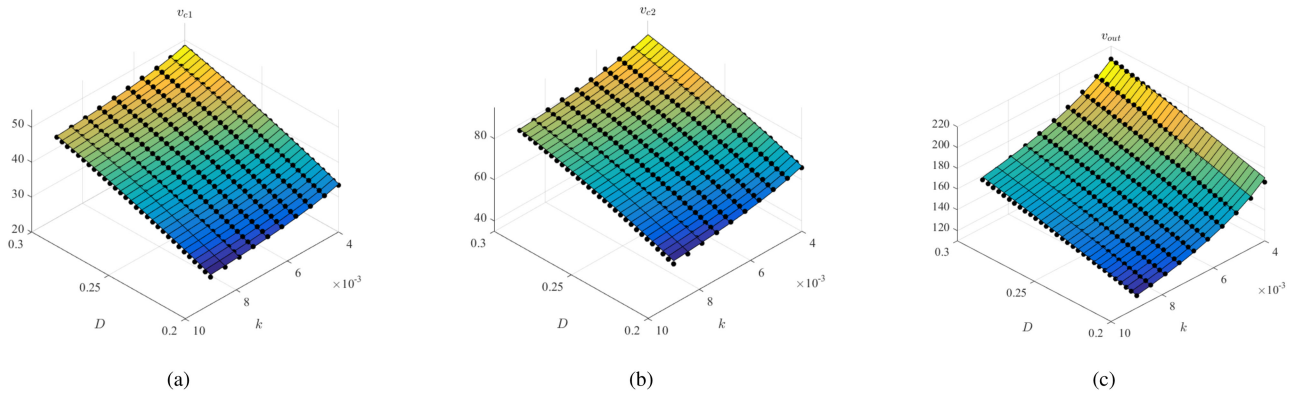

FIGURE 8. 3-D surface plot showing variation of voltages for different values of *D* and *k* obtained from MATLAB curve fit for Zone III, Case II operation (a) v_{c1}, (b) v_{c2}, (c) v_{out} for $v_{in} = 29\,V$. The variation in height of the 3-D plots has been color coded (blue and yellow correspond to minimum and maximum respectively). The black dots represent 3-D discrete sequence data showing the actual voltage values.

the converter, the voltage stress on the switching devices can be identified from Figs. 2 and 4, where the expressions for v_{c1}, v_{c2}, and v_{out} can be obtained from Section IV for different operating zones. It is to be noted that, as this work is focused on validating the converter's operation across all the operating regions, the devices are selected for the worst case voltage stress which is Zone III for a 3-phase EDR boost converter in DCM. However, for an optimized design for efficiency and power density, the converter can be designed to operate only in Zone I and II. This ensures the voltage stress on $Q_1 - Q_3$ is limited to only $1/3^{rd}$ of the output voltage, while still providing wide range of input-output voltage operation. The passive and active component details for the hardware setup are given in Table 5.

B. HARDWARE PROTOTYPE

A 300 W, 50 kHz Silicon based hardware prototype of a 3-phase EDR boost is designed for this study and is shown in Fig. 9. For steady state analysis, the converter output is kept constant at 200 V while the input voltage is varied from 15 V to 45 V to obtain results for different zones at variable power. The variable power is consistent with the microinverter operation which experiences different power based on the change of solar insolation. For validation at different power, the load resistor is varied to obtain desired output power for different zones, which results in different values of *k* in DCM operation.

TABLE V Component Details

Component	Parameters
C_1 , C_2 , C_3	6 μF, 6 μF, 4.7 μF
L_1 , L_2 , L_3	13.2 μH
Q_{s1} , Q_{s2} , Q_{s3}	IXFH72N30X3
D_1 , D_2 , D_3	C3D16065A

P42/29 core of material 3C91 from Ferroxcube is used to design each of the three inductors for DCM operation of 3-phase EDR boost converter. All the inductors are custom designed. Round copper wire is used to limit the DC

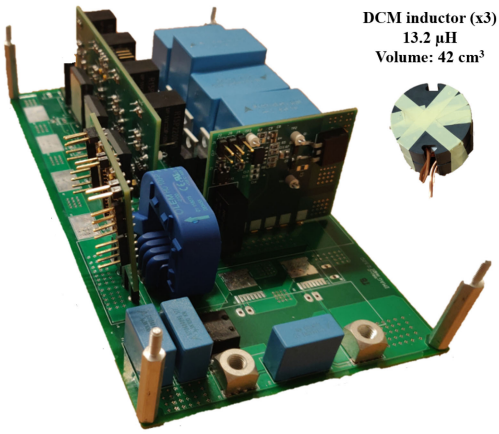

FIGURE 9. Silicon based experimental prototype for 3-phase EDR boost along with DCM inductor.

conduction losses in the inductors. Texas Instruments DSP TMS320F28379 has been used to generate the interleaved PWM signals for the three switches. LeCroy HDO8108A oscilloscope is used to capture the relevant waveforms and power analyzer YOKOGAWA WT3000 is used to measure the efficiency.

C. STEADY STATE WAVEFORMS IN DCM

Figs. 10(a) and 10(b) respectively show the experimental waveforms for Zones I and II operation under DCM. For Zone I the converter is operated with $D_1 = D_2 = D_3 = 0.7$ from 15 V to 200 V, 300 W with the load resistance of 134 Ω while for Zone II it is operated with $D_1 = D_2 = D_3 = 0.5$ from 20 V to 200 V, 300 W with the same load resistance as Zone I. The interleaved phase currents, device voltages, input current and voltage, and output voltage are shown for each zone. It can be seen that for both the zones, the inductor currents are equivalent in all three phases with similar slope, peak, and average values as discussed earlier. Further, the voltage stress for all the three devices can be observed to be $v_{out}/3$.

Figs. 11(a) and 11(b) respectively show the waveforms from hardware prototype for Cases I and II operation in Zone III under DCM for 200 V output. For Case I the converter is operated with $D_1 = D_2 = D_3 = 0.182$ with 45 V input at 200 W, with a load resistance of 200 Ω. For Case II it is operated with $D_1 = D_2 = D_3 = 0.288$ with 30 V input at 125 W with a load resistance of 320 Ω. The interleaved phase currents, and input, output and intermediate capacitor voltages are shown for each case.

It can be noted that high-frequency ringing is present in the experimental waveforms due to the circuit non-idealities. Thus simulation results are provided for further validation of the converter operation in Zone III, where operation is more complex. Figs. 12 and 13 present the corresponding simulation results for Cases I and II operation respectively showing all the relevant waveforms of the converter including the device voltage and current, which are not possible to probe in the experimental setup. It can be verified that the condition $3v_{in} < 2v_{c2} - v_{c1}$ is satisfied for Case II operation where the diode of Q_3 conducts [see Fig. 13(a) where I_{Q3} is negative for certain interval in every switching cycle] as expected. Also it can be seen that the presented simulation and experimental results are in good agreement with the analysis presented in the previous sections.

D. CLOSED LOOP WAVEFORMS IN DCM

A conventional PI controller is designed to regulate the output voltage of the 3-phase EDR boost converter in DCM. Closed loop operation of the converter is shown for both input voltage and output power changes. The input voltage change mimics the change in the PV panel voltage owing to partial shading condition for microinverter application. Figs. 14(a) and 14(b) respectively show the results corresponding to step-up from 15 to 25 V and step-down from 25 to 15 V of input voltage. Also the transitions between zones are shown: Zone I to Zone II in step-up and from Zone II to Zone I in step-down case. The zoomed in waveforms of the inductor current before and after the transient are shown for both the cases validating the zone transition. It can be observed that the transition is smooth with equal current sharing across the three phases with no significant transient spikes.

Similarly, experimental results with varying output power are shown in Fig. 15. The input voltage is kept constant at 20 V and the output voltage is regulated to 200 V at 50 kHz switching frequency. In Fig. 15(a), the output power is stepped up from 175 W to 300 W whereas waveforms corresponding to output power step down are shown in Fig. 15(b). In both the cases, the output voltage is regulated to the desired value as well as there is equal current sharing before and after the transient with no spikes. Design of sophisticated control to improve dynamic performance is part of future work.

E. LOSS BREAKDOWN AND EFFICIENCY

An experimental efficiency of respectively 94.93% and 95.14% are measured for Zones I and II while it is 95.3 % and 94.24 % respectively for Cases I and II operation in Zone III, all in DCM. The loss breakdown of the converter operating in all these operating regions is shown in Fig. 16 corresponding to the operating condition at which the experimental results are provided in Figs. 10 and 11. From Fig. 16 (which presents the loss breakdown in both % and absolute values) it can be observed that in all the regions, even with Si device at relatively high switching frequency, the MOSFET switching loss is less due to soft-switching operation during switch turn ON in DCM. However, due to higher input current as well as high current ripple, the conduction losses in MOSFETs, and diodes constitute the major portion of the total loss, all consistent with the expected operation in DCM. The inductors are designed for low conduction and core losses and their losses are estimated in ANSYS PExprt software.

A summary Table 6 is provided comparing the inherent current sharing capability, converter's gain, analytical and experimental gain and efficiency at 3 operating zones for DCM

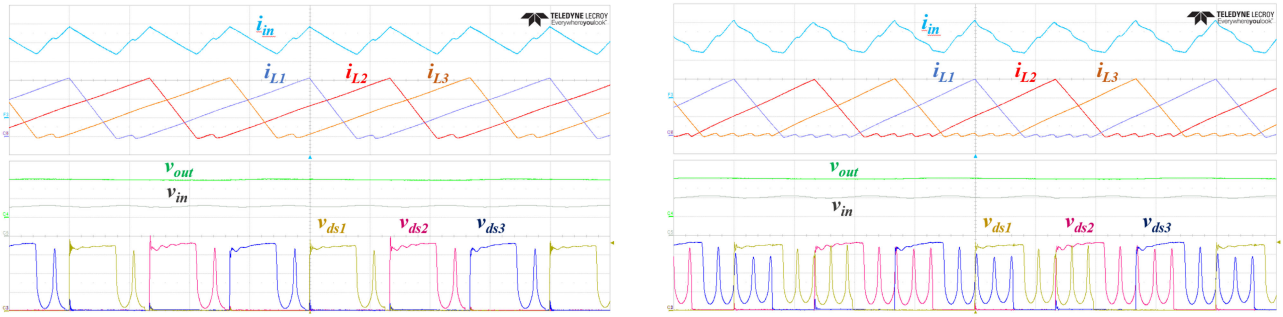

FIGURE 10. Waveforms for DCM operation from hardware (current: 5 A/div, v_{in} : 10 V/div, v_{out} : 100 V/div, v_{ds} : 20 V/div, time : 5 μs/div) of 3-phase EDR boost for (a) Zone I with $D_1 = D_2 = D_3 = 0.7$ operating from 15 V to 200 V, 300 W at 50 kHz switching frequency, (b) Zone II with $D_1 = D_2 = D_3 = 0.5$ operating from 20 V to 200 V, 300 W at 50 kHz switching frequency.

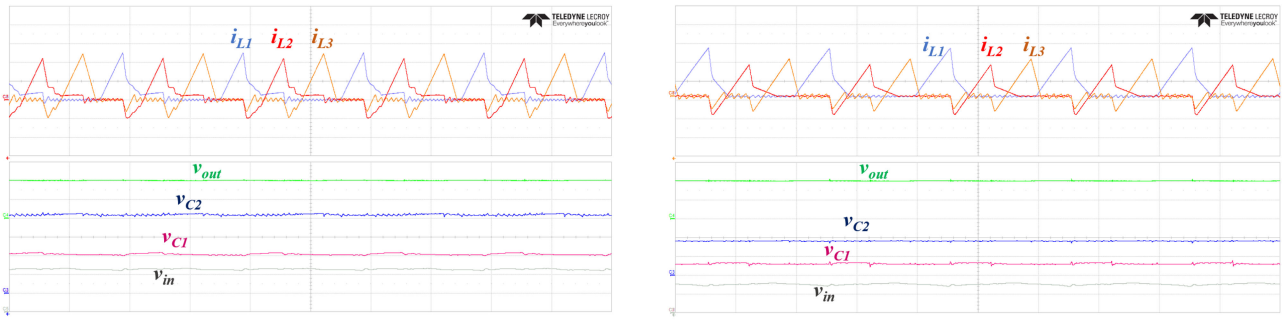

FIGURE 11. Waveforms for Zone III DCM operation from hardware at 50 kHz switching frequency (current: 5 A/div, v_{in}, v_{C1} : 20 V/div, v_{out} : 100 V/div, time : 10 μs/div) in 3-phase EDR boost for (a) Case I with $D_1 = D_2 = D_3 = 0.182$ operating from 45 V to 200 V, 200 W (v_{C2} : 20 V/div) (b) Case II with $D_1 = D_2 = D_3 = 0.288$ operating from 30 V to 200 V, 125 W (v_{C2} : 50 V/div).

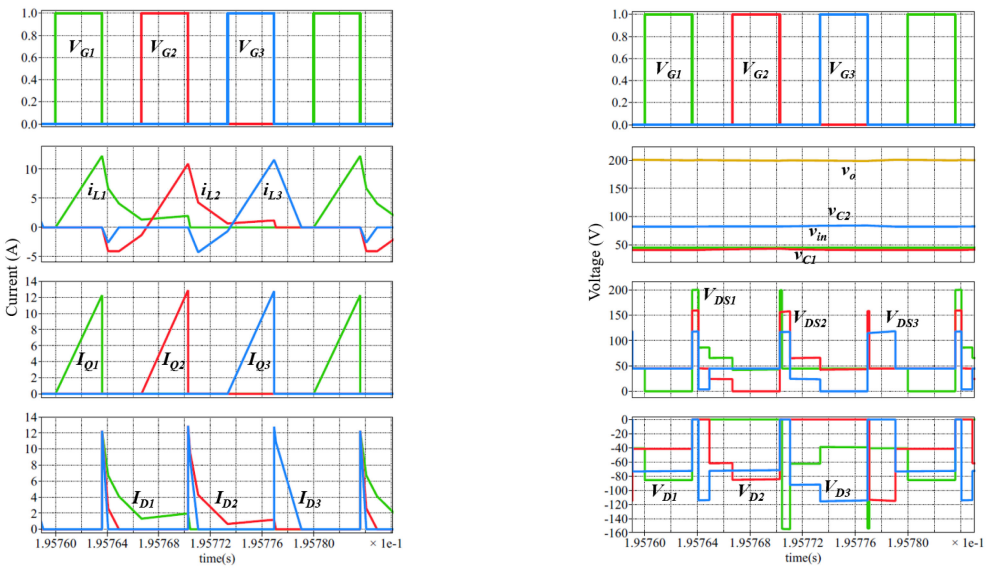

FIGURE 12. PLECS simulation waveforms for Case I Zone III 3-phase EDR boost corresponding to D1 = D2 = D3 = 0.182 operating from 45 V to 200 V, 200 W showing all the relevant waveforms.

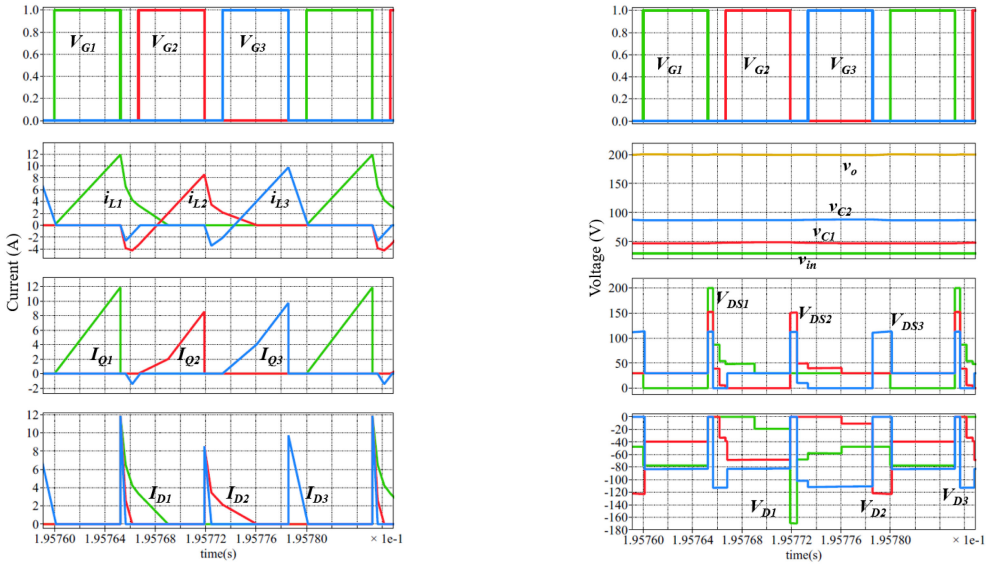

FIGURE 13. PLECS simulation waveforms for Case II Zone III 3-phase EDR boost corresponding to D1 = D2 = D3 = 0.288 operating from 30 V to 200 V, 125 W showing all the relevant waveforms.

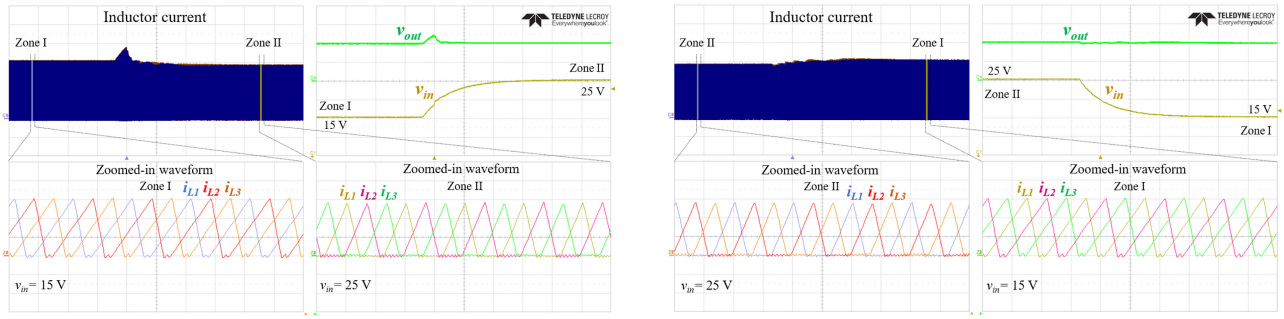

FIGURE 14. Waveforms for closed loop DCM operation from hardware at 50 kHz switching frequency, 200 V output voltage (current: 5 A/div, v_{in} : 5 V/div, v_{out} : 100 V/div, time : 100 *ms*/div) in 3-phase EDR boost for (a) Input voltage step up from 15 V (Zone I) to 25 V (Zone II) (b) Input voltage step down from 25 V (Zone II) to 15 V (Zone I).

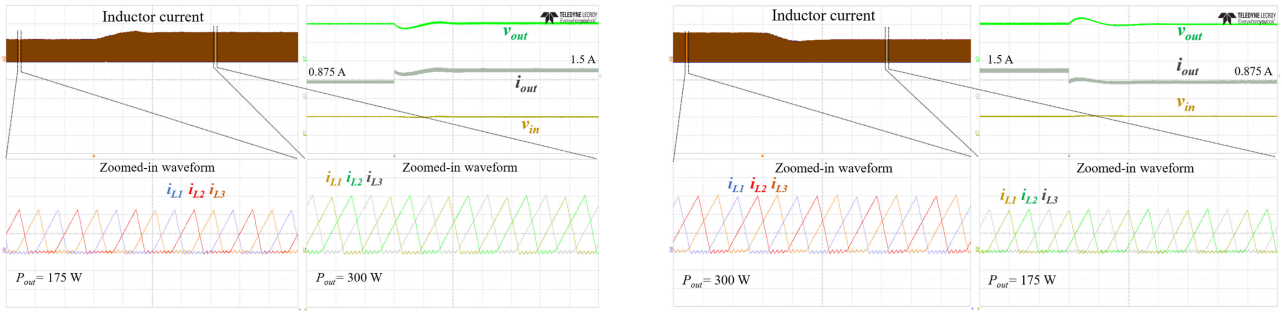

FIGURE 15. Waveforms for closed loop DCM operation from hardware at 50 kHz switching frequency, 200 V output voltage (i_L: 5 A/div, i_{out}: 1 A/div, v_{in} : 20 V/div, v_{out} : 100 V/div, time : 20 *ms*/div) in 3-phase EDR boost for (a) Output power step up from 175 W to 300 W (b) Output power step down from 300 W to 175 W.

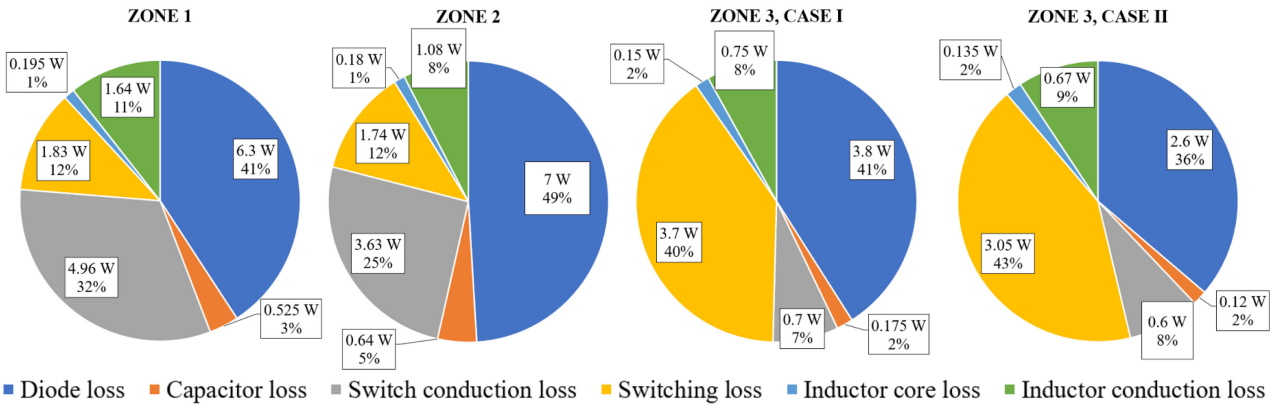

FIGURE 16. Loss breakdown for different operating regions in DCM.

TABLE VI Comparison of Analytical and Experimental Results of DCM Operation of 3-Phase EDR Boost

Operating zone	Inherent Current sharing?	Gain	k	Duty (D)	Exp. v_{out} (V)	Analyt. v_{out} (V)[@]	η_{pk} (%)
DCM Zone I	Yes	$1.5(1+\sqrt{1+\frac{4D^2}{3k}})$	0.0098	0.7	200	206.4	94.93
DCM Zone II	Yes	$1.5(1+\sqrt{1+\frac{4D^2}{3k}})$	0.0098	0.5	200	206.4	95.14
DCM Zone III*	No	$57.65D^2-213.54k+4.04$	0.0066	0.182	200	204.3	95.3
DCM Zone III+	No	$-18.97D^2+21.95D+\frac{0.012}{k}-0.74$	0.0041	0.288	200	207.5	94.24

* reported for Case I operation
+ reported for Case II operation
@ As the analytical model does not include the non-linearities of the devices, hence, there is a slight variation in the experimental and analytical values

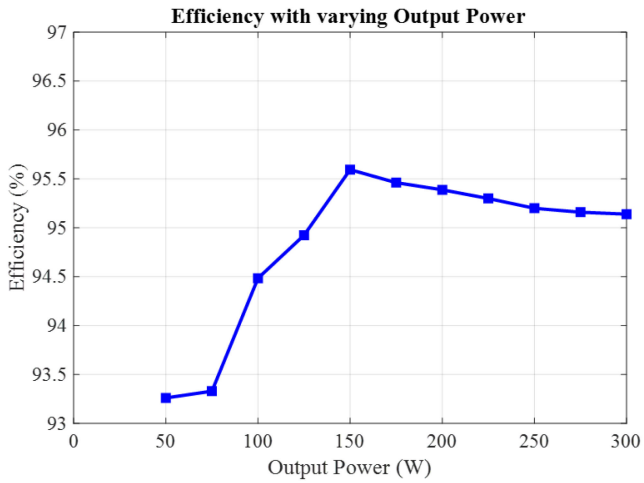

FIGURE 17. Experimental efficiency curve for DCM operation of 3-phase EDR with varying output power for 20 V to 200 V operation.

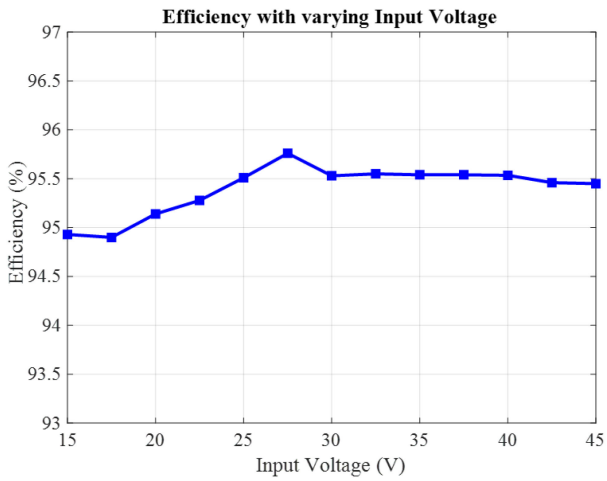

FIGURE 18. Experimental efficiency curve for DCM operation of 3-phase EDR with varying input voltage at 200 V, 300 W output.

operation. The measured efficiency for varying power operation is presented in Fig. 17. Here, the input and output voltage is fixed to 20 V and 200 V respectively. The efficiency curve with varying input voltage is shown in Fig. 18. The input voltage is varied from 15 V to 45 V while the output voltage is regulated to 200 V at 300 W. The peak efficiency achieved

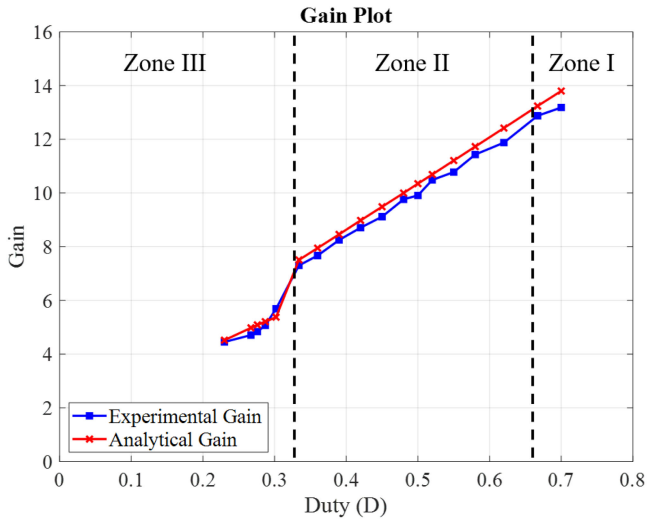

FIGURE 19. **Converter experimental and analytical gain in three zones of operation with varying duty for $k = 0.0098$.**

by the converter is 95.76% at 27.5 V input voltage. Also it can be seen from Fig. 18, the converter has efficiency more than 95% over a wide range of input voltage operation. Further it is to be noted, for optimal efficiency design, the converter can be designed to operate only in Zone I and II. This ensures the voltage stress on $Q_1 - Q_3$ is limited to only $1/3^{rd}$ of the output voltage (while still providing wide range of input-output voltage operation) and thus lower voltage rated devices could be used to minimize their conduction loss.

F. GAIN CURVE

A gain curve with experimental and analytical gain values is shown in Fig. 19 to verify the analytically derived gain equations in the three zones of operation. As the gain of the converter is dependent both on D and k, the value of k is kept constant to 0.0098 which corresponds to a load resistance of 134 Ω, and D is varied based on operating zone. For Zone III, experimental and analytical gain comparison is shown only for Case II, as to obtain other cases the value of k needs to be changed. As can be seen, both the analytical and experimental values match very closely across different zones, the slight difference in gain values is attributed to the non-idealities present in the hardware as the analytical expressions are obtained for ideal circuit.

VI. CONCLUSION

In this paper, EDR boost converter has been thoroughly studied for high step-up light load application in DCM operation. An extensive analysis of converter's DCM operating principles, key theoretical waveforms, and steady state circuit performance corresponding to all the possible zones of operation have been presented for 3-phase EDR boost converter. It is shown that inherent current sharing in three boost phases is possible in Zones I and II operation. For Zone III, multiple operating cases exist with different combination of operating modes. While it is straightforward to determine the converter gain in the first two zones, the gain expression for Zone III is obtained by curve fitting technique over the range of operating duty ratio D and DCM parameter k. The simplified gain and capacitor voltage expression is helpful in determining the voltage stress of the converter for all the operating regions. Further, a 360 W Si-based hardware prototype operating at 70 kHz is built to validate the analysis of the 3-phase EDR boost converter in DCM. Finally, the loss analysis is presented for all the operating zones in DCM.

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