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Development and Thorough Investigation of Dual-Band Wilkinson Power Divider for Arbitrary Impedance Environment

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ABSTRACT In the design and development of front-end communication systems, the arbitrary impedance environments are encountered frequently. In this article, a three-port dual-band equal power divider is proposed which also transforms all types of impedance environments at its ports inherently. The power divider is suitable for a wide range of arbitrary frequency ratios and impedance terminations at each of the input and output ports. A systematic design procedure with a design flow graph is provided. The closed-form design equations make the design process simple and quick for prototyping purposes. The proposed design approach enhances the design flexibility significantly with the presence of multiple independent variables. Design examples with distinct design specifications are provided to demonstrate the effectiveness and flexibility of the architecture. A prototype working at 1/2.6 GHz and with frequency-dependent complex load (FDCL) terminations at the input and output ports is fabricated and measured to validate the proposed architecture and design methodology. The proposed dual-band impedance transforming power divider exhibits controllable bandwidths, planar structure without any reactive element, compact size, and the ability to provide port matching for any real, complex, and frequency-dependent complex impedance terminations.

INDEX TERMS Frequency varying impedances, dual-band power divider, frequency-dependent impedance transformer, high frequency ratio, impedance matching, impedance transforming power divider, microstrip power dividers, transmission line.

I. INTRODUCTION

Traditionally, power divider (PD) found extensive usefulness in RF/Microwave communication systems such as antenna feeder networks, push-pull amplifiers, mixers, baluns, I/Q vector modulators, and phased arrays for signal-division or combination [1]–[3]. Subsequently, there has been an increased interest in the design and development of multi-band PDs owing to the rapid advancements in the multi-band/multi-standard communication systems [4]–[6]. However, emergence in advanced wireless technology has also seen a recent surge in impedance transforming PDs [7]–[10]. This has been necessitated by the fact that often there exists a wide impedance variations between the ports of PDs and interconnecting circuit blocks. These impedance variations conventionally require a real-to-real [11]–[13] or real-to-complex [14] or real-to-frequency dependent complex impedance transformation [15]–[17].

Therefore, high inherent impedance transformation capability is the need of the modern communication system. These impedance transforming power dividers (ITPDs) enable the overall circuit miniaturization, too, by eliminating the additional impedance transformers at the ports in a communication system. A number of power divider schemes with distinct features and functionalities exist in the literature [7]–[10],

[18]–[22]. In brief, there are either single-band ITPDs with real or complex impedances [7]–[10], [18], [19] or dual-band ITPDs with only real impedances [20]–[22] at the ports. The PDs with unequal port terminations between the input (source) and output (load) ports are reported [18], [19] but these designs have addressed only real-to-real impedance transformation at the ports and for a single frequency of operation. A power divider with equal and complex terminations at the output ports propounds the need of reactive components to provide the isolation between the output ports [23]. For the operations at RF frequencies, these components are needed to transform to open/short circuited stubs. The elimination of complex isolation circuits with lumped components has been addressed in a recent single-band PD, in which the impedance matching for complex termination at ports is integrated with the overall design [24]. However, these reports are limited to single frequency operation only. Importantly, these reports are limited to equal impedances at all the ports. There is one recent report on dual-band PD which utilizes the complex load for the matching purposes [25]. However, the ports are terminated to only equal and real impedances. Overall, the reported designs have not been explored for dual-band operation including the associated design challenges and performance limitations. For example, one key design challenge encountered by a dual-band design will be the arbitrary variations in impedances at the two design frequencies.

In this paper, therefore, existing knowledge available in literature has been utilized and appropriate amendments have been done in the design to address the above mentioned constraints. In essence, a dual-band PD with FDCL impedance transformations at widely separated arbitrary frequencies is proposed in this paper to meet the requirements of emerging communication applications. The simplified architecture with the systematic design procedure is presented to overcome the above mentioned limitations. The contributions of the proposed dual-band impedance transforming power divider (DBITPD) can be listed as: 1) its ability to operate at the arbitrary frequency ratios; 2) its ability to account for arbitrary terminated real, complex, or FDCL port impedances; 3) systematic design methodology with closed-form design equations; 4) absence of reactive elements for real or complex port terminations; 5) easy realization in microstrip technology; 6) a simple and planar structure; and 7) availability of the independent design variables for the enhanced design flexibility. Sections II and III develop the theoretical postulations of the proposed concept, whereas Section IV augments the novel and significant features of the proposed DBITPD. Section V provides the experimental validation of a fabricated prototype. Section VI concludes the paper.

II. DESIGN METHODOLOGY

The proposed architecture has been developed by making use of the following:

- **a Wilkinson Power Divider (WPD)-** The conventional WPD architecture [27] provides the equal power division with all the real and equal ports. The operation is limited to single frequency only.
- **a T-Type Structure-** The T-type structure (TTS) [28] can transform the complex output port impedances to a real input port termination. However, the transformation to a fixed and real input port faces challenges for a wide range of arbitrary impedances.

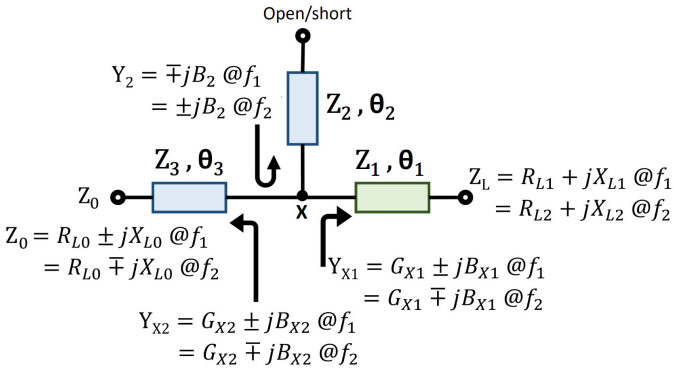


FIGURE 1. Utilized design scheme in this work.

At the outset, there have been several modifications in the conventional WPD architecture to make it useful for either the dual-band operation or impedance transformation [23], [24], [26]. However, the presented work in this paper significantly advances the microstrip compatibility for the arbitrary impedances at the two arbitrary design frequencies. The proposed design methodology contributes to improving the range of arbitrary frequency ratios and impedance terminations with enhanced design flexibility. In this design methodology, the TTS transforms the FDCL (Z_L) to a complex conjugate load (CCL), i.e. Z_0, as depicted in Fig. 1. This setup provides an additional flexibility to the proposed power divider as the transformed impedance Z_0 can be tuned in case the design parameters are not realizable. This discussion is further elaborated in the design analysis in the next section which, overall, enhances the design flexibility of the DBITPD for the increased range of the input and output port impedances.

III. PROPOSED DESIGN AND ITS ANALYSIS

The proposed dual-band equal PD is depicted in Fig. 2. The characteristic impedances and electrical lengths of the proposed DBPD, shown in Fig. 2, are denoted by the corresponding Z and θ, respectively. The TLs with respective characteristic impedances Z_{a2} and Z_{b2} are either short- or open-circuited stubs. The input port (port 1) is terminated with source impedance Z_S and the output ports (ports 2 and 3) are terminated with load impedance Z_L. The impedances Z_S and Z_L are uncorrelated FDCLs at the two arbitrarily chosen design frequencies and can be defined as (1) and (2), respectively.

$$Z_S = \begin{cases} R_{S1} + jX_{S1}\ @f_1 \\ R_{S2} + jX_{S2}\ @f_2 \end{cases} \tag{1}$$

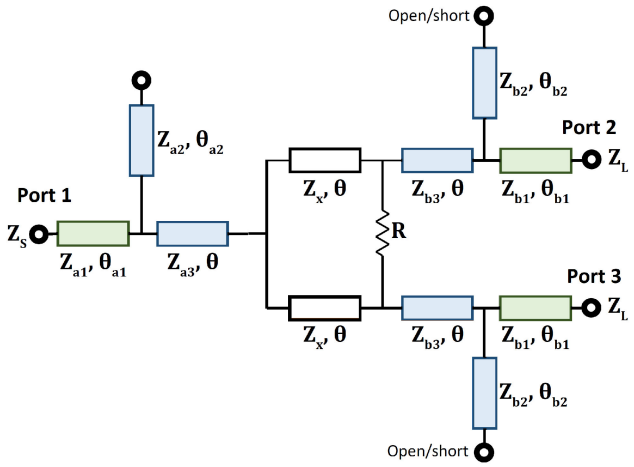


FIGURE 2. Schematics of the proposed DBITPD.

$$Z_L = \begin{cases} R_{L1} + jX_{L1} \ @f_1 \\ R_{L2} + jX_{L2} \ @f_2 \end{cases} \tag{2}$$

It can now be seen that the TTS is formed at all the three ports which is revisited here for dual-band operation [28]. The TTS is depicted in Fig. 1 for its analysis as a dual-band impedance transformer at frequencies f_1 and f_2 ($f_1 \leq f_2$) with frequency ratio ($r = f_2/f_1$). Here, left port has a CCL admittance, i.e., $Y_0(Z_0) = G_{L0}(R_{L0}) \pm jB_{L0}(X_{L0})$ $@f_1$ and $Y_0 = G_{L0} \mp jB_{L0}$ $@f_2$, and right port has FDCL admittance, i.e., $Y_L = G_{L1} + jB_{L1}$ $@f_1$ and $Y_L = G_{L2} + jB_{L2}$ $@f_2$.

The TL with parameters Z_1 and θ_1, as depicted in Fig. 1, can be computed to transform the FDCL at right port to a CCL of Y_{X1} for the chosen frequencies f_1 and f_2 [28]. Subsequently, the dual-band TL segment with characteristic impedance Z_3 provides matching between the real part of the left port admittance Y_0, i.e., G_{L0}, and the real part of Y_{X1} using TL theory, which translates to (3), at the two arbitrary design frequencies f_1 and f_2. The terms Y_{X1} and Y_{X2} are both CCLs with the same real parts at node X. The imaginary terms of these CCLs at node X are cancelled by the dual-band stub possessing the characteristic impedance of Z_2 and electrical length of θ_2. This stub fulfills the condition (4) at both design frequencies f_1 and f_2.

$$G_{X1} = G_{X2} \tag{3}$$

$$B_2 = -(B_{X1} + B_{X2}) \tag{4}$$

The discussed design scheme is utilized to analyse the proposed DBITPD. A closer look at the proposed architecture in Fig. 2 reveals that it is symmetric and, therefore, can be decomposed into even- and odd-mode equivalent circuits, as shown in Figs. 3 and 4, for simplifying the design analysis.

A. ODD-MODE ANALYSIS

The simplified odd-mode equivalent circuit of the proposed PD, depicted in Fig. 3, includes the TTS and the portion containing $R/2$ and the TL segment with parameters Z_X and

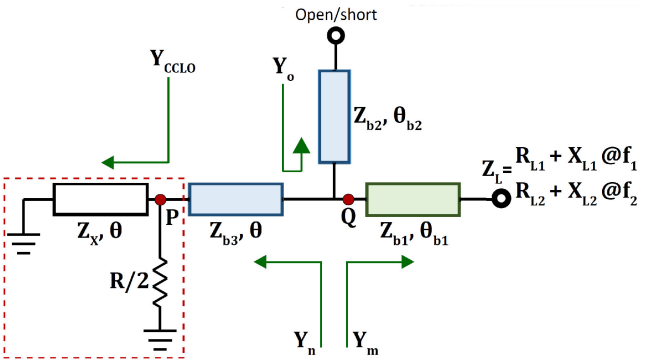


FIGURE 3. Odd-mode equivalent circuit of the DBITPD.

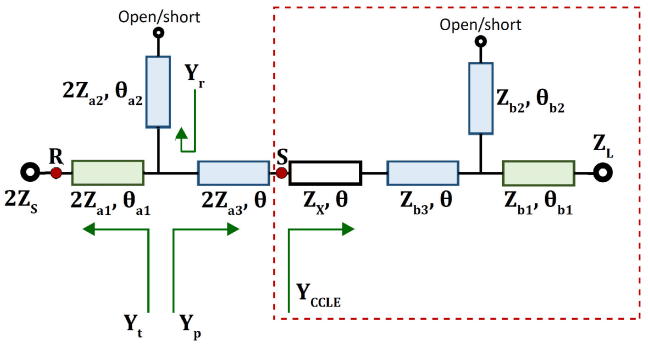


FIGURE 4. Even-mode equivalent circuit of the DBITPD.

θ (in red dotted box). In essence, this circuit consists of a T-network terminated with FDCL Z_L on the right side. The left side of the T-network is terminated in a CCL at node P, expressed in (5), created by the combination of a resistor ($R/2$) and a short-circuited stub (Z_X, θ). Importantly, it will be clear in the next-coming section that the term Z_X is an independent design parameter, whereas θ must follow (6) for dual-band operation [20]. Furthermore, the terms Z_{b1} and θ_{b1} in the TTS can be calculated using (7) and (8) to get a CCL, denoted as Y_m, at point Q [28]. As depicted in Fig. 3, the TL with parameters Z_{b3} and θ transforms the real part of Y_{CCLO} in such a way that the real part of Y_n equals the real part of Y_m. Therefore, the expression of Z_{b3} can be deduced by equating the real parts of Y_m and Y_n, expressed in (9). Again, for dual-band functionality the electrical length θ follows (6), where n is an integer [41].

$$Y_{CCLO} = \frac{2}{R} - \frac{j}{Z_X \times \tan\theta} \tag{5}$$

$$\theta = \frac{(1+n)\pi}{1+r} \tag{6}$$

$$Z_{b1} = \left[R_{L1}R_{L2} + X_{L1}X_{L2} + \frac{X_{L1} + X_{L2}}{R_{L2} - R_{L1}}(R_{L1}X_{L2} - R_{L2}X_{L1}) \right]^{\frac{1}{2}} \tag{7}$$

$$\theta_{b1} = \frac{n\pi + \tan^{-1}\frac{Z_1(R_{L1}-R_{L2})}{R_{L1}X_{L2}-R_{L2}X_{L1}}}{1+r},\ n\text{: Integer} \tag{8}$$

$$Z_{b3} = \left[\sqrt{\frac{\mathrm{Re}\{Z_{CCLO}\}(1+\tan^2\theta)}{\mathrm{Re}\{Y_m\}} - \mathrm{Re}\{Z_{CCLO}\}^2} - \mathrm{Im}\{Z_{CCLO}\}\right] \times \cot\theta \tag{9}$$

At this stage, the real parts are matched and the imaginary parts of Y_n and Y_m are canceled by an open-/short-circuited stub, having parameters Z_{b2} and θ_{b2} in Fig. 3, capable of synthesizing desired susceptances at the two design frequencies. The admittance offered by the stub, Y_o, should be conjugate to the combination of imaginary parts of Y_m and Y_n. The admittance offered by the stub can be given by (10) and the expression of Z_{b2} is given in (12). Again, the electrical length θ_{b2} should follow (13) for its dual-band operation and cancellation of the imaginary admittance at the two different frequencies. Here, an initial value of n should be 0 for the miniaturized TL lengths and design, however, subsequent increment should be done to achieve the design parameters in the realizable range in microstrip technology, i.e., the interval [20, 150]Ω.

$$Y_o = \frac{j\tan\theta_{b2}}{Z_{b2}} \text{ for open condition}$$

$$Y_o = -\frac{j\cot\theta_{b2}}{Z_{b2}} \text{ for short circuit} \tag{10}$$

$$Y_o = -j\{\mathrm{Im}\{Y_m\} + \mathrm{Im}\{Y_n\}\} \tag{11}$$

$$Z_{b2} = -\frac{\tan\theta_{b2}}{\mathrm{Im}\{Y_m\} + \mathrm{Im}\{Y_n\}} \text{ for open condition}$$

$$Z_{b2} = \frac{\cot\theta_{b2}}{\mathrm{Im}\{Y_m\} + \mathrm{Im}\{Y_n\}} \text{ for short condition} \tag{12}$$

$$\theta_{b2} = \frac{(1+n)\pi}{1+r} \tag{13}$$

It is interesting to note that the above discussed design procedure has multiple sets of solution. This is due to the fact that, a) term Y_{CCLO} has two independent design parameters Z_X and R which can be tuned to a wider range to achieve the realizable design parameters, b) the selection of "n," and, c) short- or open-circuited stub enhances the design freedom. This essentially provides the superior design flexibility to the proposed power divider.

B. EVEN-MODE ANALYSIS

The even-mode equivalent circuit of the proposed PD is shown in Fig. 4. Again, the effective circuit includes the TTS with TL characteristic impedances $2Z_{a1}$, $2Z_{a2}$, and $2Z_{a3}$. The TTS is terminated with an FDCL of $2Z_S$ at point R, effectively. All the design parameters of the structure (inside a red dotted box) connected with the TTS at point S are known from the odd-mode analysis. It is identified from the odd-mode analysis that the term Y_{CCLE} forms a complex conjugate quantity at

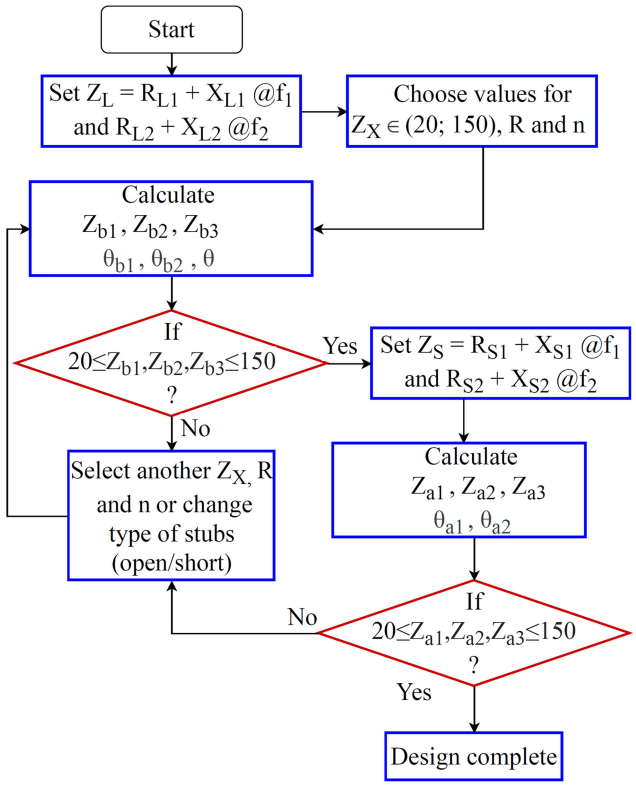


FIGURE 5. Flow chart for design of the proposed DBITPD.

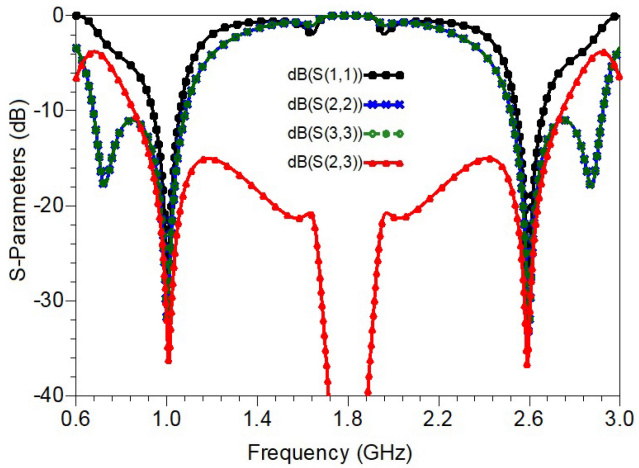
the two frequencies and, therefore, behaves as a CCL termination for the TTS. This effectively creates the scenario as in odd-mode analysis, and, therefore, the design parameters for the even-mode circuit given in equations (14)-(20) also have similar formulations with the appropriate changes in the design variables.

Moreover, to obtain the realizable design parameters for a wide variety of arbitrary and different port impedances, multiple solution sets discussed in odd-mode analysis can be reviewed. This design procedure is also depicted in a systematic design flow graph in the next section.

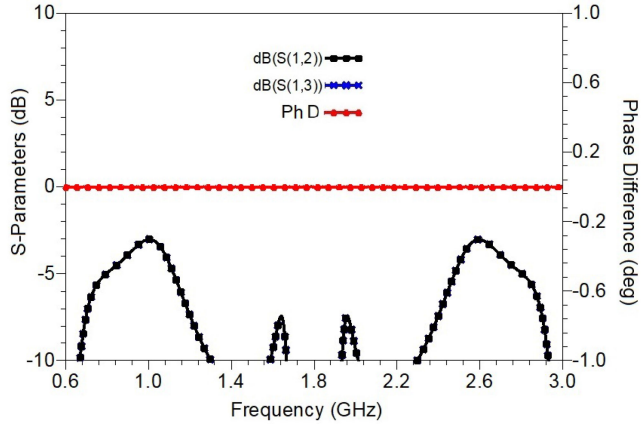
$$Z_{a1} = \left[R_{S1}R_{S2} + X_{S1}X_{S2} + \frac{X_{S1}+X_{S2}}{R_{S2}-R_{S1}}(R_{S1}X_{S2} - R_{S2}X_{S1})\right]^{\frac{1}{2}} \tag{14}$$

$$\theta_{a1} = \frac{n\pi + \tan^{-1}\frac{Z_{a1}(R_{S1}-R_{S2})}{R_{S1}X_{S2}-R_{S2}X_{S1}}}{1+r},\ n:\ \text{Integer} \tag{15}$$

$$Z_{a3} = \left[\sqrt{\frac{\mathrm{Re}\{Z_{CCLE}\}(1+\tan^2\theta)}{\mathrm{Re}\{Y_t\}} - \mathrm{Re}\{Z_{CCLE}\}^2} - \mathrm{Im}\{Z_{CCLE}\}\right] \times \cot\theta \tag{16}$$



(a) Results for S_{11}, S_{22}, S_{33} and S_{23}.



(b) Results for S_{12}, S_{13}, and, phase difference (PhD).

FIGURE 6. Calculated results for the design example.

$$Y_r = \frac{j\tan\theta_{a2}}{2Z_{a2}} \text{ for open condition}$$

$$Y_r = -\frac{j\cot\theta_{a2}}{2Z_{a2}} \text{ for short circuit} \tag{17}$$

$$Y_r = -j\text{Im}\{\{Y_t\} + \text{Im}\{Y_p\}\} \tag{18}$$

$$Z_{a2} = -\frac{\tan\theta_{a2}}{\text{Im}\{Y_t\} + \text{Im}\{Y_r\}} \text{ for open condition}$$

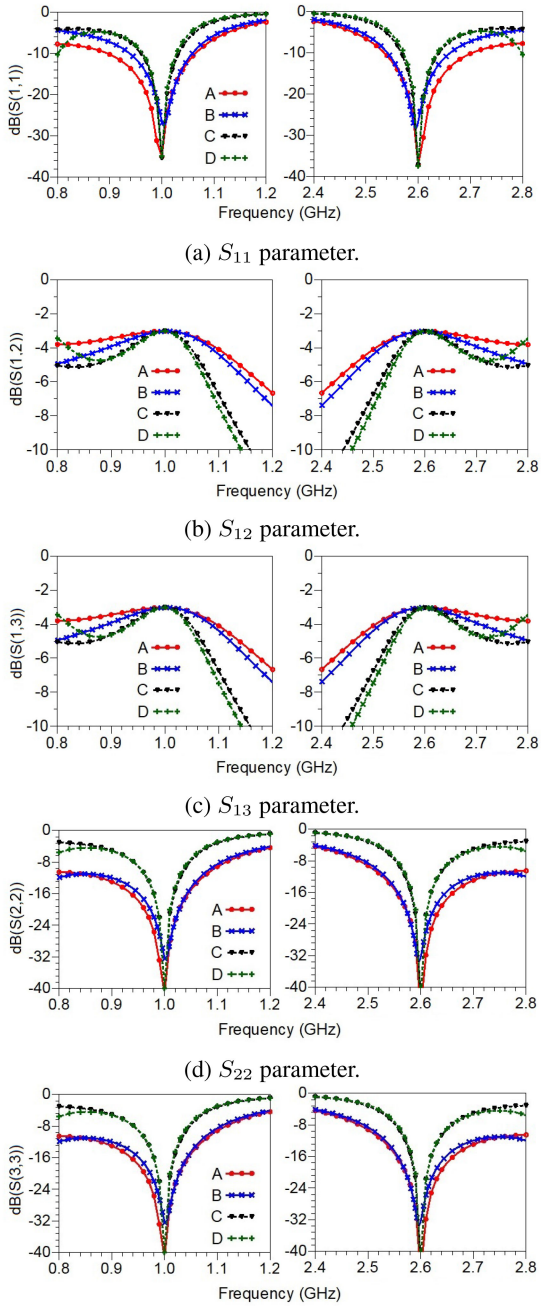
$$Z_{a2} = +\frac{\cot\theta_{a2}}{\text{Im}\{Y_t\} + \text{Im}\{Y_r\}} \text{ for short condition} \tag{19}$$

$$\theta_{a2} = \frac{(1+n)\pi}{1+r} \tag{20}$$

IV. DESIGN PROCEDURE AND DISCUSSIONS

A. DESIGN FLOW CHART

The complete procedure to design the proposed DBITPD is depicted by the flow chart provided in Fig. 5. This design flow is explained using a design example intended for frequency of operations of 1 GHz and 2.6 GHz. The source and load impedances are assumed as $Z_S = 54.1 + j8.6$ @1 GHz / $Z_S = 70.8 + j5.2$ @2.6 GHz and $Z_L = 54.8 + j26.4$ @1 GHz / $Z_L = 93.9 + j68.3$ @2.6 GHz. Then, the parameters Z_X and R are chosen independently to be 100 Ω each to design the proposed PD. Subsequently, the design parameters Z_{b1}, θ_{b1}, Z_{b3}, θ, Z_{b2}, and θ_{b2} are calculated as 100 Ω, 30°, 78.5 Ω, 50°, 130.5 Ω, and 50° using (6)–(9), and (12)–(13), respectively. It should be noted here that Z_{b1}, Z_{b2}, and Z_{b3}



(a) S_{11} parameter.

(b) S_{12} parameter.

(c) S_{13} parameter.

(d) S_{22} parameter.

(e) S_{33} parameter.

FIGURE 7. Bandwidth comparison of the proposed DBITPD with different combinations of the stubs. A: short-circuited stub (SCS) at source and open-circuited stub (OCS) at load, B: OCS at source and OCS at load, C: SCS at source and SCS at load, and D: OCS at source and SCS.

TABLE 1. Design Examples of the Proposed DBITPD for Distinct Specifications, $f_1 = 1$ GHz, (Open): Open-Circuited Stub; (Short): Short-Circuited Stub

Design Parameters	Case-1 (r = 2.0)	Case-2 (r = 2.6)	Case-3 (r = 2.6)	Case-4 (r = 3.0)	Case-5 (r = 3.5)	Case-6 (r = 6.2)
$Z_S\Omega$ @f_1 GHz $Z_S\Omega$ @f_2 GHz	30 + j0 30 + j0	54.1 + j8.6 70.8 + j5.2	85 + j17 70 + j5	83.6 + j12.1 110 + j21.4	36.5 - j10.6 42.9 + j10.1	60.9 + j3.3 73.7 - j3.5
$Z_L\Omega$ @f_1 GHz $Z_L\Omega$ @f_2 GHz	200 + j0 200 + j0	54.8 + j26.4 93.9 + j68.3	68 + j42.5 40 + j25	65 + j22.3 115.9 + j53.4	153.1 + j59.5 164.7 + j50.8	141.3 + j24.8 116.6 + j26
$Z_{a1}\Omega, \theta^\circ_{a1}$	52.5, 60	60, 70	84.6, 33.63	100.17, 24.97	37.3, 36.5	66.95, 33.6
$Z_{a2}\Omega, \theta^\circ_{a2}$	139.1, 60 (Short)	65, 150 (Open)	83.6, 50 (Short)	159.9, 45 (Open)	145.9, 120 (Open)	62.82, 150 (Short)
$Z_{a3}\Omega, \theta^\circ$	39.5, 60	32.25, 50	35.2, 50	44.9, 45	20, 40	42.4, 25
$Z_x\Omega, \theta^\circ$	100, 60	100, 50	125, 50	100, 45	110.8, 40	100, 25
$Z_{b1}\Omega, \theta^\circ_{b1}$	110.1, 60	100, 30	61.5, 75	100.15, 24.97	95.5, 46.44	124.6, 35.55
$Z_{b2}\Omega, \theta^\circ_{b2}$	128.4, 60 (Short)	130.49, 50 (Open)	73, 150 (Open)	114.2, 45 (Open)	106.3, 160 (Open)	42.88, 25 (Open)
$Z_{b3}\Omega, \theta^\circ$	64.3, 60	78.5, 50	54.7, 50	66.5, 45	70.4, 40	79.13, 25
$R\,\Omega$	100	100	100	100	185	100

are within the realizable range. Another important point to note is that in this case an open-circuited stub with the initial value of n, i.e., $n = 0$ is able to provide a realizable Z_{b2}. The next step of the design according to the flow chart entails the calculation of the design parameters θ, Z_{a1}, θ_{a1}, Z_{a3}, Z_{a2}, and θ_{a2} using equations (6), (14)–(16), and (19)–(20), respectively. The corresponding values come out to be 60 Ω, 70°, 32.25 Ω, 50°, 65.02 Ω, and 150°, respectively. Once again, it is important to mention that an open circuited stub with $n = 3$ provides realizable Z_{a3} in this example. The other parameters Z_{a1} and Z_{a3} are within the realizable limit. This completes the design of the PD considering that all the calculated design parameters are realizable and then a simulation was carried out and the achieved results are depicted in Fig. 6.

The plots in Fig. 6 provides good clarity about the performance and behavior of the dual-band PD proposed in this paper. Figure 6(a) demonstrates that the matching at all the ports (S_{11}, S_{22}, and, S_{33}) and the isolation between the two output ports (S_{23}) of the DBITPD is achieved at the two design frequencies of 1 GHz and 2.6 GHz. In essence, the matching at the output ports is in perfect consonance, as is apparent from the fully overlapped S_{22} and S_{33}. The Fig. 6(b) provides the information about the output power (S_{12} and S_{13}) and the phase difference, (i.e., $\Delta\phi = \phi(S_{12}) - \phi(S_{13})$), at the two design frequencies. It can be clearly seen that no difference exists in the magnitude of S_{21} and S_{31} and, therefore, the output power division is equal at both design frequencies. The phase difference is also maintained at 0° for a wide range of frequencies including the design frequencies. These results are a clear testament to the proposed design methodology for the proposed DBITPD.

B. SELECTION OF STUBS FOR OPERATIONAL BANDWIDTH

It is observed that the presence of the stubs can control the bandwidth performance of the PD [27], and therefore the bandwidth performance of the presented design example for all the combinations of the open- or short-circuited stubs are studied. It should be noted here that the choice of open- or short-circuited stubs is limited to either the input port or the output port only and not between the two output ports (ports 2 and 3) to maintain the symmetry. Therefore, the possible configurations are short-circuited stub at the source and open-circuited stub at the load (case-A), open-circuited stub at the source and open-circuited stub at the load (case-B), short-circuited stub at the source and short-circuited stub at the load (case-C), and open-circuited stub at the source and short-circuited stub at the load (case-D). The calculated results of the presented design example with all the four cases are demonstrated in Fig. 7, where A, B, C, and D are indicated for their respective cases. As depicted in Fig. 7, the bandwidth performance of the proposed DBITPD for case-A (Fractional bandwidth (FBW) of approx. 17%) is more than double in comparison to case-D (FBW of approx. 7%). It is important to note that the bandwidth performance of the DBITPD at these combinations of stubs may also vary depending on the type of FDCLs, CCLs, or real impedances and its variation over the frequency ranges.

C. DESIGN EXAMPLES

To further assess the effectiveness of the proposed architecture, six distinct design examples, including the example discussed in Section IV-A, are considered. The corresponding design parameters are given in Table 1. The design examples demonstrate the cases with high impedance transformation at high frequency ratios of $r = 2$, $r = 2.6$, $r = 3.0$, $r = 3.5$, and $r = 6.2$. It is apparent from Table 1 that all the design parameters are realizable in microstrip technology. A very high impedance transformation of 6.6 is presented in case-1. This case also demonstrates the effectiveness of the proposed ITPD for the real impedances. The design examples of case-2 to case-6 are presented for the arbitrary FDCL port impedances at the arbitrary frequency ratios. It should be noted here that several arbitrarily chosen impedance values of these design cases are not realizable with the state-of-the-art impedance transformers [28]–[30]. Additionally, the impedance values of case-3 fall under the forbidden range of classical complex impedance transformers [31]. Interestingly, the proposed design not only provides the dual-band power division but provides the inherent impedance transformation for arbitrary FDCL impedances at the two arbitrary design frequencies

TABLE 2. Measurement Results of the Fabricated Prototype, AI: Amplitude Imbalance, PI: Phase Imbalance

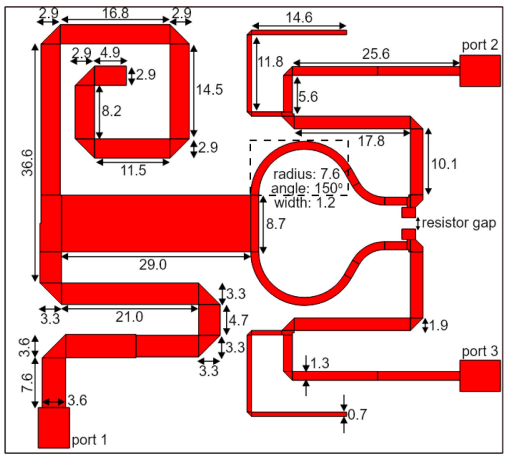
Measure	1 GHz	2.6 GHz	Measure	1 GHz	2.6 GHz
S_{11} (dB)	-31.78	-27.86	S_{23} (dB)	-25.7	-19.65
S_{22} (dB)	-32.36	-26.59	S_{33} (dB)	-32.09	-30.19
S_{21} (dB)	-3.2	-3.6	S_{31} (dB)	-3.2	-3.6
PI (°)	-0.3	0.4	FBW	16%	13.1%

too. This is, therefore, safe to convey that the proposed design is capable of overcoming the problems inherent with the other state-of-the-art impedance transformers in addition to the unique features within the WPD architecture. The design flexibility of the proposed ITPD is demonstrated by designing a PD at concurrent high impedance transformation (a maximum ratio of 2.32 for the real parts and 7.43 for the imaginary parts of Z_S and Z_L) and high frequency ratio of 6.2 in case-6. These examples demonstrate the versatility of the proposed design technique and validate that the functionality is suitable for a wide range of design specifications for arbitrary port impedances and frequency ratios.

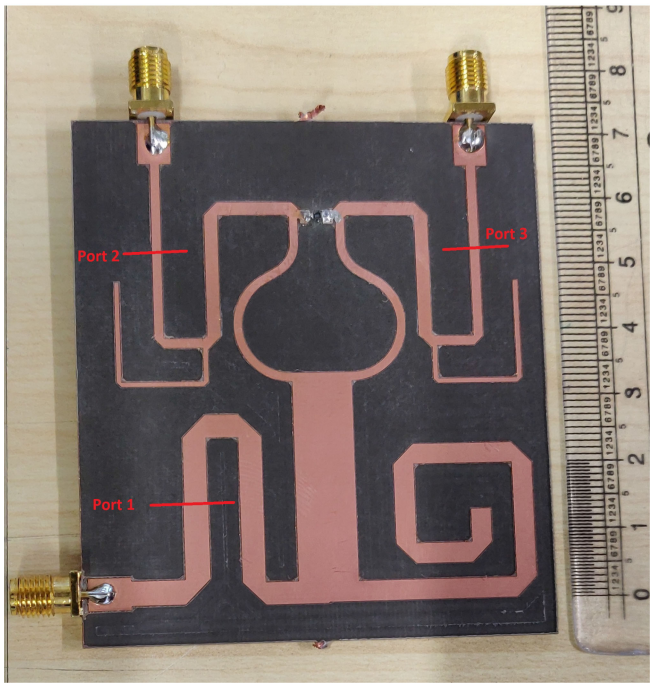
V. PROTOTYPE AND EXPERIMENTAL RESULTS

To experimentally verify the proposed design technique, the case-2 of the design examples is evaluated. A micro-strip prototype of the design example is fabricated on RT/Duroid 5880 substrate. The substrate has a thickness of 1.58 mm, relative permittivity (ϵ_r) of 2.2 and dissipation factor (tan δ) of 0.0009. The substrate is laminated with 35 μm thick copper on both the sides of the substrate. As per the specifications, the FDCL impedances at all three ports are synthesized using the combination of a TL and 50 Ω SMA connector individually. The source termination Z_S is synthesized by a combination of a micro-strip line of width 3.6 mm and length of 18.4 mm and a 50 Ω SMA connector. The load termination Z_L is synthesized by a combination of a micro-strip line of width 1.4 mm and length of 12.6 mm and a 50 Ω SMA connector. As per the availability in the lab, the isolation resistor of 100 Ω (part no. CRCW0603100RFKTA) is used. The layout, including these synthesized ports, is simulated in Keysight ADS and the optimizations are done to compensate for the anomaly associated with the resistor, resistor gap, junction discontinuities, bends, etc. The layout of the fabricated PD with the details on dimensions is depicted in Fig. 8 with an overall size of 64.9 mm × 69.6 mm, which includes the dimensions of the synthesized ports.

The fabricated prototype is evaluated using a Keysight vector network analyzer, and the measurement results are compared with the EM simulated result in Fig. 9. Apparently, the measurement results, denoted by M in suffix, and the EM simulated results, denoted by E in suffix, are in very good agreement. The impedance matching at all the ports and the isolation between the two output ports of the PD are depicted in Fig. 9(a), whereas the insertion loss at the two output ports and the phase difference between the two output ports are depicted in Fig. 9(b). The measurement results at the design frequencies are listed in Table 2. The amplitude imbalance



(a) Layout design (all the dimensions are in mm)



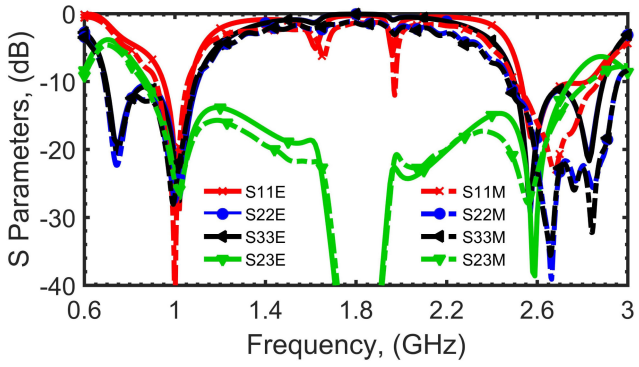
(b) Prototype of DBITPD on RO5880 Substrate

FIGURE 8. Layout and photograph of the fabricated prototype with FDCL port terminations.

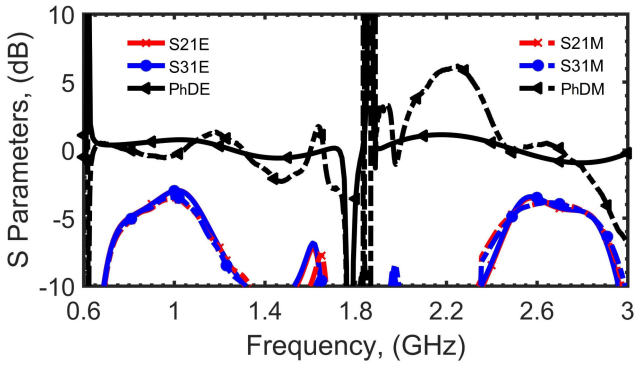
(AI) is the difference between the magnitudes of the signals present at the output ports and the phase imbalance (PI) is the phase difference between the phase response of the output ports signals. It can be seen that the excellent matching response at all the ports is better than −27 dB at both the design frequencies. Furthermore, the matching at the input port and the isolation between the output ports are also very good and better than −25 dB at both the design frequencies with a slight frequency shift due to the soldering and fabrication losses.The phase difference is also measured to be in good agreement with a tolerance of ±0.5 dB for the operational bandwidth of the PD. The respective measured overall FBW

TABLE 3. Qualitative Comparison With State-of-The-Art Impedance Transforming Power Dividers [R: Resistor, FBW: Fractional Bandwidth, $^{\$}$Calculated/estimated From Provided Data]

Refs	No. of bands	Impedance Transformation	Isolation Network	Operating Frequencies (GHz)	S_{11} (dB) at f_1, f_2	S_{21} (dB) at f_1, f_2	S_{31} (dB) at f_1, f_2	FBW (%) at f_1, f_2	Size (λ_g^2)
[36]	single	-	reactive	1.5	-26$^{\$}$	-3.27	-3.28	26.8$^{\#}$	0.023
[9]	single	real	resistor	1	-31	-3.28	-3.42	8	0.088
[39]	single	complex	resistive (1R only)	2.0	-29	-3.77	-3.38	36	0.35
[24]	single	complex	reactive	2	-17.5	-3.25	-3.25$^{\$}$	16.8	0.25$^{\$}$
[37]	dual	-	reactive	1, 3.5	-20.0, -20.3	-3.28, -3.35	-3.25, -3.37	50$^{\#}$, 15$^{\#}$	0.023
[40]	dual	real	resistive (1R only)	1, 6.4	<-30	-3.45, -4.37	-3.45, -4.37	53, 7.3	0.087$^{\$}$
[22]	dual	real	resistive	1, 5	-29, -21	-3.6, -3.9	-3.4, -4.1	11, 12	0.175
[38]	dual	-	resistive	0.7, 2.6	<-15	3.45, 3.45$^{\$}$	3.45, 3.45$^{\$}$	24.3, 8.1	0.34
[This Work]	dual	real, complex and FDCL	resistive (1R only)	1, 2.6	-31.8, -27.9	-3.2, -3.6	-3.2, -3.6	16 and 13.1	0.106



(a) All ports matching and isolation between output ports



(b) The insertion loss and phase difference

FIGURE 9. Comparison of the measured and simulated results for proposed DBITPD.

for the proposed DBITPD are 16% at 1 GHz (0.91 GHz-1.07 GHz) and 13.1% at 2.6 GHz (2.49 GHz-2.84 GHz). It is pertinent to note that these bandwidth specifications are appropriate for a wide range of applications in antenna feeding networks, amplifiers, wireless receivers, etc., in modern wireless/industrial electronics working at IEEE wireless communication standards such as 802.11a/b/j/p/y/g/n/ac/ax, 802.16a (Superseded), P802.16.2a, Wireless Body Area Network, and FR-1 bands of 5 G applications [32]–[34].

In addition, the proposed ITPD is compared in terms of number of bands, possible impedance transformations, isolation network, the fractional bandwidth and the sizes with the recently reported PDs in Table 3. These recently published PDs are either limited with single-band operation or with the FDCL port impedances, if operates at two arbitrary frequencies. A report [23] recommends complex isolation network for the complex port impedances, however, the proposed PD doesn't use any reactive element in the isolation circuit, whether for real, complex, or FDCL port impedances. Though handling real, complex, and FDCL port imepdances at two arbitrary frequencies, the performance of the proposed ITPD compares favorably with the state-of-the-art single- and dual-band PDs. The size of the fabricated prototype, integrated with the impedance transformers at the ports, are on the lower side. It is also found that the proposed ITPD has superior amplitude and phase imbalance performance over mostly published state-of-the-art designs such as [22], [36], [38], [39]. Clearly, the achievable r and k with the proposed ITPD is highest among the earlier published ITPDs.

VI. CONCLUSION

An impedance transforming dual-band equal PD has been proposed in this paper. The proposed design utilizes the well known T-Type structure to achieve real, complex, and FDCL impedance transformations at the two arbitrary frequencies. The proposed design approach not only uses a simplified architecture but provides the enhanced design flexibility also. The closed-form design equations and the systematic design flow aid in quick prototyping of the DBITPD. For experimental verification, a design example has also been fabricated on RO5880 substrate to demonstrate the performance. The agreement between the simulation and measurement results has demonstrated the effectiveness of the proposed circuit.

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