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Comparison of Isolated Bidirectional DC/DC Converters Using WBG Devices for More Electric Aircraft

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ABSTRACT With the aim towards lighter and more efficient electrical systems in future aircraft, design of DC/DC converters with high efficiency, power density and improved thermal management becomes necessary. This paper investigates the detailed design of isolated bidirectional DC/DC converters for more electric aircraft (MEA). Use of wide bandgap (WBG) devices to enhance system efficiency is considered. A transformer optimization technique based on switching frequency for different converter topologies is investigated. The control strategy of the discussed configurations are verified in the PLECS simulation environment. Dual active bridge (DAB), input-series output-parallel (ISOP), neutral point clamped (NPC) and active neutral point clamped (ANPC) converters are considered to exploit benefits offered by WBG devices for MEA. A comparison is performed in terms of efficiency, thermal management, power density and electromagnetic interference (EMI). The results indicate that the ANPC converter is better for efficiency, thermal management and power density. The DAB converter showed similar results to the ISOP with the DAB yielding higher efficiency. The NPC and ANPC configurations resulted in the best EMI performance. The NPC converter proved to be the least effective solution with regard to efficiency, thermal management and power density.

INDEX TERMS DC/DC converter, more electric aircraft, MOSFET, multilevel converter, thermal management.

I. INTRODUCTION

As the trend of electrified transportation, as a means to mitigate carbon dioxide (CO_2) emissions, spreads outside the automotive sector, the concept of more electric aircraft (MEA) is gaining traction. In recent years, the design of aircraft has changed with the substitution of traditional hydraulic or pneumatic actuators with electrical systems. Removal of such systems results in improvements to fuel efficiency. However, electrical systems in the aircraft may be associated with large weight and volume. Power electronics enable the design of more compact and lighter electrical systems in aircraft design [1].

The system architecture of the high voltage direct current (HVDC) network for the MEA is shown in Fig. 1. The generators supply 115 Vac or 230 Vac to the AC/DC rectifier units. The AC voltage is then converted to DC link voltages of +/− 135 V and +/− 270 V, respectively. Solid State Power Controller (SSPC) connects the load to the DC bus. With the need for reduced weight, size and energy loss in electrical systems along with increased power levels, new electric network in aircraft require a standard 350 Vdc and 540 Vdc (+/− 270 Vdc), also known as the HVDC voltage. From the high voltage (HV) bus, the 28 Vdc bus, also referred to as the low voltage direct current (LVDC) network is generated. Most of the electric loads used in MEA are designed for a nominal voltage of 28 V [2]. An example of such load is the onboard control units. The conversion from the +/− 270 Vdc bus to 28 V occurs through a DC/DC converter. These converters have transformers, providing galvanic isolation between the high voltage and low voltage buses.

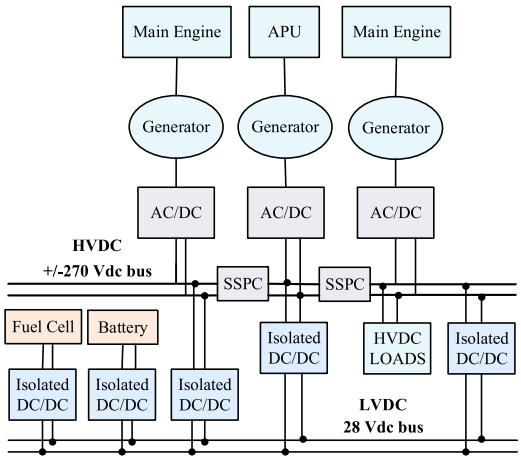

FIGURE 1. HVDC architecture of MEA.

In the future, electrical systems in aircraft are expected to achieve higher power density, with the help of power electronics technology. However, aerospace applications pose challenges for power electronics in terms of weight, volume, cost and reliability of power converters [1]. Improvement of power density stems from the weight and size of the transformer and heatsinks required for thermal management. Converters with higher efficiency dissipate lower losses and thus, relieve thermal requirements. Therefore, to design a DC/DC converter for MEA applications, efficiency, volume and weight, fault-tolerant capability and reliability along with cost must be considered [3]. The power density, thermal management and efficiency depend to a great extent on the topology selected. The dual active bridge (DAB) converter has shown good performance in terms of power density, efficiency and wide gain range with simple control [4], [5]. Development of a bidirectional DC/DC converter for future avionic applications where a DC bus of 270 V is interfaced with a 28 V bus, is proposed in [6]. A conventional 1.2 kW DAB converter with two full bridges is compared to a DAB topology with centre-tapped transformer at the secondary side in terms of efficiency, power density and transformer design. Only the weight and volume of the transformer, inductor and capacitor are considered. In [7] a current-fed isolated DC/DC converter is compared with the DAB for interconnection of the 270 V DC network with the 28 V network. Results are presented considering efficiency, weight and volume analysis without heatsink consideration. A comprehensive analysis of a 1 kW bidirectional isolated DC/DC converter for electric vehicle (EV) charging systems in automotive applications is conducted in [5]. Half-bridge and full-bridge DAB and CLLC configurations are compared with regard to efficiency, cost and power density. The weight and volume were based on the number of switches, capacitors and inductors in the converter.

The majority of the work investigating isolated DC/DC converters in the literature do not consider thermal management as part of the comparison analysis, with consideration of efficiency and power density. Considering the cooling system in the power density analysis is beneficial in selecting the right topology for different applications, since in most cases, these components form majority of the weight of the converter alongside the transformer. A transformer optimization technique is also useful to obtain the optimal design considering different core materials. With increased power levels and concern for lighter electrical systems and improved thermal management, future aircraft are expected to use wide bandgap (WBG) devices such as SiC and GaN. Most comparison analysis in literature for MEA, is done with either Si or SiC devices. Comparison of different converters using GaN devices will be helpful to determine the cost and efficiency tradeoffs associated with these switches. Also, the comparative analysis found in the literature was performed mainly for the 270 V bus. DC/DC converters at higher voltage levels need to be designed with the standard 540 HVDC voltage in aircraft. The DC/DC converter will operate with a wider range, therefore a high voltage operating range of 480 V to 650 V is considered. The 28 V DC bus voltage can fluctuate from the charging and discharging of the battery connected to it. The low voltage range is from 22 V to 29 V. The nominal high voltage, and low voltage buses are considered to be at 600 V and 28 V, respectively. Design of a 5 kW converter will be investigated for this application.

In power electronics, operating at higher switching frequencies is associated with improved power density since the size of the magnetics decreases. However, at higher switching frequencies, the switching losses of the semiconductor devices increases, resulting in larger heatsinks needed to dissipate the higher losses. Therefore, a tradeoff exists between the power density and thermal solution. Considering these factors, a switching frequency of 100 kHz has been chosen for this application. High frequency applications are prone to radiated and conducted emissions, resulting in electromagnetic interference (EMI) which can lead to incorrect operation of the electrical devices [8]. This is particularly important with fast switching semiconductors such as WBG devices. WBG devices such as Silicon Carbide (SiC) and Gallium Nitride (GaN) have shown improvements in the design of highly efficient and compact power converters [9]. With high voltage levels in MEA applications and the limited voltage rating of GaN (650 V) Metal Oxide Silicon Field Effect Transistors (MOSFETs), use of GaN devices can be restricted based on the selected topology. A configuration that will split the high voltage DC bus, such as an input-series output-parallel or multilevel structure is required to exploit the benefits offered by GaN devices. Due to the higher voltage rating of SiC devices (1200 V), two-level topologies such as the DAB can take advantage of these MOSFETs without the need for modifying the configuration. A detailed comparison of two-level (DAB and input-series output-parallel (ISOP)) and multilevel (neutral point clamped (NPC) and active neutral point clamped (ANPC)) isolated bidirectional DC/DC converters, based on the DAB, employing WBG technology for MEA are investigated in this paper.

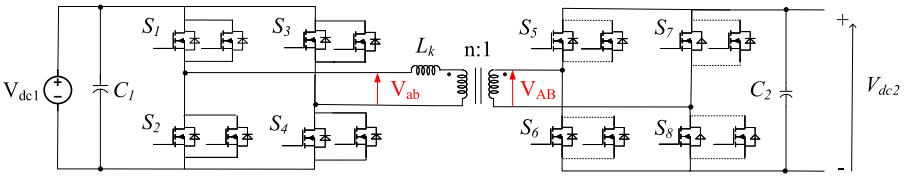

FIGURE 2. Dual Active Bridge (DAB) converter.

The rest of the paper is presented as follows. Section II includes the design and modulation technique of two-level and multilevel DC/DC converters. Design parameter selection considering soft-switching is outlined. Transformer design and optimization for the considered converters is discussed in Section III. In Section IV, control of the two-level and multilevel configurations is investigated. A nested-loop control strategy based on input current and output voltage sensing is proposed. Effectiveness of the controllers when subject to disturbance, are presented. Section V includes simulation results verifying circuit operation and validating the design. Comparison of the topologies in terms of efficiency, thermal management, power density, and EMI is provided. Finally, the topology that outperforms based on the considered design criteria is presented.

II. ISOLATED BIDIRECTIONAL TOPOLOGIES

A. TWO-LEVEL TOPOLOGIES

1) DUAL ACTIVE BRIDGE

The areas that are mainly investigated to increase the efficiency and power density of DC/DC converters are the converter topology, switching device technology and optimization of the magnetic components. The selection process for the switching devices and operating frequency is related to the selected topology. Some topologies offer lower switching device losses permitting the increase of switching frequency and reduction of the magnetics size as well as the heatsink size. One solution to reduce the switching device losses is to eliminate the overlap transition period between the switching intervals. This process is known as soft switching where the voltage across the device goes to zero before it turns on, known as zero-voltage switching (ZVS), or having the current going to zero before turning the device off, known as zero-current switching (ZCS). Fig. 3(a) shows the device waveforms when being hard switched. When the device turns on, the device voltage V_d decreases while the current I_d increases creating an overlap area causing the turn-on switching losses. The same operation applies while the device is being turned off causing the turn-off switching losses. Fig. 3(b) shows the switching waveforms under ZVS and ZCS operation. The DAB converter, introduced in [4], is one of the most utilized topologies to achieve ZVS. The leakage inductor is added between the HV side and transformer to aid power flow. The most utilized control strategy for the DAB is based on phase-shift modulation where the gating signals of the primary and secondary bridges are phase shifted with respect to each other, controlling the power flow in either direction.

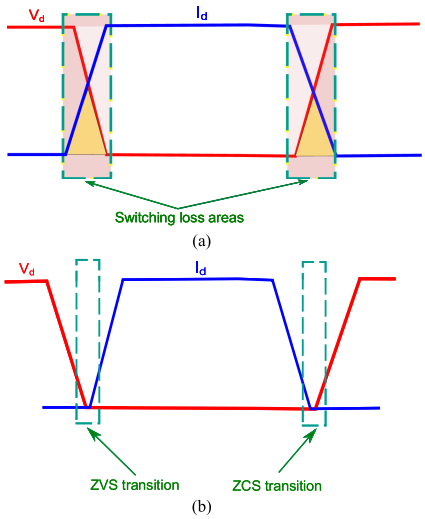

FIGURE 3. (a) Hard switching and (b) soft switching.

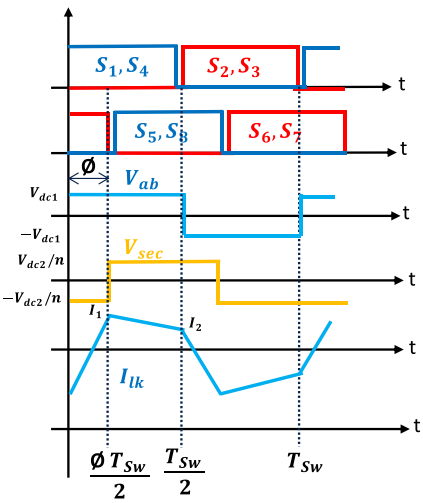

FIGURE 4. Modulation technique and switching waveforms of DAB.

The added inductor along with phase shifting the two bridges causes current to still flow when the devices are turned off. The flow of current leads to charging and discharging of the output capacitances of the power devices, flowing through the device body diode during the deadtime which causes the devices to turn on while the diode is conducting allowing for ZVS. Thus, turn-on losses of the devices are eliminated. The DAB topology is illustrated in Fig. 2. The DAB modulation and switching waveforms are shown in Fig. 4.

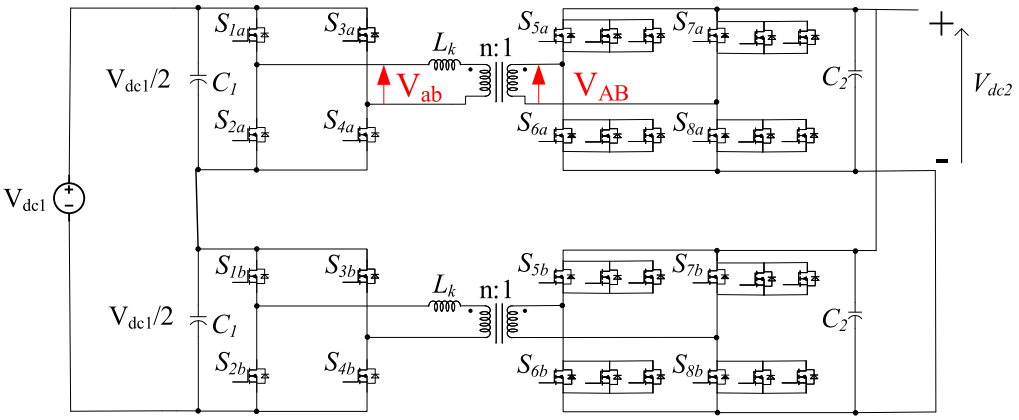

FIGURE 5. Input-series output-parallel (ISOP) DAB converter.

To achieve ZVS, the leakage inductance as well as the phase shift (ϕ) need to be selected across the required operating range of the input and output voltage. The conditions to achieve ZVS require both I_1 and I_2 larger than zero to flow through the diodes during the deadtime. Expressions for both I_1 and I_2 have been derived in [10], applying the ZVS condition, the following boundaries for achieving ZVS can be derived to get the following conditions [10]. Condition for lagging bridge:

$$\phi > \frac{1-M}{2}. \tag{1}$$

Condition for leading bridge:

$$\phi > \frac{M-1}{2M}, \tag{2}$$

where M is defined as $\frac{nV_{dc2}}{V_{dc1}}$. The ZVS zone can be further limited depending on the converter operating range through defining a minimum ($M_{\min}$) and maximum ($M_{\max}$) required gain, based on the input voltage range.

2) INPUT-SERIES OUTPUT-PARALLEL

With the limitations of silicon (Si) devices due to its inherent properties, use of WBG devices has gained attention in recent years. In power electronics, specifically DC/DC converters, SiC and GaN WBG devices have shown benefits in electrified transportation applications [9]. For higher voltage DC/DC converters, SiC would be a better choice due to the limited voltage range of GaN devices (650 V). However, GaN-based converters typically obtain higher efficiency, power density and operating frequency [11]–[13]. A 600 V to 28 V DAB DC/DC converter restricts the use of GaN on the primary side. The voltage rating of the MOSFETs on the primary bridge need to be higher than 650 V to account for the voltage peaks of the switches when in operation. Therefore, to use GaN devices, the topology needs to be slightly modified, splitting the input voltage and enabling the use of 650 V rated GaN MOSFETs. One such configuration is the ISOP connected converter shown in Fig. 5. This topology can withstand higher input voltage and provide higher output power, lower cost and better performance [14]. However, the ISOP connection of the DAB converter is associated with control complexity as the connection of multiple modules does not necessarily ensure equal power, voltage and current distribution. This is especially useful in high power applications where the aim is to increase the voltage rating and current handling capability. In these applications, paralleling of multiple modules is common, also referred to as modularization. Modularization of power converters provides performance enhancement and less costly manufacturing. Despite the high input voltage of 600 V, series connection of two DAB converters at the input will split that voltage to 300 V enabling the use of 650 V rated GaN devices. With ISOP connection, the weight and size of the converter along with the magnetic components are improved [15], [16]. This in turn can enhance the converter performance.

The switching modulation of the ISOP DAB configuration is similar to the DAB. Each bridge is operating at 50 % duty cycle with the phase shift between the primary and secondary bridges acting as the control variable. The sign of this variable determines the power flow in both, buck and boost, directions. The magnitude of the phase shift determines the amount of power flow. The output side of the modules are connected in parallel and therefore have equal voltages. The input current is also the same for both modules. It is important to keep the input current-output voltage ratio the same for all modules to prevent one of the input capacitors from discharging while the other is charging. This ratio depends on circuit parameters such as the transformer turns ratio, external leakage inductance, phase shift (ϕ) and switching frequency. Thus, one module supports the entire input voltage range while the other module has zero voltage. Obtaining uniform distribution of input voltage among the two modules is essential for design of compact modules as well as for ZVS. In ZVS, the turn-on losses are essentially zero leading to a more efficient operating condition for the converter, under soft switching conditions. However, practically, in open loop operation of the ISOP-DAB converter, the input voltage is evenly distributed in all

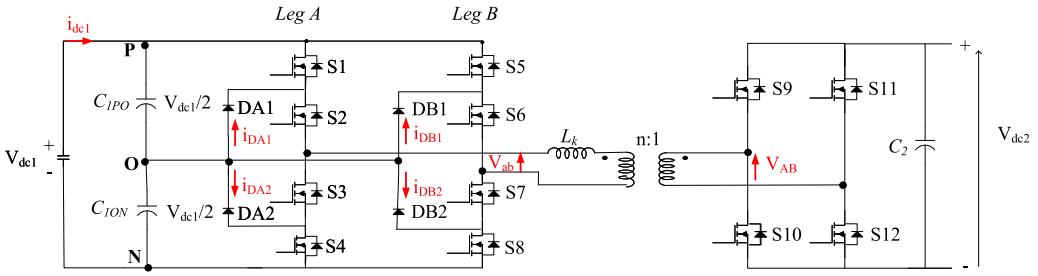

FIGURE 6. Neutral-point-clamped dual active bridge (NPC-DAB) converter.

modules. The distribution of input voltage depends on the differences in the design of the two modules and can be negligible if component tolerances are low, and circuit parasitics are minimized. Since the aim of this paper is to conduct a comparison among different topologies in terms of efficiency, power density and thermal management, the control of the ISOP configuration is based off of the DAB via input current and output voltage control. Design parameters such as the leakage inductance and input/output capacitors are derived in the same manner as the DAB. The turns ratio in this topology is half of that of the DAB since the input voltage is split in half, at 300 V.

B. MULTILEVEL TOPOLOGIES

Multilevel converters have been very popular in low to medium voltage (MV) applications due to their higher DC-voltage ratings. Thus enabling use of lower-voltage rated devices which reduce conduction and switching losses of semiconductors, and reduce the total harmonic distortion (THD) of the current and voltage waveforms while enhancing fault-tolerance capability [17]. These multilevel converters can also result in lower dv/dt with smaller filter sizes [18]. The most common multilevel topologies are the cascaded H-bridge (CHB), NPC, and flying capacitor (FC) converters. FC and NPC topologies permit use of devices with lower voltage rating compared to CHB. In FC, the power rating of the flying capacitors need to be three times higher than that of the NPC configuration. Since voltage balancing of the capacitors in the NPC topology become more complicated as the levels increase, only three-level NPC topologies have become popular in MV industrial applications.

The NPC-DAB converter topology is shown in Fig. 6. The capacitors used to split the DC-link voltage should ideally be at the same voltage. This can be achieved by using ideal DC sources. Factors such as aging, non-ideal circuit operation, and parasitic effects of the circuit can cause a voltage imbalance across these capacitors. Voltage imbalance may lead to loss of a voltage level at the multilevel output, possibly damaging the associated switches or diodes in the converter. The 3-level (3-L) NPC diodes connect the neutral point to the converter phase output, forming three-levels in the topology. Two three-level NPC legs are connected to form five-levels. This five-level configuration allows the devices used on the HV side of the DAB to block part of the DC voltage V_{dc1}. The

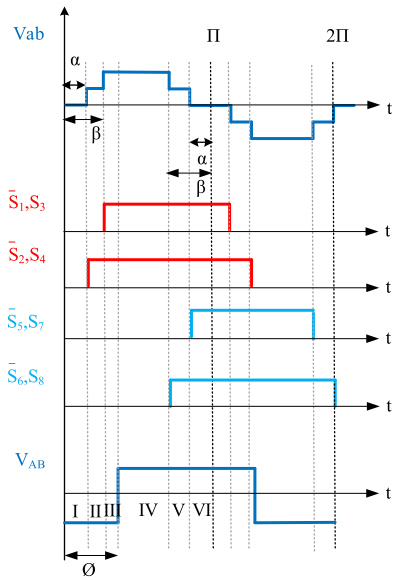

FIGURE 7. Modulation technique and switching waveforms of NPC.

3-L NPC legs provide three voltages of ($V_{dc1}/2$, 0, $-V_{dc1}/2$). The two legs (A and B) form five levels (V_{dc1}, $V_{dc1}/2$, 0, $-V_{dc1}/2$, $-V_{dc1}$).

1) NEUTRAL-POINT-CLAMPED DUAL ACTIVE BRIDGE

The modulation technique is based on either space vector modulation (SVM) or carrier based pulse-width modulation (PWM). For simplicity, the PWM method has been employed in this paper. The switching waveforms of this converter are shown in Fig. 7. The modulation is considered from regions I to VI (0 to π) with symmetric modulation from π to 2π. No devices in series are used in the NPC bridge, thereby eliminating dynamic and static voltage sharing problems. The gating signal of leg B switches are lagging by 90○ phase shift from leg A. The DAB bridge is operating at 50% duty cycle using the phase shift (ϕ) modulation technique used for the DAB in Section II-A1. The 5-level primary bridge is phase shifted from the two-level secondary bridge by this parameter. The sign of ϕ determines the power flow direction, enabling operation in buck and boost modes. When ϕ is positive (primary bridge leads secondary bridge) power flows from primary to secondary. Reverse power flow is obtained when ϕ is negative

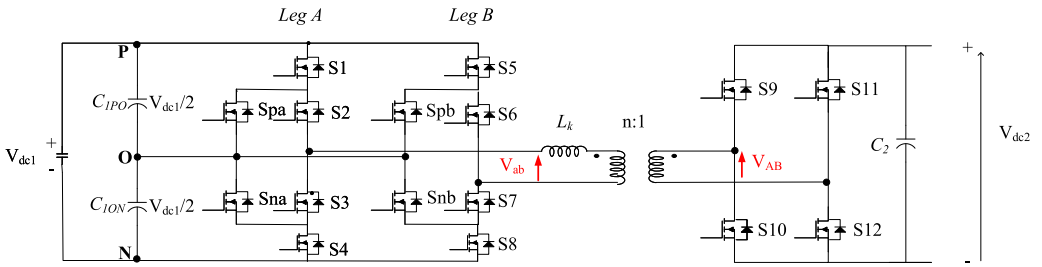

FIGURE 8. Active neutral-point clamped dual active bridge (ANPC-DAB) converter.

(the primary bridge lags secondary bridge), enabling power flow from secondary to primary bridge. Two parameters, α and β are defined to produce the five-level voltage waveform, V_{ab}. As seen from Fig. 7, the primary voltage is symmetric around $\phi = \pi/2$. Thus, α and β are used to determine the switching modulation of the four MOSFETs in each leg of the NPC. According to [19], the output power flow equation can be obtained for three cases based on ϕ. In this paper considering the values of the control variables, the output power equation is given in (3), where $\beta < \phi \leqslant \frac{\pi}{2}$:

$$P_o = \frac{V_{dc1}V_{dc2}}{n\omega L}\left(\phi - \frac{\phi^2}{\pi} - \frac{\alpha^2}{2\pi} - \frac{\beta^2}{2\pi}\right). \tag{3}$$

In (3), $\omega = 2\pi f_{sw}$, where f_{sw} is the switching frequency, n is the transformer turns ratio, L is the leakage inductance and d is the voltage conversion ratio defined as $d = \frac{V_{dc2}}{nV_{dc1}}$. According to [20], the DAB is most efficient when all switches are operating in ZVS. This is possible with the conversion ratio set to unity. The five-level DAB in this section can also achieve ZVS when d = 1. Therefore, the transformer turns ratio is obtained as follows

$$n = \frac{V_{dc2}}{V_{dc1}}. \tag{4}$$

The NPC phase leg has uneven distribution of losses and switching stress [21]. Based on the converter operating condition and the neutral current path, the switching stress and loss distribution can vary [18]. Therefore, the ANPC converter was proposed to improve the shortcomings of NPC.

2) ACTIVE-NEUTRAL-POINT-CLAMPED DUAL ACTIVE BRIDGE

One of the benefits of ANPC over NPC is its ability to select the current commutation loop through its two active clamp switches. These switches replace the diodes in the NPC topology as shown in Fig. 8. The diodes in the NPC topology incur high conduction losses, therefore the ANPC is found to be more efficient.

The modulation technique is similar to the NPC with the exception of the added clamping switches, Sp and Sn. The adopted modulation strategy is based on that proposed in [18], as shown in Fig. 9.

The gating sequence is also similar to the NPC with the clamping switches (Sp and Sn) operating complementary to the outer switches ($S1$ and $S4$). The inner switches ($S2$ and $S3$) operate synchronously to the clamping switches (Sn and Sp) respectively. This is demonstrated in Table 1.

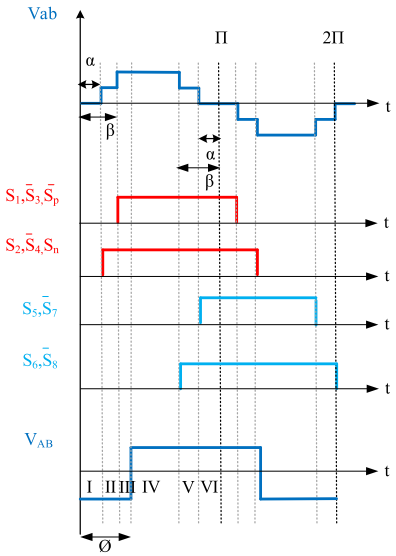

FIGURE 9. Modulation technique and switching waveforms of ANPC.

TABLE 1. Gating Sequence for ANPC Converter

State	Sp	$S1$	$S2$	$S3$	$S4$	Sn
P	0	1	1	0	0	1
O	1	0	1	1	0	1
N	1	0	0	1	1	0

The modulation scheme used in this paper was proposed by [18]. The gating signals are shown in Table 1. This technique has three states; positive (P), negative (N) and neutral (O). Switches $S1$ and $S2$ are turned on in the positive (P) state.

Switch Sn is also switched on to divide the DC-link voltage equally across $S3$ and $S4$ in the OFF-state. The negative state follows similarly. For the neutral path, there are two paths connecting the neutral point "O" to the mid-level switches Sp and Sn simultaneously. Therefore, unlike the conventional ANPC modulation method where the mid-level switches connect to the neutral point in two different states, only one neutral state is present in the utilized modulation scheme. Regardless of the output voltage switching between the positive and neutral or the negative and neutral paths, only one neutral state is used. Since both mid-level paths are used, the conduction loss can

TABLE 2. Transformer Specifications

Parameter	DAB	ISOP	NPC	ANPC
Input voltage		480 V - 650 V		
Output voltage		22 V - 29 V		
Power		5 kW		
Transformer turns ratio	22:1	11:1	22:1	22:1
Primary RMS current	12.5 A	6.25 A	11 A	9.5 A
Secondary RMS current	270 A	135 A	245 A	290 A

be significantly reduced. The switching loops in this method include one switch/diode and two diodes/switches connected in parallel versus the single switch and diode used in the commutation loop of conventional ANPC modulation.

III. TRANSFORMER DESIGN

It is necessary to have an isolation element on the aircraft electrical distribution network for both safety and electromagnetic compatibility (EMC) [2]. A high-frequency transformer is usually utilized to achieve the isolation function. With the increase in the electrical demand in MEA, more isolated DC/DC converters are utilized where the magnetics design process is crucial to attain high power density and high specific power. Utilizing WBG switching devices permits operation at higher frequencies. WBG devices have the advantage of having better switching characteristics as well as lower on-resistance and lower total gate charges over silicon devices, which decreases the conduction losses and losses in the driving circuit. However, with higher switching frequency, the transformer core losses increase and heat management problems due to the temperature rise occur. Planar technology is also one solution to reduce the volume and weight of the magnetic components while improving the thermal performance due to increased outer surface area [22]. The transformer core is selected for the four topologies based on an optimization tool that reduces transformer core and copper losses. The core is selected upon optimization of the maximum flux density at a fixed frequency. Paralleled core configurations are considered. The selection process is discussed in detail in [23]; where the maximum flux density is optimized to minimize the total transformer losses. Table 2 shows the worst-case conditions for the four topologies for which the transformer core is selected. The selection process is based on calculating a geometrical factor for each core in a database of cores and relating that factor to the converter specifications as discussed in [23].

The switching frequency is selected to be 100 kHz for the four topologies. The transformer core is selected based on the specifications shown in Table 2. The ISOP consists of two 2.5 kW converters, with two transformers. Each transformer has a single EE58 core. For the DAB, NPC and ANPC converters, the transformer in each topology has two EE58 cores in parallel. The two EE58 cores in parallel are selected as the optimum design at the 100 kHz switching frequency featuring a total weight of 238 g, and a volume of 49.2 cm^3. The transformer weight and volume is consistent for all four

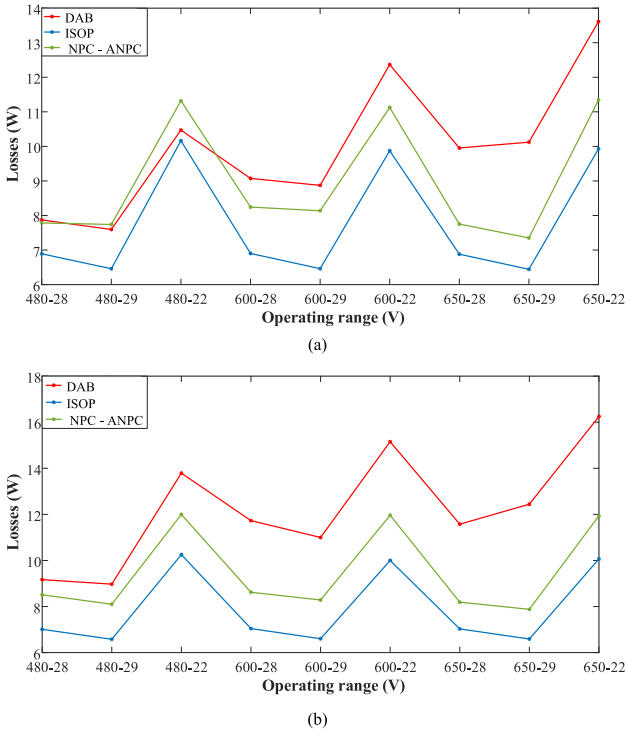

FIGURE 10. Transformer losses at various operating points in: (a) buck, and (b) boost operation.

topologies. Note that the design is based on the worst-case operating point.

The total transformer losses are then calculated and compared between the four topologies at different operating points in both power flow directions (buck and boost). The transformer losses are divided into copper and core losses and are calculated using (5) and (6), respectively.

$$P_{Copper} = \sum_{i=1}^{n} I_i^2 R_i \tag{5}$$

I_i is the winding rms current, R_i is the winding resistance which is equal to $\frac{nMLT\rho}{A_{Wire-i}}$, n is the number of turns, ρ is the copper resistivity equal to $1.724 \cdot 10^{-8}\ \Omega \cdot m$, MLT is the mean length per turn, and A_{Wire-i} is the wire cross-sectional area. The wires are sized based on the available window area and to maintain a current density of $5\ A/mm^2$. The core losses are then calculated using Steinmetz equation:

$$P_{Core} = k f^{\alpha} \beta_{\max}^{\beta} V_{core} \tag{6}$$

k, α and β are the Steinmetz coefficients provided by the core manufacturer, frequency is represented by f, $B_{\max}$ is the maximum flux density and V_{core} is the core volume. R-Material from Magnetics Inc. is selected as the core material due to its high temperature stability, high saturation limit and low core losses per unit volume. The total losses are shown in Fig. 10 for buck and boost operation, at different operating points. According to Fig. 10, the NPC and ANPC have the same transformer losses, due to the same RMS

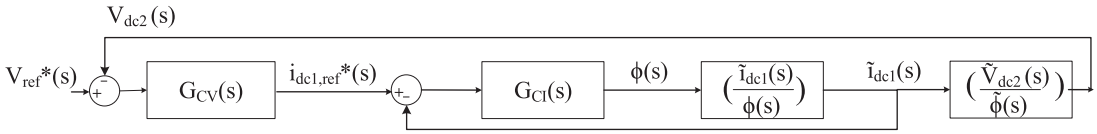

FIGURE 11. Nested loop control strategy based on an inner current loop and an outer voltage loop.

current passing through the primary and secondary windings of the transformer. From Fig. 10, it is seen that the losses among the first two operating points (480-28 and 480-29) are very close as expected for the DAB, ISOP and NPC/ANPC due to the small variation in the secondary side dc link voltage.

The same applies for the other operating points with $V_{dc2} = 28$ V and $V_{dc2} = 29$ V. The highest losses occur when $V_{dc2} = 22$ V as expected since this is the lowest secondary side dc link voltage. Among the three operating points where V_{dc1} is set to 480 V, 600 V and 650 V and $V_{dc2} = 22$ V, the last operating point ($V_{dc1} = 650$ V and $V_{dc2} = 22$ V) has the highest loss for the DAB. The other topologies (ISOP, NPC and ANPC) have similar losses at the operating points where $V_{dc2} = 22$ V. In buck and boost operation, the ISOP has essentially the same losses across the operating points when $V_{dc2} = 28$ V and $V_{dc2} = 29$ V.

IV. CONTROL

In this section, the control strategy of the topologies is discussed. Since the DAB control is similar to the ISOP and control of the NPC is similar to the ANPC, control of only one two-level and one multilevel topology is discussed.

A. NESTED CONTROL LOOP

The control of the DAB is similar to the ISOP. Therefore, only the DAB control will be discussed in this section. It is common practice to use a proportional-integral (PI) controller to control and regulate a DC/DC converter. In control design, either a lead or lag compensator could be used [24]. For the DAB, lag PI compensation is chosen based on the following generalized transfer function

$$G_c(s) = G_{c\infty}\left(1 + \frac{\omega_L}{s}\right). \tag{7}$$

The design strategy is based on choosing $G_{c\infty}$ to obtain the desired crossover frequency while selecting ω_L to be low enough to ensure adequate phase margin for system stability [24].

In terms of sensing, either the voltage, current or both are sensed in order to regulate the converter to operate within the desired power levels. The PI controller concept used for the DAB is shown in Fig. 11. As seen from Fig. 11, a nested-loop control strategy is employed. The current and voltage lag compensators are demonstrated as $G_{CI}(s)$ and $G_{CV}(s)$ in Fig. 11, respectively. This control strategy senses both the input current and the output voltage. The output voltage regulation allows for controlled operation of the converter in its nominal operating range. The input current sensing is particularly useful in modular approaches where paralleling of multiple converters is desirable. In such cases, the current being fed into each module is controlled ensuring equal current sharing among the different units. The ISOP topology can specially benefit from this due to the requirements described in Section II.

The input current (i_{dc1}) is sensed and compared to the reference current ($i_{dc1,ref}$). The reference current is obtained by the outer voltage loop. The output voltage (V_{dc2}) is sensed and compared to the reference voltage which is the desired value at which V_{dc2} should regulate to. The error between the output and reference voltage results in the reference current being used for the inner current loop. Therefore, two PI control loops are used. The transfer functions are obtained via the PLECS small signal analysis toolbox.

The general transfer function is of the form

$$G_C(s) = k_p + \frac{ki}{s}. \tag{8}$$

The inner current loop transfer function is obtained first, followed by the output voltage transfer function. The crossover frequency must be selected such that it is less than one tenth of the switching frequency. A crossover frequency of 8 kHz is chosen for the inner current loop. Here, the reference current ($i_{dc1,ref}$) is set to the desired constant value. The bode plot of the system is obtained and the controller gains (k_p and k_i) are obtained at the crossover frequency. The following transfer function for the inner current loop was obtained

$$G_{CI}(s) = \frac{0.069s + 17.44}{s}. \tag{9}$$

Similarly, the outer voltage transfer function is obtained. Since the outer voltage loop is supplying the reference current of the inner current-loop, its crossover frequency must be smaller than the current-loop crossover frequency. This is chosen as one tenth of the 8 kHz selected for the current-loop. In other words, the voltage control should supply the reference current at a slow rate to the current control. The same design strategy is followed obtaining the voltage transfer function as

$$G_{CV}(s) = \frac{0.35s + 32.53}{s}. \tag{10}$$

It is important to mention that the gains for the two transfer functions have been selected such that the controller is stable providing sufficient gain and phase margin. The effectiveness of the proposed nested control-loop is shown in Fig. 12. As seen from Fig. 12(a), the output voltage regulates at the nominal output voltage of 28 V. The output current is at 178.6 A supplying the 5 kW power rating of the converter. The system

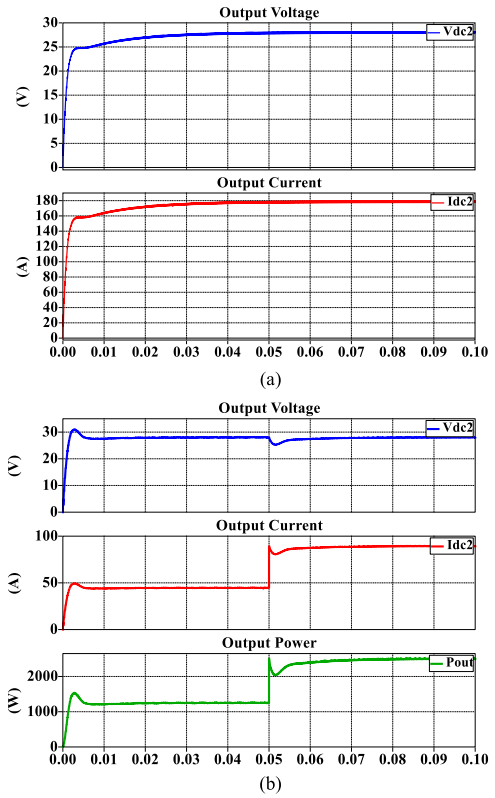

FIGURE 12. Effectiveness of the proposed nested-loop control strategy; (a) Controller output at 5 kW, and (b) Step change from 25% to 50% of full-load.

response when the load changes from 25% to 50% of full-load (5 kW) is shown in Fig. 12(b). The system is able to regulate with changes in the load, within a settling time of 24 ms.

B. CAPACITOR VOLTAGE BALANCING

There have been many voltage balancing strategies proposed in literature for NPC converters. Most methods yield a line frequency (50/60 Hz) as the output voltage. For the multi-level (ML) DAB, the switching frequency is considered the fundamental frequency. Since the voltage balancing of the NPC is similar to the ANPC, only the strategy to balance the capacitors of the NPC is discussed in this section. To control the voltage imbalance between two NPC capacitors, a neutral-point current control technique has been proposed in [17]. When the voltages are unbalanced ($V_{C1PO} \neq V_{C1ON}$), a neutral-point current i_O flows into and out of the neutral point "O" as seen in Fig. 6 resulting in

$$i_O = i_{C1PO} - i_{C1ON}, \tag{11}$$

$$i_O = i_{DA1} - i_{DA2} + i_{DB1} - i_{DB2}. \tag{12}$$

From (12), control of the neutral point current i_O requires control of the diode currents through changing the control parameters α and β. The controller accounts for the imbalance by changing the amount of current being injected into the capacitors. For instance, in the case where the voltage across

TABLE 3. Neutral-Point Current Control Strategy

Compensation	$\downarrow i_{C1PO}$	$\uparrow i_{C1ON}$
$S1$	off+$\Delta\alpha$ on+$\Delta\beta$	-
$S2$	-	off-$\Delta\beta$ on-$\Delta\alpha$
$S3$	on+$\Delta\alpha$ off+$\Delta\beta$	-
$S4$	-	on-$\Delta\beta$ off-$\Delta\alpha$
$S5$	off+$\Delta\beta$ on+$\Delta\alpha$	-
$S6$	-	off-$\Delta\alpha$ on-$\Delta\beta$
$S7$	on+$\Delta\beta$ off+$\Delta\alpha$	-
$S8$	-	on-$\Delta\alpha$ off-$\Delta\beta$

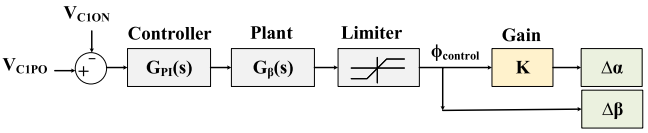

FIGURE 13. Voltage balancing control scheme.

$C_{1PO} > C_{1ON}$, i_{C1PO} should be reduced and i_{C1ON} should be increased to balance the voltage. The control variable must be subtracted/added from/to control parameters α and β, as demonstrated in Table 3. The variables $\Delta\alpha$ and $\Delta\beta$ outline the delay for turn-on and turn-off for each switch. This delay increases or decreases the current through the NPC capacitors to balance the voltages evenly.

Control variables $\Delta\alpha$ and $\Delta\beta$ are obtained from a PI controller. The voltages across the capacitors (V_{C1PO} and V_{C1ON}) are sensed. The PI controller is developed using *"pidTuner"* tool in MATLAB. The kp and ki gains are obtained resulting in the PI controller shown in (13)

$$G_{PI}(s) = K\frac{1+s\tau}{s\tau}, \tag{13}$$

where $K = kp$ and $\tau = \frac{kp}{ki}$. The plant transfer function is given as

$$G_\beta(s) = \frac{V_{dc2}}{n\omega L}\left(\frac{-|\beta|}{\pi}\right)\frac{R_{dc1}}{1+sR_{dc1}C_{PN}}. \tag{14}$$

In (14), R_{dc1} is the equivalent resistance at the NPC bridge replacing V_{dc1}, assuming V_{dc2} is the source, and C_{PN} is the equivalent input capacitance. The voltage balancing control scheme of the NPC is shown in Fig. 13.

To demonstrate the effectiveness of the controller, V_{C1PO} is set to an initial voltage of 280 V with V_{C1ON} set to 320 V. Therefore, an initial imbalance of 40 V is considered as shown in Fig. 14. From Fig. 14, it can be concluded that the voltage balancing algorithm is effective and can be used to ensure equal voltage sharing between the two capacitors.

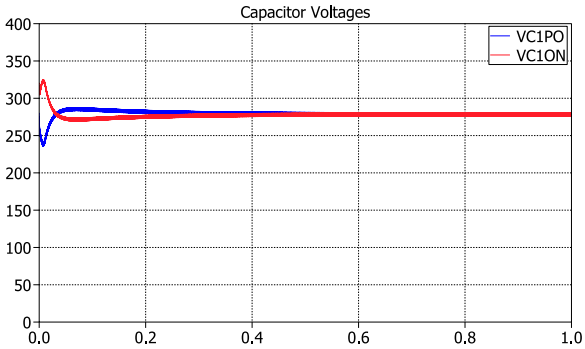

FIGURE 14. Voltage balancing of capacitors with an initial imbalance of 40 V.

TABLE 4. Simulation Parameters of Different Topologies

Topology	Description	Parameter	Value
DAB	Leakage inductance	L_k	40 μH
	Transformer turns ratio	n	22
	Input capacitor	C_1	3 uF
	Output capacitor	C_2	3 mF
ISOP	Leakage inductance	L_k	36 μH
	Transformer turns ratio	n	11
	Input capacitor	C_1	6 uF
	Output capacitor	C_2	1.5 mF
NPC & ANPC	Leakage inductance	L_k	1 μH
	Transformer turns ratio	n	22
	Input capacitor	C_{PN}	3 uF
	Output capacitor	C_2	3 mF

V. SIMULATION RESULTS AND COMPARISON

In DC/DC converters, efficiency is one of the most important factors that is taken into consideration when selecting a topology. Most converters need to be highly efficient, power dense as well as employ good thermal management. Efficiency and thermal management go hand in hand as lower dissipated losses per device result in relieved cooling and heatsink requirements. Since the topologies use WBG devices and operate at high frequencies, the converters will be compared at a high level in terms of EMI. Reliability of the power converter system is an important factor that must be considered when designing a DC/DC converter for avionic applications [3]. Stability of MEA power systems, along with protection of the MEA power grid fall under the reliability study which is outside the scope of this paper. Thus, in this section, the four discussed topologies will be compared in terms of efficiency, thermal management requirements, power density and EMI. From the detailed comparison, the topology that performs best using these four performance metrics will be outlined. The input voltage (V_{dc1}), output voltage (V_{dc2}), output power (P_{out}), and switching frequency (f_{sw}) are set to 600 V, 28 V, 5 kW and 100 kHz respectively, for all four topologies. Prior to conducting the efficiency analysis, circuit operation of the converters is simulated and validated on the PLECS Simulink Blockset environment with parameters presented in Table 4.

Simulation verification of the converters is shown in Fig. 15. As seen from Fig. 15, the DAB and ISOP primary

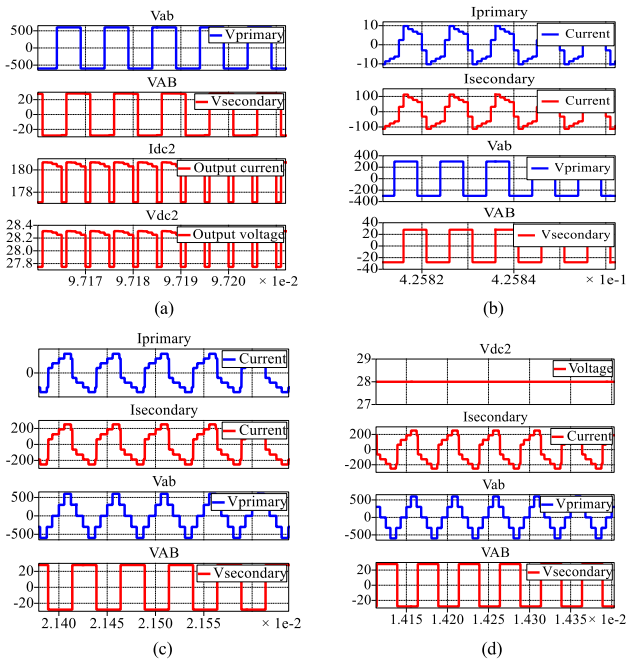

FIGURE 15. Simulation results verifying the operation of the four converters: (a) DAB, (b) ISOP, (c) NPC, and (d) ANPC.

and secondary transformer voltages are two levels whereas the primary voltage of the NPC and ANPC have five levels, as expected. The primary voltage varies from V_{dc1} to $-V_{dc1}$ in the DAB, NPC and ANPC and the secondary voltage varies from V_{dc2} to $-V_{dc2}$ in all topologies. The ISOP primary voltage varies from $V_{dc1}/2$ to $-V_{dc1}/2$ due to the configuration. The simulation was conducted at the nominal operating condition (5 kW, $V_{dc1} = 600$ V and $V_{dc2} = 28$ V).

A. EFFICIENCY ANALYSIS

Semiconductor selection for each of the four considered topologies involved a few steps. First, the voltage rating of the respective dc links was considered. In the case of the DAB, the input dc link voltage (V_{dc1}) is set to a nominal value of 600 V. At this voltage level, use of 650 V rated GaN devices is limited. One option that could be considered for this higher voltage level is series connection of two of these devices. The main concern with connecting devices in series rises from unequal dynamic voltage sharing. This is mostly due to the parasitic capacitances from gates to ground [25]. Using well-matched devices and gate drivers can result in equal voltage sharing among the connected devices. However, gate current will flow from the switch gate to the ground as a result of the dv/dt at the respective gates. The gate current flowing through the parasitic gate to ground capacitors increases as the dv/dt of the MOSFETs increases, increasing the voltage imbalance between the series switches. Many methods for voltage balancing of series connected semiconductors have been proposed in literature such as passive snubbers, master-slave switching of series semiconductors, and active voltage balancing methods [25]. Most of these methods are associated

with considerable losses and added circuitry. For simplicity purposes, higher rated semiconductors can be used. Therefore, SiC devices have been selected for the high voltage bridge of the DAB converter to exploit benefits offered by WBG devices while meeting the dc link voltage level with appropriate component derating. For the ISOP, NPC and ANPC converters, the HV dc bus is split in half due to the configuration of such converters. Therefore, use of GaN devices on the primary side is possible. For the secondary side switches in all four topologies, the low voltage bus ($V_{dc2} = 28$ V) permits the use of Si devices. Conventional Si MOSFETs cost much less than SiC and GaN devices and offer lower on-resistance at the specific secondary bus voltage level chosen for this application. Due to the aforementioned reasons, and to have a fair comparison among the considered converter configurations, Si MOSFETs were selected for the secondary bridge devices in all topologies.

To conduct the efficiency analysis, the devices must be selected first. In the DAB, two switches are connected in parallel on the HV side, per device, with six switches connected in parallel on the low-voltage (LV) side. The number of switches connected in parallel is based on meeting the current requirements of the HV and LV sides in each configuration. Rohm Semiconductor's SiC MOSFET SCT3160KLHRC11 is used on the HV side with Infineon's Si MOSFET IPP023N10N5 used on the secondary side. The LV side switch was the same for all four topologies. In the ISOP, single switches are used on the primary side with three switches connected in parallel on the secondary bridge. GaN Systems' GS66516 T GaN MOSFET was chosen for primary switches. In the NPC converter, single GaN Systems switches are used on the HV side (GS66504B) with STMicroelectronics diodes STTH12R06. ANPC HV switches are also GS66504B, with clamping switches chosen from GaN Systems' GS66506 T GaN MOSFETs. ISOP and DAB have a total of 8 switches on the primary bridge with 24 on the secondary. NPC and ANPC have 8 switches on the primary bridge with 12 on the secondary. NPC and ANPC also contain 4 diodes and 4 clamping switches on the primary bridge, respectively. NPC and ANPC converters have three switches connected in parallel on the LV side, to meet the current requirements, with single switches on the primary bridge.

To obtain the efficiency of the converters, the topologies are simulated using the PLECS thermal library. The losses are captured in terms of conduction and switching losses and obtained from (15) as shown below [26].

$$P_{loss} = I_{rms}^2 R_{dson} + \frac{V_s i_s f_{sw} Q_g}{i_g} \tag{15}$$

Equation (15) includes the conduction losses shown by the first term, and the switching losses for a MOSFET represented by the second term. The switching frequency is referred to as f_{sw}, with Q_g and i_g representing the gate charge and gate current respectively, the switching voltage and current are represented by V_s and i_s respectively, and R_{dson} is the on-resistance of the MOSFET. Here, I_{rms} corresponds to the RMS current going through the device.

TABLE 5. Operating Points Selected for Comparison

Operating Point	Voltage Range
OP1	V_{dc1}= 480 V , V_{dc2}= 22 V
OP2	V_{dc1}= 480 V , V_{dc2}= 28 V
OP3	V_{dc1}= 480 V , V_{dc2}= 29 V
OP4	V_{dc1}= 600 V , V_{dc2}= 22 V
OP5	V_{dc1}= 600 V , V_{dc2}= 28 V
OP6	V_{dc1}= 600 V , V_{dc2}= 29 V
OP7	V_{dc1}= 650 V , V_{dc2}= 22 V
OP8	V_{dc1}= 650 V , V_{dc2}= 28 V
OP9	V_{dc1}= 650 V , V_{dc2}= 29 V

Therefore, semiconductor and transformer losses are considered in this section. The transformer losses are obtained from Fig. 10. Semiconductor (switching and conduction) losses are modeled via the PLECS thermal library. Passive (capacitor and inductor) losses are neglected in the efficiency analysis as the contribution of these components to the total loss is negligible compared to the switching devices and transformer losses. Various operating points are considered with V_{dc1} varying from 650 V, 600 V and 480 V and V_{dc2} changing from 29 V, 28 V and 22 V, as shown in Table 5. The operating points were selected based on the voltage range for the high voltage and low voltage DC bus of the aircraft.

The efficiency analysis of the four converters, in buck and boost mode, are shown in Fig. 16. Since the four topologies were designed in buck operation, efficiency in buck mode will be compared for the four converters. Fig. 17 shows the efficiency comparison of the converters at various operating points. As seen from Fig. 17, the NPC and ISOP converters obtain the lowest efficiency at all operating points. The peak efficiency for DAB, ISOP, NPC and ANPC is 96.54%, 94.6%, 94.52% and 97%, respectively. Therefore, it can be concluded that ANPC obtains the highest efficiency among the four topologies, followed by the DAB. ISOP has a peak efficiency slightly higher than the NPC. It is worth mentioning that the efficiency analysis conducted here is at full-load, with nominal power of 5 kW.

Since the above analysis was conducted at full-load, to make a fair comparison, the efficiency profiles at differing power levels must be considered. The efficiency versus output power characteristics are shown for buck operation in Fig. 18. As expected at light load, converters operate at lower efficiency. Among the four topologies, the ISOP results in the lowest efficiency. One justification for higher losses with ISOP are the two transformers used in the topology that incur higher losses compared to the single transformer in the DAB. Another reason for higher losses with ISOP is attributed to the higher current on the primary side since the current is doubled compared to the DAB due to the 300 V input voltage. Therefore, the current flowing through the 5 kW DAB converter ($V_{dc1} = 600$ V, $I_{dc1} = 8.3$ A) is equal to the current flowing

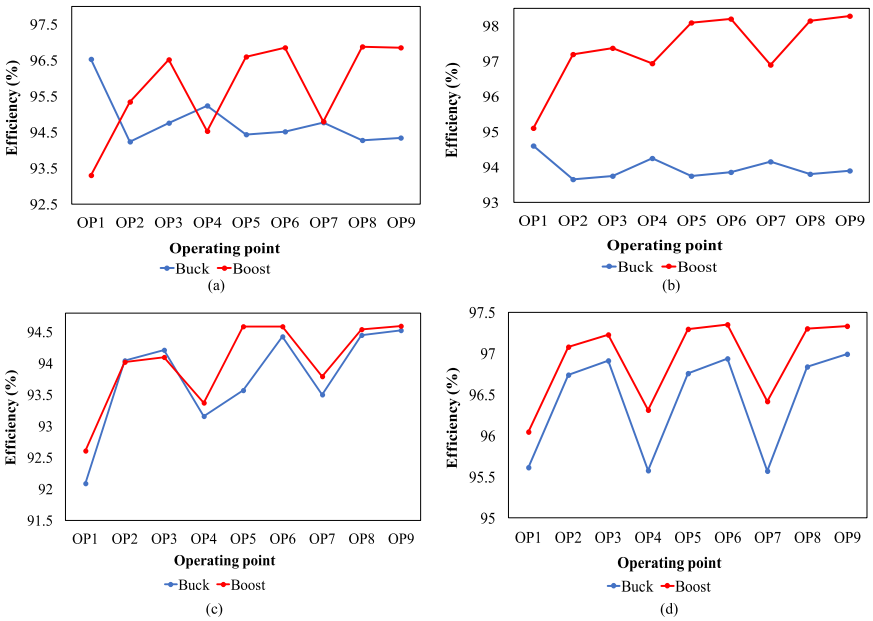

FIGURE 16. Efficiency analysis of (a) DAB, (b) ISOP, (c) NPC, and (d) ANPC for bidirectional operation at various operating points.

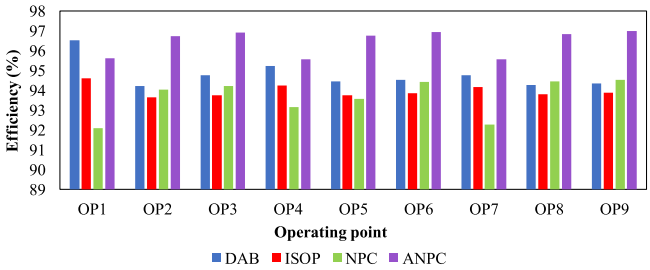

FIGURE 17. Efficiency comparison of converters in step-down operation.

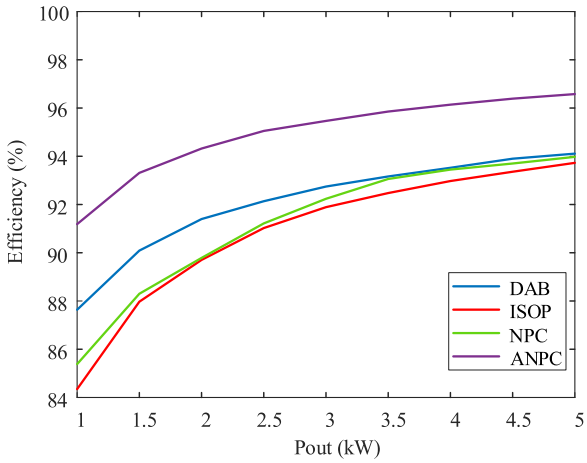

FIGURE 18. Efficiency comparison at different power levels.

through one 2.5 kW module ($V_{dc1} = 300$ V, $I_{dc1} = 8.3$ A) of the ISOP. Hence, the 5 kW ISOP sees higher current than the 5 kW DAB. This higher current results in higher conduction loss for the ISOP, explaining its lower efficiency. Between the NPC and ANPC, the NPC has lower efficiency due to the high conduction losses of the diodes in its primary bridge. The ANPC uses switches instead of diodes, hence resulting in a higher efficiency. Not only does the ANPC result in the highest peak efficiency but it also obtains the highest efficiency at varying power levels. Thus, from an efficiency perspective, ANPC seems to be the better choice among the considered topologies.

B. THERMAL MANAGEMENT ANALYSIS

The thermal design for each converter is necessary for maintaining the switches below their critical operating temperature. The maximum junction temperature, T_j, for all the switches is 150 °C in all the topologies studied, and the ambient condition during operation of the converter, T_a, is 70 °C. Therefore, the maximum required heatsink thermal resistance for both the primary and secondary side may be calculated with

$$R_{HS} = \frac{T_j - T_a}{NP} - \frac{\left(R_{j-c} + R_{TIM}\right)}{N}, \tag{16}$$

where N represents the number of switches, P the losses for each switch and R_{TIM} is the thermal resistance of the thermal pad. For the analysis, SARCON XR-m high thermal conductivity pad is used [27], where the equivalent thermal resistance is calculated based on the footprint of each switch.

Considering the worst-case losses in both the primary and secondary side for each converter topology at the nine operating points, a forced-air cooled heatsink is sufficient for the thermal design. The thermal resistance from the datasheet of Fischerelektronic heatsink [28] was used to determine the number of heatsinks required for each design. The required cooling system volume (heatsink and fan) for both the primary and secondary side is shown in Fig. 19. It is observed

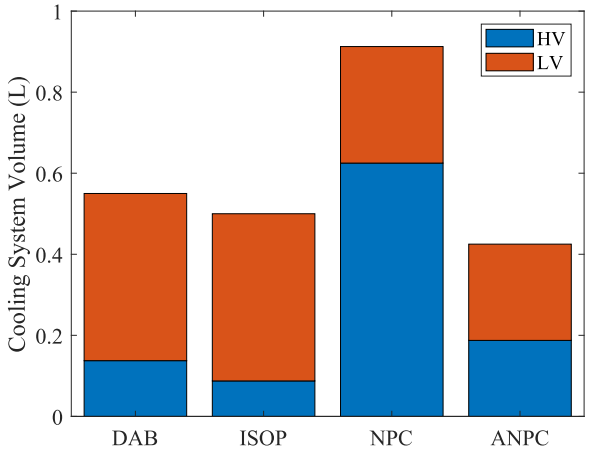

FIGURE 19. Cooling system volume for the four investigated converter topologies.

TABLE 6. Power Density Comparison

	Cooling System & Switches	
Topology	Weight [g]	Volume [cm^3]
DAB	260	550
ISOP	210	500
NPC	320	962
ANPC	188	425

that lowest volume is achieved by the ANPC topology, while the NPC requires the largest cooling system due to the high losses from the clamping diode. The DAB topology and ISOP topology achieve similar volumes due to the GaN devices on the primary side of the ISOP having the lowest losses.

C. POWER DENSITY

The transformer turns ratio is consistent for all four topologies due to the same nominal voltage operation (600 V and 28 V) as described in Section III. Based on the design, the volume of the transformer is 49.2 g/cm^3 with an estimated weight of 238 g. Therefore, the main difference stems from the weight and size of the cooling system as well as the switches for each topology. The power density results based on the switch technology and cooling system are tabulated in Table 6.

The weight consists of the heatsink, fans, and switches while the system volume includes the heatsink and fans. Since the NPC converter has the highest losses at the worst-case condition among different operating points, its cooling system will have the largest volume and weight. The power density of the ISOP is higher than the DAB since the weight of the SiC MOSFETs in the DAB are about three times higher than that of GaN in the ISOP. Considering both weight and volume, the ANPC has the highest power density among the four topologies.

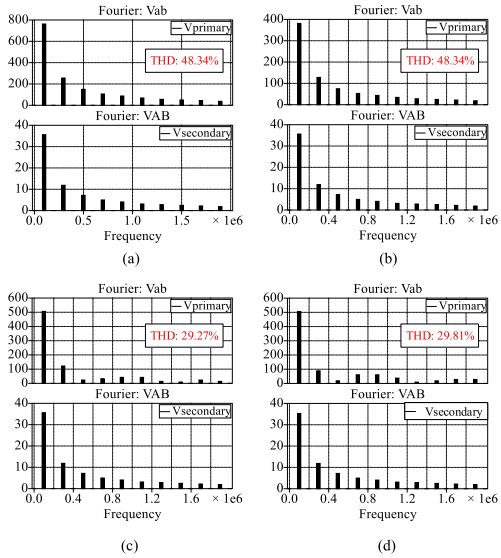

FIGURE 20. Fast Fourier Transformation (FFT) of transformer primary and secondary voltages for (a) DAB, (b) ISOP, (c) NPC and (d) ANPC.

D. ELECTROMAGNETIC INTERFERENCE (EMI)

High frequency radiated and conducted emissions from power converters can lead to unacceptable response in electrical devices. This is particularly important in high frequency applications. The transient current (di/dt) and transient voltage (dv/dt) generated during fast switching attribute to EMI. Along with the nonlinear behavior of semiconductor devices in power converters, parasitic elements and nonlinear control components also add to the conducted EMI [8]. The generated noise may result in interference with other electronic systems [29]. The use of WBG devices (SiC/GaN) is associated with high conducted and radiated EMI emissions at high frequencies due to the very fast changes in currents and voltages of these switching devices. To protect the network from such emissions while adhering to the electromagnetic compatibility (EMC) standards, an EMC filter is necessary [30].

A high-level comparison of EMI emissions among the four topologies based on the harmonic content of the transformer voltages is demonstrated in Fig. 20.

Among the four topologies, NPC and ANPC configurations are expected to have lower total harmonic distortion (THD) and generate an output current with small ripple [31]. Therefore, smaller filters can be used to improve the power quality. For this study, the transformer voltage waveforms were considered. Fast Fourier Transformation (FFT) technique is applied to convert the time-domain waveform to frequency-domain spectrum in order to better evaluate the EMI filter performance [30]. The FFT results of the transformer waveforms for the four topologies are shown in Fig. 20. From Fig. 20, it can be concluded that the secondary voltage waveforms have essentially the same FFT response for all four topologies, since the transformer secondary voltage in all converters consists of two levels, as seen from Fig. 15. Therefore, in this analysis, transformer primary voltage will be considered. It is seen that the first harmonic has the highest amplitude

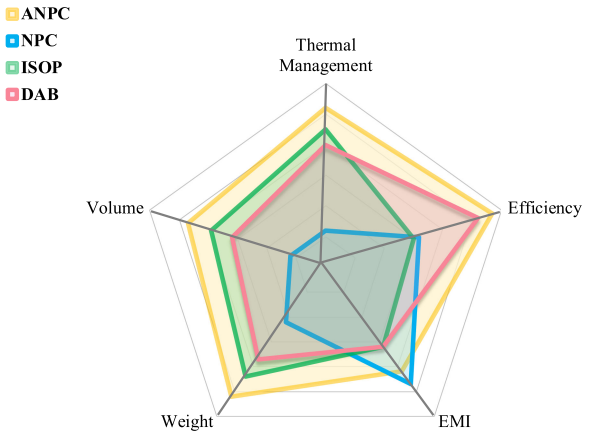

FIGURE 21. **Comparison of the four converters in terms of power density, thermal management, efficiency and EMI.**

in the DAB. The ISOP has about half the amplitude as expected since it consists of two DAB modules, with half the input voltage (300 V). The transformer primary voltage of the multilevel converter topologies (NPC and ANPC) has five levels. This means that the THD is lower for these topologies compared to the DAB, as seen from Fig. 20. The amplitude of the higher order harmonics for the primary voltage is lower for the NPC and ANPC compared to the DAB. Therefore, smaller EMI filters can be used for these topologies. Among the NPC and ANPC, higher order harmonics seem to be of similar magnitude. Therefore, for further analysis the THD of the waveforms will be considered. The primary voltage THD of the NPC and ANPC is 29.27% and 29.81% respectively, with the THD of the DAB and ISOP at 48.34%. Hence, the NPC can have the smallest EMI filter, followed closely by the ANPC. It is worth mentioning that the lower harmonics in the ISOP in Fig. 20(b) represents the harmonics for one 2.5 kW module. In terms of filter design, either two filters, one for each 2.5 kW module, can be used or one larger filter for the overall 5 kW converter resulting in essentially the same filter size as the DAB. Details regarding the design of the EMI filter are outside the scope of this paper and may be addressed in future work.

Fig. 21 shows the comparison of the presented topologies in terms of different factors. Superiority of each parameter is considered. For instance, for weight, the converter with the lowest weight (ANPC) is superior and the converter with the highest weight (NPC) is inferior. Overall, the ANPC outperforms in all aspects except the EMI, which lags closely behind the NPC. With the exception of EMI, the NPC proved to be the least effective solution for the selected specifications. The DAB and ISOP provide similar performance in terms of power density, thermal management and EMI. The efficiency obtained with the DAB however is higher than the ISOP.

From the analysis conducted in this section, it can be concluded that the ANPC outperforms the other topologies in terms of efficiency, thermal management, power density and EMI. Although use of GaN devices generally results in more efficient and power-dense converters such as the ANPC, it was shown that this is not always the case, as seen with the NPC. Therefore, the ANPC topology provides the best solution, in terms of the considered design parameters, for the MEA application.

VI. CONCLUSION

In this paper, design of a 5 kW converter with nominal voltage of 600 V and 28 V at 100 kHz for MEA was investigated. Multiple topologies were considered to provide the optimal design in terms of efficiency, thermal management, weight, volume and EMI. Transformer optimization was briefly touched on to optimize the design, considering different cores. The control and modulation strategy of the DAB, ISOP, NPC and ANPC converters were presented. Performance of the four DC/DC converters using WBG technology was analyzed. Detailed analysis was conducted for various operating points. The ANPC converter is the most effective configuration with regards to overall efficiency, thermal management, weight and volume. For the considered design parameters, the DAB lagged closely behind the ISOP in terms of power density and thermal management. The DAB had similar EMI to the ISOP with higher efficiency. The NPC had the lowest efficiency due to the diodes in its configuration, resulting in the bulkiest cooling system. As part of future work, the EMI analysis should be conducted in more depth, looking at specific filter design for each of the converters. Reliability analysis should also be investigated to choose a converter that can meet the stability requirements for MEA applications. Furthermore, the ANPC converter can be designed and built to verify the results obtained from simulation, through experimental validation.

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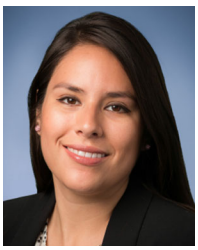

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