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A Fast Multilevel SVPWM Method Based on the Imaginary Coordinate With Direct Control of Redundant Vectors or Zero Sequence Components

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ABSTRACT This paper for the first time comprehensively presents a multilevel space vector pulse width modulation (SVPWM) method based on the imaginary coordinate system. This method is probably one of the most efficient methods in fast multilevel SVPWMs. It avoids trigonometric operation, look-up tables and only requires simple logic judgement and arithmetic calculation. A distinct advantage of this method over other coordinate-transformation-based methods is that it does not need to transform from the imaginary coordinate system back to the a-b-c (or α-β) coordinate in order to select the redundant vectors using look-up tables. The redundant vectors or zero-sequence components are directly worked out in the proposed method, e.g., for balancing dc-link capacitor voltages, which avoids identifying the starting vector, vector rotation direction (clockwise or anti-clockwise), vector sequence, etc. as used in conventional methods. This paper entails each step to implement this SVPWM method, which can be replicated for multilevel converters with any number of voltage levels. The presented method has been used and validated by various converters, including a three-level and a five-level neutral-point-clamped converter. The archive value of this paper is that it demonstrates a milestone of fast multilevel SVPWM based on coordinate transformation.

INDEX TERMS Multilevel converter, space vector pulse width modulation (SVPWM), zero-sequence component, redundant vector, imaginary coordinate, neutral point voltage balancing.

I. INTRODUCTION

Multilevel converters have been widely used in various medium-voltage, high-power conversion applications such as large motor drives, renewable (wind, solar) power generation and utility systems. They are also being increasingly used for low voltage systems to achieve higher power density by reducing output harmonics hence the filter requirements and to achieve higher efficiency by reducing switching losses due to a lower switching voltage, i.e., a portion of the whole dc-link voltage.

As is well known, there are mainly two types of modulation methods for multilevel converters, i.e., carrier-based modulation and space vector modulation (SVM). Though nowadays there is a trend to use more and more carrier-based modulation than space vector based modulation [1] due to its simpler implementation and their equivalence [2], [3], the SVM still has its own advantages. For example, the impact of voltage vectors on the dc-link capacitor voltage balancing, common-mode voltage, conduction/switching losses and output harmonics are easier to be identified with an SVM. In theory, carrier-based methods are much easier to implement than space vector based methods because no matter which method is used, the final step of the modulation is to have the comparison between the modulation signal and the carrier signal, which in fact is the definition of carrier-based modulation. If the required modulation signal, including the zero-sequence component can be directly identified, the carrier-based modulation will be the simplest and it simply becomes

a comparison between the modulation signal and the carrier signal.

To generate this required modulation signal, the space vector based modulation needs a relatively complex process such as identifying the location of the reference vector, selecting vectors to synthesize the reference, determining their sequences and duration, and selecting among the redundant vectors. On the other hand, carrier based implementation only needs to identify the required modulation signal, which is a composition of the fundamental sinusoidal signals plus a zero-sequence component, noting the selection of the zero-sequence component is equivalent to the selection between the redundant vectors in the SVM [1], [4]. However, obtaining the exact zero-sequence form to mimic the modulation wave that have been generated from the SVM is not straightforward, though efforts have been made to find optimal zero-sequence/modulation waves for carrier based modulation to achieve various objectives such as capacitor voltage balancing, reducing switching losses [4]–[6]. Therefore, space vector based modulation is still used to achieve various control objectives for various applications today.

The SVM for conventional three-level neutral point clamped (NPC) converters such as the diode NPC converter or the T-type converter is relatively simple. The process of three-level SVM can follow what has been used for the two-level SVM. However, when the number of voltage levels is four or higher, the conventional SVM process becomes very complicated as the number of vectors is cubed to the number of voltage levels, i.e., for a four-level converter, there are 64 voltage vectors and 125 for a five-level converter.

There are various ways to simplify the multilevel SVM process to achieve fast modulation. For example, one idea is to divide the multilevel space vector diagram to a number of two-level diagrams [7]–[9]. Another group of methods is to use unconventional coordinate systems such as the *g-h* coordinate (60 degree) [10], *K-L* (120 degree) coordinate [11], imaginary coordinate (line coordinate) [12]–[14], α'-β' coordinate [15] and others [16]. However, the key issue with most of these methods is that after the calculation in the new coordinate system, it has to be transferred back to the original α-β or *a-b-c* coordinate system to select the redundant vectors to determine which vector should be used and their sequence and duration, e.g., for capacitor voltage balancing purposes, which complicates the process and hinders the advantage of using the unconventional coordinate systems. A look-up table is also normally required to select the redundant vectors. [11] has reviewed and compared various SVM methods.

This paper will focus on the imaginary coordinate based SVM to show how it simplifies the calculation process and how it can directly select the redundant vectors without transferring back to the α-β or *a-b-c* coordinate. The concept of the multilevel SVM based on the imaginary coordinate system was partly introduced in [12]–[14], though the detailed implementation process and how to select between the redundant vectors are not given. As a result, this method is not well understood by the power electronics community and hence not widely adopted albeit its advantages. To the best of the authors' knowledge, this method is one of the most efficient multilevel PWM methods. The main advantages are: it has reduced and simple calculation without the need for trigonometric calculations and look-up tables; the amount of calculation does not increase with the number of voltage levels and the zero-sequence component can be directly selected. Therefore, this method can be seen as a milestone in the multilevel SVM development as a representative of the unconventional coordinate systems and should be properly archived in literature. Hence, this is the motivation of the authors to give the full details of its implementation in this paper based on the authors' extensive use of this method in various research and industrial applications.

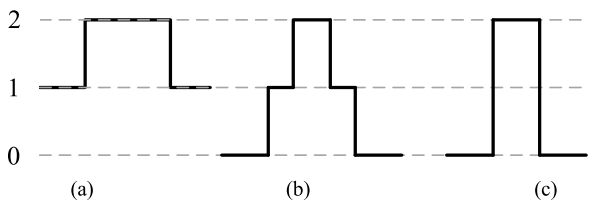


FIGURE 1. Three switching patterns in one switching period. (a) Switching twice with one-level jump. (b) Switching four times with one-level jump using three voltage levels. (c) Switching with two-level jump.

To complete the picture of multilevel PWM, there are several freedoms that can be used for the control purposes in terms of the number of voltage transitions (switching actions) in each switching period and the amplitude of voltage jump in each transition. To reduce the switching loss of the power electronics devices and voltage stress on the load, e.g., electric machines, the number of switching actions in each switching period is normally restricted to only twice (one turn-on transition and one turn-off transition) and the voltage jump (*dv/dt*) is restricted to one adjacent voltage level (one voltage level). This is illustrated in Fig. 1(a), where 0, 1, 2 represent three voltage levels. The above mentioned multilevel SVPWM methods such as the one based on the imaginary coordinate system is one of this type of PWMs. For some multilevel topologies, the switching pattern in Fig. 1(a) is not enough for certain control purposes. For example, the switching pattern in Fig. 1(a) is not sufficient to regulate the dc-link capacitor voltages for four-level or five-level NPC converters at high modulation indexes or high power factors [17]. To solve this problem, the switching pattern in Fig. 1(b) was introduced where there are four switching transitions and three voltage levels are used instead of two in each switching period. This can also be perceived as part of the middle level '1' being split into levels '2' and '0', equivalently. The corresponding modulation schemes are 'virtual vector modulation' or 'redundant level modulation' [18], [19]. Although the method in Fig. 1(b) can achieve neutral point voltage balancing, the drawback of this method is increased harmonics and increased switching losses due to more switching actions

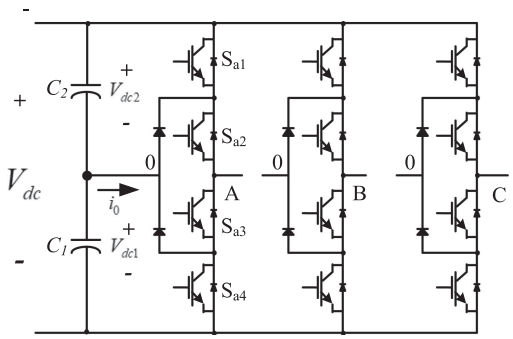


FIGURE 2. Schematic of a three-level diode NPC converter.

[20]. Thanks to the introduction of fast-speed (low switching loss) wide-bandgap (e.g., SiC, GaN) devices, the switching loss may not be a big issue where used. To further extend the control capability, another freedom can be used is to allow the voltage jump by two levels as shown in Fig. 1(c), from level '0' to '2' as an example. [21] has used this pattern to achieve voltage balancing of five-level NPC converters and the negative effects are increased voltage stress (dv/dt) and increased switching losses and harmonics. Recent work also includes the use of a combination of zero-sequence component control and redundant level modulation to best trade-off between capacitor voltage balancing capability and switching actions [22].

In the following, the detailed modulation process for the imaginary coordinate based multilevel SVPWM will be given.

II. IMAGINARY COORDINATE BASED MULTILEVEL SVPWM

Here, a three-level converter and three-level SVPWM is used as an example to describe the imaginary coordinate based SVPWM. The method can be readily extended to converters with higher number of voltage levels following the same process. Fig. 2 shows the schematic of a three-level diode NPC converter.

In Fig. 2, each phase leg can output three voltage levels, denoted by 2, 1, 0, corresponding to $+V_{dc}/2$, 0, $-V_{dc}/2$, respectively with respect to the potential of the dc-link neutral point (0). The corresponding space vector diagram in an α-β or a-b-c coordinate of the three-level converter is shown in Fig. 3. At some vertexes, there are redundant vectors, which means there are more than one vector at the vertex. For example, (2, 2, 1) and (1, 1, 0) are redundant vectors. They can achieve the same output line voltage but they can have different effect for various control purposes, e.g., balancing dc-link capacitor voltages. In Fig. 3, V_{ref} is the reference vector that needs to be synthesized using the space vectors. It is normally obtained from the current control loop of a rectifier or inverter, given in the form of V_{ra}, V_{rb}, V_{rc} in the a-b-c coordinate or V_α, V_β in the α-β coordinate. The reference vector can also be generated in an open-loop manner by giving the voltage amplitude and a rotating phase angle.

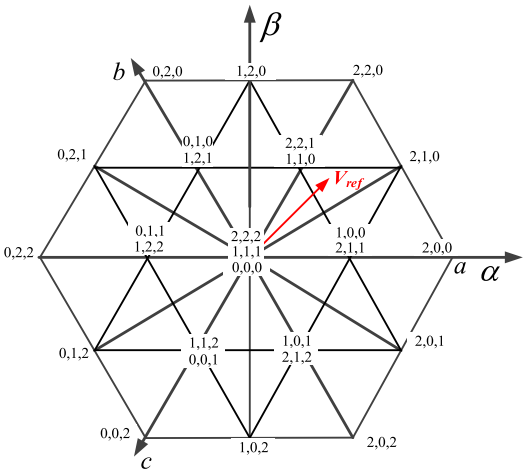


FIGURE 3. Three-level space vector diagram in an α-β or a-b-c coordinate.

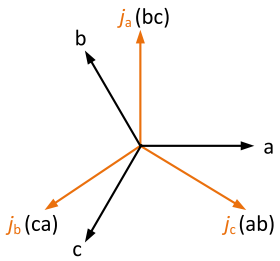


FIGURE 4. Relationship between the $j_a - j_b - j_c$ coordinate and the a-b-c coordinate.

A. COORDINATE TRANSFORMATION

The imaginary coordinate system ($j_a - j_b - j_c$) is defined as shown in Fig. 4. The reason it is named the imaginary coordinate system is because the axis j_a is perpendicular to the axis a, same for j_b to b, and j_c to c. Also, using voltage as an example, it can be seen from Fig. 4 that v_{ja} can be obtained as $v_b - v_c$ (bc), $v_{jb} = v_c - v_a$ (ca) and $v_{jc} = v_a - v_b$ (ab). Hence, any coordinate in the a-b-c plane can be transferred to the $j_a - j_b - j_c$ plane by (1).

$$\begin{pmatrix} x_{ja} \\ x_{jb} \\ x_{jc} \end{pmatrix} = \begin{pmatrix} 0 & 1 & -1 \\ -1 & 0 & 1 \\ 1 & -1 & 0 \end{pmatrix} \begin{pmatrix} x_a \\ x_b \\ x_c \end{pmatrix} \tag{1}$$

where, (x_a, x_b, x_c) are the coordinates in the a-b-c system and (x_{ja}, x_{jb}, x_{jc}) are the coordinates in the $j_a - j_b - j_c$ system. The imaginary coordinate system can also be called the line coordinate system from the definition in (1).

For completeness, as normally the reference voltage is given in the α-β coordinate (after the park transformation from the d-q coordinate), by the relationship between the α-β coordinate and the a-b-c coordinate given in (2) and with (1), the transformation from the α-β coordinate to the $j_a - j_b - j_c$

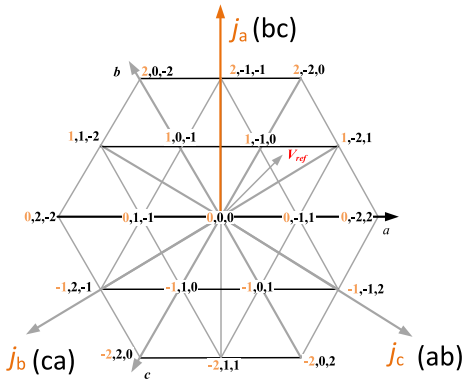


FIGURE 5. Three-level space vector diagram in the $j_a - j_b - j_c$ coordinate.

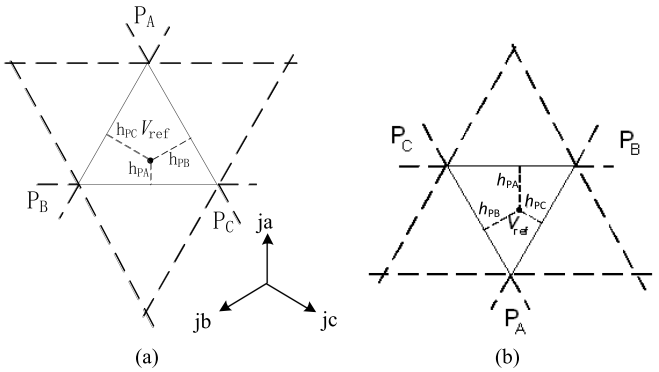


FIGURE 6. Two different types of triangles: (a) upright triangle, (b) upside-down triangle.

coordinate can be obtained as in (3).

$$\begin{pmatrix} x_a \\ x_b \\ x_c \end{pmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix} \begin{pmatrix} x_\alpha \\ x_\beta \end{pmatrix} \tag{2}$$

$$\begin{pmatrix} x_{ja} \\ x_{jb} \\ x_{jc} \end{pmatrix} = \begin{pmatrix} 0 & \sqrt{2} \\ -\sqrt{\frac{3}{2}} & -\frac{1}{\sqrt{2}} \\ \sqrt{\frac{3}{2}} & -\frac{1}{\sqrt{2}} \end{pmatrix} \begin{pmatrix} x_\alpha \\ x_\beta \end{pmatrix} \tag{3}$$

From (1), the three-level space vector diagram in the *a-b-c* coordinate shown in Fig. 1 can be transformed to the imaginary coordinate system as shown in Fig. 5. In Fig. 5, −2, −1, 0, 1, 2 correspond to the output phase-to-phase voltages of $+V_{dc}$, $+V_{dc}/2$, 0, $-V_{dc}/2$, $-V_{dc}$, respectively.

There are mainly two reasons that the imaginary coordinate is used.

1. There will be no trigonometric calculation involved in the modulation process. Only logic judgement and arithmetic calculations are needed.
2. From Fig. 5, for the lines perpendicular to the imaginary axis, each line determines the voltage level , i.e., 2, 1, 0, −1, −2, which is illustrated by dark lines and orange numbers in the figure with j_a as an example. Therefore, the location of the reference voltage can be relatively easily determined based on the integer part of the reference voltage (voltage level) and the fractional part of the reference voltage represents the duty cycle of that reference vector, which will be detailed later.

It can also be seen from Fig. 5 that there are no redundant vectors in the imaginary coordinate as it is essentially a line (*bc*, *ca*, *ab*) coordinate where the redundancy (zero-sequence) does not exist in the line (voltage), which only exists in the phase (voltage) such as in the *a-b-c* coordinate system.

B. JUDGING THE TYPE OF TRIANGLES

The reference vector will fall into one of the triangles in the space vector diagram in the imaginary coordinate as shown in Fig. 5. There two types of triangles to be distinguished in the

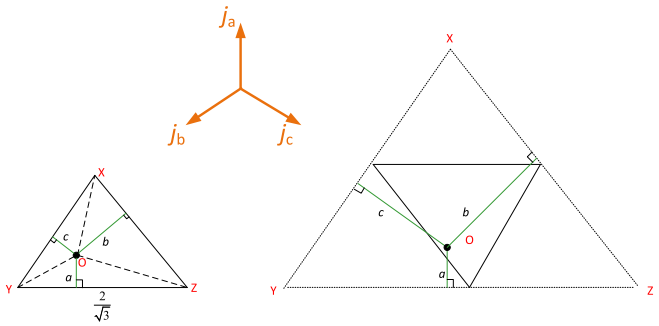


FIGURE 7. Illustration of how to obtain equations (4) and (5): left: for upright triangle, right: for upside down triangle.

diagram: one is an upright triangle as shown in Fig. 6(a) and the other one is an upside-down triangle as shown in Fig. 6(b).

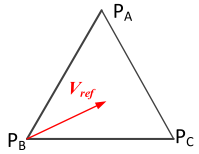
To determine which type of triangle the reference vector is located in, assuming the coordinates of the reference vector is (V_{rja}, V_{rjb}, V_{rjc}), then, it will be a upright triangle (Fig. 6(a)) if the condition in (4) is met. It will be an upside-down triangle (Fig. 6(b)) if the condition in (5) is met.

$$\underline{V_{rja}} + \underline{V_{rjb}} + \underline{V_{rjc}} = -1 \tag{4}$$

$$\underline{V_{rja}} + \underline{V_{rjb}} + \underline{V_{rjc}} = -2 \tag{5}$$

where, $\underline{V_{rja}}$, $\underline{V_{rjb}}$, $\underline{V_{rjc}}$ are the rounding down of the coordinates (V_{rja}, V_{rjb}, V_{rjc}) as integers (as voltage level). The conditions in (4) and (5), can be obtained from the illustration shown in Fig. 7 . The one on the left shows the case for the upright triangle. The black dot in the figure is the location of the reference vector. *a,b,c* represent the value that will be removed by rounding down the V_{rja}, V_{rjb}, V_{rjc}. Using the fact that the total area of the three small triangles (YOZ, ZOX, XOY) equal the area of the large triangle XYZ. Then, it can be worked out that $a + b + c = 1$. Given $V_{rja} + V_{rjb} + V_{rjc} = 0$, then if it is an upright triangle, $\underline{V_{rja}} + \underline{V_{rjb}} + \underline{V_{rjc}} = -1$, i.e., the condition in (4). Similarly, it can be worked out that $a+b+c=2$ for the upside down triangle shown on the right. Therefore, $\underline{V_{rja}} + \underline{V_{rjb}} + \underline{V_{rjc}} = -2$, i.e., the condition in (5).

$$P_A:(\underline{V_{rja}}+1,\underline{V_{rjb}},\underline{V_{rjc}})$$
$$P_B:(\underline{V_{rja}},\underline{V_{rjb}}+1,\underline{V_{rjc}})$$
$$P_C:(\underline{V_{rja}},\underline{V_{rjb}},\underline{V_{rjc}}+1)$$



$$P_A:(\underline{V_{rja}},\underline{V_{rjb}}+1,\underline{V_{rjc}}+1)$$
$$P_B:(\underline{V_{rja}}+1,\underline{V_{rjb}},\underline{V_{rjc}}+1)$$
$$P_C:(\underline{V_{rja}}+1,\underline{V_{rjb}}+1,\underline{V_{rjc}})$$

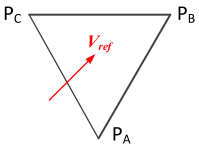


FIGURE 8. The coordinates of the vertexes for the two types of triangles.

As an example, if the coordinates of the reference vector (V_{ref}) is (V_{rja}, V_{rjb}, V_{rjc}) =(0.9, −1.2, 0.3) as shown in Fig. 5, then, ($\underline{V_{rja}}$, $\underline{V_{rjb}}$, $\underline{V_{rjc}}$) = (0, −2, 0). Hence, according to (5), the reference vector is located in a upside down triangle because $\underline{V_{rja}}+\underline{V_{rjb}}+\underline{V_{rjc}}=-2$, which is the case (an upside down triangle) as shown in Fig. 5. The criteria in (4) and (5) to judge whether it is an upright triangle or an upside down triangle can be used for a N-level converter. Also, the reference voltage is normalised by half of the dc-link voltage, i.e., $V_{\text{dc}}/2$ for a three-level converter. For an N-level converter, the base value will be $V_{\text{dc}}/(\text{N-1})$.

Next, the coordinates of the three vertexes of the triangle where the reference vector locates can be found out as: if it is an upright triangle, the vertexes are be given by (6). If it is an upside down triangle, they are given by (7).

$$\begin{aligned}
&P_A:(\underline{V_{rja}}+1,\underline{V_{rjb}},\underline{V_{rjc}})\\
&P_B:(\underline{V_{rja}},\underline{V_{rjb}}+1,\underline{V_{rjc}})\\
&P_C:(\underline{V_{rja}},\underline{V_{rjb}},\underline{V_{rjc}}+1)
\end{aligned}\tag{6}$$

$$\begin{aligned}
&P_A:(\underline{V_{rja}},\underline{V_{rjb}}+1,\underline{V_{rjc}}+1)\\
&P_B:(\underline{V_{rja}}+1,\underline{V_{rjb}},\underline{V_{rjc}}+1)\\
&P_C:(\underline{V_{rja}}+1,\underline{V_{rjb}}+1,\underline{V_{rjc}})
\end{aligned}\tag{7}$$

For example, again, if the coordinates of the reference vector (V_{rja}, V_{rjb}, V_{rjc}) =(0.9, −1.2, 0.3), as known earlier it is located in an upside down triangle, then the coordinates of the three vertexes can be obtained below from (7).

$P_{\text{A}} = (0, -2+1, 0+1) = (0, -1, 1)$
$P_{\text{B}} = (0+1, -2, 0+1) = (1, -2, 1)$
$P_{\text{C}} = (0+1, -2+1, 0) = (1, -1, 0)$

This is exactly what have been shown in the triangle in Fig. 5 where the reference vector locates and the three vertexes are (0, −1, 1), (1, −2, 1) and (1, −1, 0), respectively.

C. DURATION OF THE NEAREST THREE VECTORS IN THE IMAGINARY COORDINATE

The next step is to determine the time duration (t_{PA}, t_{PB}, t_{PC}) of each of the three vectors (nearest three vectors) of the triangle. The duration can be represented by the percentage (duty cycle) of the switching period as shown in (8), as d_{PA}, d_{PB}, d_{PC}.

$$\begin{cases} d_{PA} = \dfrac{t_{PA}}{T_s} \\ d_{PB} = \dfrac{t_{PB}}{T_s} \\ d_{PC} = \dfrac{t_{PC}}{T_s} \end{cases}\tag{8}$$

From the voltage-time equivalence as shown graphically in Fig. 6, the duration of each vector can be simply found as below.

$$d_{PA} = h_{PA}, \quad d_{PB} = h_{PB}, \quad d_{PC} = h_{PC}\tag{9}$$

h_{PA}, h_{PB}, h_{PC} represent the duration of the corresponding vectors at the vertexes, i.e., PA, PB, PC, respectively. The value of h_{PA}, h_{PB}, h_{PC} can be found from the distance between the coordinates of the reference vector and the rounding down integer (voltage level) of the coordinates. Therefore, the following distance (fractional part of the coordinates) is calculated first.

$$\begin{cases} \widetilde{v}_{rja} = V_{rja} - \underline{V_{rja}} \\ \widetilde{v}_{rjb} = V_{rjb} - \underline{V_{rjb}} \\ \widetilde{v}_{rjc} = V_{rjc} - \underline{V_{rjc}} \end{cases}\tag{10}$$

If the reference vector is located in an upright triangle, the duty cycle can be calculated as

$$d_{PA} = \widetilde{v}_{rja}, \quad d_{PB} = \widetilde{v}_{rjb}, \quad d_{PC} = \widetilde{v}_{rjc}\tag{11}$$

If the reference vector is located in an upside-down triangle, the duty cycle can be calculated as

$$d_{PA} = 1 - \widetilde{v}_{rja}, \quad d_{PB} = 1 - \widetilde{v}_{rjb}, \quad d_{PC} = 1 - \widetilde{v}_{rjc}\tag{12}$$

In summary, now, the coordinates of the three vertexes are obtained. The duration of each vector (vertex) is also obtained, which is very simple. The above process is generic and not specific to the three-level converter so it can be used for multi-level converters with any number of levels without increasing the complexity. Normally, each vertex corresponds to several (redundant) vectors in the *a-b-c* coordinate system. The next step is to determine which redundant vectors to select and their sequences.

D. IDENTIFY THE REDUDANT VECTORS

With the proposed method based the imaginary coordinate system, the redundant vectors in the *a-b-c* or α-β coordinate can be worked out directly, without the need to transfer back to the *a-b-c* coordinate and without look-up tables, which is one of the advantages of the proposed method. In fact, the zero-sequence component is used to replace the complexity of selecting redundant vectors.

As shown earlier, the coordinates of the three vertexes in the imaginary coordinate system were given by (6) and (7), which are also rewritten in Fig. 8 for the upright triangle and the upside-down triangle, respectively.

Now the question is how to find the corresponding (redundant) vectors.

From (1), there is

$$\begin{cases} v_a - v_b = v_{jc} \\ v_b - v_c = v_{ja} \\ v_c - v_a = v_{jb} \end{cases} \tag{13}$$

For the vertexes (voltage vectors), v_a, v_b, v_c are integers (e.g., 1, 1, 0 for a vertex in Fig. 3) in the *a-b-c* coordinate system. v_{ja}, v_{jb}, v_{jc} are also integers for the vertexes in the imaginary coordinate system as shown in Fig. 5. From (13), there is

$$\begin{cases} v_a = v_a \\ v_b = v_a - v_{jc} \\ v_c = v_a + v_{jb} \end{cases} \tag{14}$$

For a three-level converter, the value range for v_a, v_b, v_c in the *a-b-c* coordinate is between 0 and 2, i.e., 0,1,2. Hence, there is

$$\begin{cases} 0 \le v_a \le 2 \\ 0 \le v_b \le 2 \\ 0 \le v_c \le 2 \end{cases} \tag{15}$$

Now, with the value boundary given in (15) for v_a, v_b, v_c, (14) can be turned into (16) below.

$$\begin{cases} 0 \le v_a \le 2 \\ 0 \le v_a - v_{jc} \le 2 \\ 0 \le v_a + v_{jb} \le 2 \end{cases} \tag{16}$$

Hence, from (16), the value range of v_a must meet those in (17) below.

$$\begin{cases} 0 \le v_a \le 2 \\ v_{jc} \le v_a \le 2 + v_{jc} \\ -v_{jb} \le v_a \le 2 - v_{jb} \end{cases} \tag{17}$$

Therefore, v_a must be larger than the maximum of the three values: 0, v_{jc} and -v_{jb} as shown on the left in (17). Here, a v_{aFloor} is defined, which shows the minimum (floor) of the v_a.

$$v_{aFloor} = \max\{0, v_{jc}, -v_{jb}\} \tag{18}$$

In the meantime, v_a must be smaller than the minimum of the three values 2, 2+v_{jc}, 2-v_{jb} as also shown on the right in (17). Here, a v_{aCeil} is defined, which shows the maximum (ceiling) of the v_a.

$$v_{aCeil} = \min\{2, (2 + v_{jc}), (2 - v_{jb})\} \tag{19}$$

In other words, there is

$$v_{aFloor} \le v_a \le v_{aCeil} \tag{20}$$

From the boundaries in (20) or (17), the corresponding vectors (vertexes) in the *a-b-c* coordinates can be worked out from the vertex in the imaginary coordinate. For example, for the vertex (v_{ja}, v_{jb}, v_{jc}) = (1, −1, 0) in the imaginary coordinate as shown in Fig. 9(a), the maximum of (0, v_{jc}, $-v_{jb}$) = (0,0,1) is 1, which is v_{aFloor}. The minimum of (2, 2+v_{jc}, 2-v_{jb}) = (2, 2, 3) is 2, which is v_{aCeil}. In other words, from (20), there is

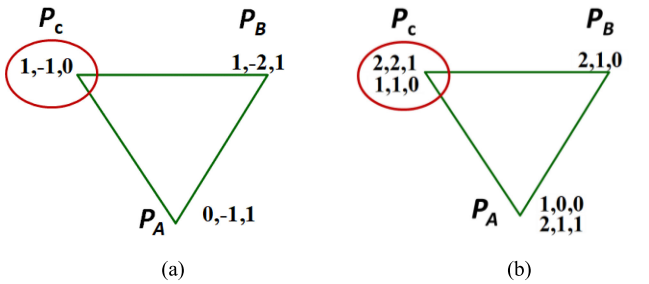


FIGURE 9. A triangle example and its vertexes in the imaginary coordinate and the *a-b-c* coordinate. (a) Imaginary coordinate. (b) *a-b-c* coordinate.

$$1 \le v_a \le 2$$

Therefore, the values for v_a can be either 1 or 2. Once the value for v_a is worked out, the value for v_b and v_c can be easily obtained by (14). For $v_a = 1$, then from (14) and $v_{jb} = -1$, $v_{jc} = 0$, there are $v_b = 1$, $v_c = 0$. Therefore, one coordinate of the vertex in the *a-b-c* coordinate system will be (1,1,0). For $v_a = 2$, again from (14) and $v_{jb} = -1$, $v_{jc} = 0$, there are $v_b = 2$, $v_c = 0$. Therefore, the other coordinate of the vertex will be (2, 2, 1). This is exactly what have been shown in the *a-b-c* coordinate in Fig. 3, also shown for vertex P_c in Fig. 9(b). The coordinate values of the other two vertexes P_B and P_A in the *a-b-c* coordinate system can also be easily obtained in the same way.

For converters with other number of levels (e.g., a N-level converter), the above process can also be used. The only thing needs to modify is to change the upper value limit of v_a from 2 (for three-level) to N-1 (for N-level) in (15).

It should be noted that the identification of the redundant vectors in the *a-b-c* coordinate is not necessary as a step in the modulation process, but it is just given here to show the redundant vectors can be obtained directly if needed (without converting back to the *a-b-c* coordinate or using a look-up table).

E. DETERMINING THE REQUIRED ZERO-SEQUENCE COMPONENTS (EQUIVALENT TO REDUNDANT VECTORS)

The essence of selecting redundant vectors is adding different amount of zero-sequence component to the fundamental components (three-phase sinusoidal) to obtain the final modulation signal [1]. Therefore, in the following, the corresponding zero-sequence components of the redundant vectors will be identified and selected. The advantages of this approach are twofold: first, it does not require transforming back to the *a-b-c* or α-β coordinate system or using a look-up table to select the redundant vectors. Second, this approach avoids determining the starting vector and the rotating directions (clockwise or anti-clockwise), i.e., the sequence of the vectors, which much simplifies the process.

The overall process is described here. First, the minimum zero-sequence component of the three vertexes (vectors) will be determined. Then, the amount of zero-sequence component can be added is also determined and evaluated against the control objective. Finally, the optimal amount of zero-sequence component is selected to form the final modulation signal. From the definition of the zero-sequence component (v_{zero}) and (14), there is

$$v_{zero} = \frac{v_a + v_b + v_c}{3} = \frac{v_a + v_a - v_{jc} + v_a + v_{jb}}{3} = v_a + \frac{1}{3}(v_{jb} - v_{jc}) \tag{21}$$

Therefore, the minimum zero-sequence component at each vertex can be obtained by

$$v_{\text{zeroMin}} = v_{aMin} + \frac{1}{3}(v_{jb} - v_{jc}) \tag{22}$$

where, v_{aMin} is the minimum value of the coordinate a (phase a) of each vertex. Again, v_{aMin}, v_{jb} and v_{jc} are integers (because of vertexes). As an example, for the triangle shown in Fig. 9(b), the v_{zeroMin} for the vertexes P_{A}, P_{B}, P_{C} can be calculated as $P_{\text{A}} = 1 + 1/3 \times (-1-1) = 1/3$; $P_{\text{B}} = 2 + 1/3 \times (-2-1) = 1$ and $P_{\text{C}} = 1 + 1/3 \times (-1-0) = 2/3$. From v_{zeroMin}, it immediately tells the P_{A} has the lowest zero sequence value, followed by P_{C} and P_{B}. Therefore, the vectors must start from the lowest zero sequence one, i.e., P_{A} then to P_{C}, then to P_{B}. This is exactly what the vectors in Fig. 9(b) tells: the sequence of the vectors must be 100 (P_{A})— 110 (P_{C}) — 210 (P_{B})—211(P_{A})—221 (P_{C}).

By putting the zero-sequence in order according to their values, the corresponding redundant vectors will line up accordingly. In this way, the process of determining the starting vector and figuring out the sequence of the redundant vectors in conventional methods are avoided. They are all done by sorting the zero-sequence values from low to high.

As is well known, there are two kinds of modulations: one is the 'two-phase' mode, also called the '5-segment' mode, where only two phases change voltages in each switching period and the third phase keeps unchanged. Only three vectors are used for this mode. This mode benefits from less switching actions, hence lower switching loss. The other one is the 'three-phase' mode, also called the '7-segment' mode, where all the three phases change voltages in each switching period. This mode has lower high-frequency harmonics.

Here, the 'two-phase' mode is used as an example to demonstrate the idea of how to select the zero-sequence component. The case for the 'three-phase' mode will be given in the Appendix. In the following, the equivalent minimum zero-sequence component of the three vertexes (vectors) is worked out first. Then, the variable amount of zero-sequence component that can be added is worked out. Finally, the optimal zero-sequence component will be selected.

In one switching period, the equivalent minimum zero-sequence components of the three vertexes can be calculated as in (23), i.e., the minimum zero sequence component

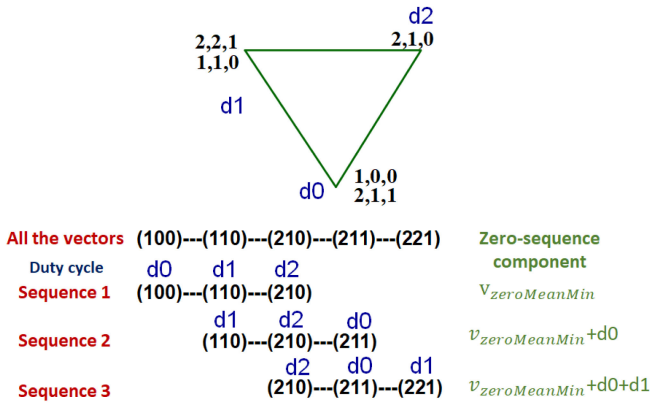


FIGURE 10. Illustration of adding zero-sequence components and its relation to redundant vectors.

(v_{zeroMin}) at each vertex is multiplied by the duty cycle d of each vertex.

$$v_{zeroMeanMin} = \sum_{i=0}^{2} (v^i_{\text{zeroMin}} \cdot d_i) \tag{23}$$

where, $i = 0, 1, 2$ represent the three vectors at the three vertexes, respectively. The v_{zeroMin} at each vertex can be calculated by (22) and the duty cycle (duration) of each vertex was calculated by (11) and (12).

As an example, all the space vectors for the triangle in Fig. 9(b) is shown again in Fig. 10. There are five vectors. For a two-phase mode modulation, there will be three possible vector sequences (sequence 1, 2, 3 as shown in the figure). The duty cycle for each vertex (vector) is shown in the figure as well, i.e., d_0, d_1, d_2, which is the same as what has been defined in (23). For the Sequence 1, it has the lowest zero-sequence component vectors (100-110-210), which can be obtained by by $v_{\text{zeroMeanMin}}$ given in (23). For the other sequences, although the vectors involved are different, the fundamental difference is only the zero-sequence component. For the Sequence 2, the zero sequence component of the vectors 110 and 210 are the same as those given in Sequence 1. The zero sequence component of 211 is larger than 100 but their duration are the same, i.e., d_0. Therefore, the additional zero-sequence component between Sequence 2 and Sequence 1 can be calculated as (211-100)/3 $\times$ d_0 = (2 + 1 + 1-1-0-0)/3 $\times$ d_0 = d_0. Hence, the zero-sequence component for Sequence 2 can be calculated as $v_{\text{zeroMeanMin}}$ (Sequence 1)+d_0. Similarly, the zero-sequence component difference between Sequence 3 and Sequence 2 is (2 + 2 + 1-1-1-0)/3 $\times$ d_1 = d_1. Therefore, the zero-sequence component of Sequence 3 will be $v_{\text{zeroMeanMin}}$ +d_0 +d_1.

To summarize and generalize for converters with other number of voltage levels, the zero-sequence component for various vector sequences can be calculated as

$$v_{\text{zeroMean}} = \sum_{i=0}^{2} (v^i_{\text{zeroMin}} \cdot d_i) + \sum_{l=0}^{SumVect-4} d_i \,|_{i=l\%3} \tag{24}$$

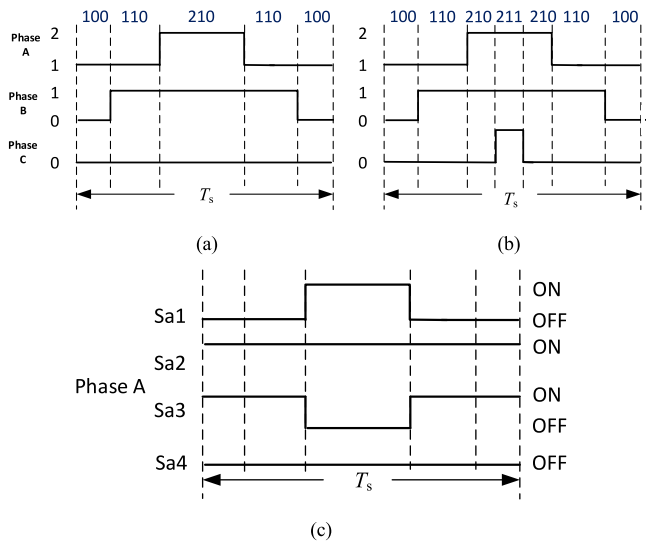


FIGURE 11. Switching pattern example for the (a) two-phase mode and (b) the three-phase mode and (c) the gate pulses for the four switching devices in Phase A for the two-phase mode.

where the first part of (24) is the minimum zero-sequence component $u_{\text{zeroMeanMin}}$, corresponding to the zero-sequence component of the Sequence 1 in Fig. 10. The second term in (24) is the variable zero-sequence component that can be added, i.e., d_0, d_1, etc, corresponding to other vector sequences in Fig. 10. In (24), l can be seen as various layers of zero-sequence components to be added. l %3 means the residual of l divided by 3. For example, if $l = 0$, $i = l$ % 3=0, then d_0 as the zero-sequence component will be added. If l=1, d_1 will be added.

The total number of layers (l) that can be selected to be added can be worked out as follows. First, the total number of vectors at the three vertexes can be calculated by

$$sumVect = \sum_{i=0}^{2} (v^i_{aCeil} - v^i_{aFloor} + 1) \tag{25}$$

u_{aCeil} and u_{aFloor} were given in (18) and (19). $i = 0, 1, 2$ represents the three vertexes. For the case in Fig. 9(b), it can be calculated that there are 5 vectors in total. Then, if a two-phase mode is used, the number of possible sequences will be the total number of vectors minus 2, i.e., *sumVector* − 2=5–2=3. There are 3 possible sequences as demonstrated in Fig. 10. The number of layers (l) of variable zero-sequence component that can be added on top of the minimum zero-sequent component is therefore *sumVector*-3=5-3=2. As in (24), l starts from 0, so the upper limit for l is therefore set as *sumVector*-4 as shown in (24), i.e., 5-4=1 for the case in Fig. 10. layer=0 and 1 corresponds to the Sequences 2 and 3. For the three-phase mode, the minimum zero-sequence component that can be added and the variable part of the zero-sequence component can be found in the Appendix. Fig. 11 shows the switching pattern for the two-phase mode (100-110-210) and three-phase mode (100-110-210-211) within a switching period. Fig. 11(c) also shows the gate pulses for the four switching devices of Phase A for the two-phase mode. The following section will explain how to select the optimal zero-sequence component from (24) for control purposes.

It should be noted that the adjustment and selection of the zero-sequence component will determine which vectors will be used for the 2-phase mode modulation. For the 3-phase mode, the adjustment and selection of the zero-sequence component will not only determine which vectors will be used but also the duration (proportion) of the starting and ending vectors (e.g., 100, 211) in Fig. 11.

F. SELECTING THE OPTIMAL ZERO-SEQUENCE COMPONENT

In this section, the selection process of the optimal zero-sequence component for dc-link capacitor voltage balancing will be explained as a control example. Various layers of zero sequence component as shown in (24) can be evaluated to see which one leads to the optimal control objective.

For example, for a three-level NPC converter, to minimize the dc-link neutral point (NP) voltage variation, the control objective can be set as (26) [1].

$$\min V = \left| V_{dc1} + \Delta V_{dc1} - \frac{V_{dc1} + V_{dc2}}{2} \right| \tag{26}$$

where, V is the control objective and V_{dc1}, V_{dc2} are the dc-link capacitor voltages as shown in Fig. 2. The objective of (26) is to let the lower capacitor voltage be as close to half of the dc-link voltage as possible. In each switching period, the NP voltage variation ΔV_{dc1} can be calculated by

$$\Delta V_{dc1} = \frac{i_0}{2} \times \frac{T_s}{C} \tag{27}$$

where, i_0 is the neutral current as shown in Fig. 2, T_{s} is the switching period, and C is the capacitance of the upper or lower dc-link capacitor. When any output phase is clamped to the NP during the middle level '1', the neutral current will flow and affect the NP voltage. Assuming that the neutral current i_0 is constant within one switching period, the average neutral current in one switching period can be calculated as the product of the phase current i_x (x = a,b,c) and the NP connection time duration of the corresponding phase [1]. The actual phase current can be measured by output current sensors, and the time duration connecting to the NP can be easily determined from the reference voltage. If the integer part of the reference voltage v_x ($x = a, b, c$) is 0 (level 0), the NP time duration will be the fractional part of v_x (Sa2 and Sa3 are ON). On the other hand, if the integer part of the reference voltage v_{x} is 1 (level 1), the NP time duration will be 1 minus the fractional part of v_x. Here, the reference voltage is unified (divided) by half of the dc-link voltage so the value range of the reference voltage v_x is in the range of 0∼2. Thus, the average neutral current can be calculated by

$$\overline{i_0} = \sum_{x=a,b,c} i_x \times ((1 - \text{int}(v_x)) \times frac(v_x) + \text{int}(v_x)$$

$$\times (1 - frac(v_x))) \tag{28}$$

where, int(v_x) denotes the integer part of v_x and $frac(v_x)$ denotes the fractional part of the v_x in the unified system.

As mentioned, the control objective is to let the voltage of the capacitor C_1 to be as close to the half of the dc-link voltage in the next switching cycle as in (26). Now, the voltage variation of capacitor C_1 in the next switching cycle can be predicted by (27), which shows that the NP current i_o will affect the capacitor voltage variation. From (28), it is obvious that the NP current i_o is affected by the voltage reference v_x, which can be adjusted by the zero-sequence component. Therefore, various zero-sequence components can be evaluated to see how they affect v_x, then i_o, then the control objective in (26).

From (21), the reference voltage v_x can be expressed as

$$\begin{cases} v_a = v_{\text{zeroMean}} - (V_{rjb} - V_{rjc})/3 \\ v_b = v_{\text{zeroMean}} - (V_{rjc} - V_{rja})/3 \\ v_c = v_{\text{zeroMean}} - (V_{rja} - V_{rjb})/3 \end{cases} \tag{29}$$

where, V_{rja}, V_{rjb}, V_{rjc} are the coordinates of the reference vector in the imaginary plane as defined earlier in Part B of Section II. For example, (V_{rja}, V_{rjb}, V_{rjc}) =(0.9, −1.2, 0.3) as used at the beginning of Section II.

Each possible zero-sequence component v_{zeroMean} in (24) will be evaluated against the control objective in (26), through first obtaining v_x by (29), then i_0 in (28) and then ΔV_{dc1} in (27). And the zero sequence component that leads to the minimum of the objective in (26) will be selected and will be used to get the final reference voltage v_{x} in (29). Then, this reference voltage v_{x} can be used to compare with the carrier signal to generate the gate pulses for the switching devices and the modulation process is complete. In summary, there are three steps in working out the required zero-sequence components and hence the final modulation signal: Step 1, work out the available zero-sequence components, i.e., equation (24); Step 2, evaluate zero-sequence components against the control objective, i.e., equation (26); Step 3, final modulation signal can be obtained by equation (29). A flowchart describing the full modulation process in given in Fig. 12.

For dc-link capacitor voltage balancing of converters with higher number of voltage levels, the control objective can be defined according to [21]. For other control purposes, such as mitigating the common-mode voltage, the selection of the zero-sequence component based on the imaginary coordinate system can be found in [1].

As can be seen, the modulation and control algorithm can be applied to converters with higher number of voltage levels without increasing much calculation.

The proposed PWM can be used for closed-loop control system with current/voltage control. For example, with current controllers implemented in the rotating *d-q* frame as widely used for rectifiers and motor control, the output of the current controllers will be the reference voltage (u_{d}, u_{q}). Then, through inverse park transformation, the reference voltage vector V_{ref} in the form of (u_α, u_β) or (u_{a}, u_{b}, u_{c}) will be obtained. Then, using the transformation matrix in equations

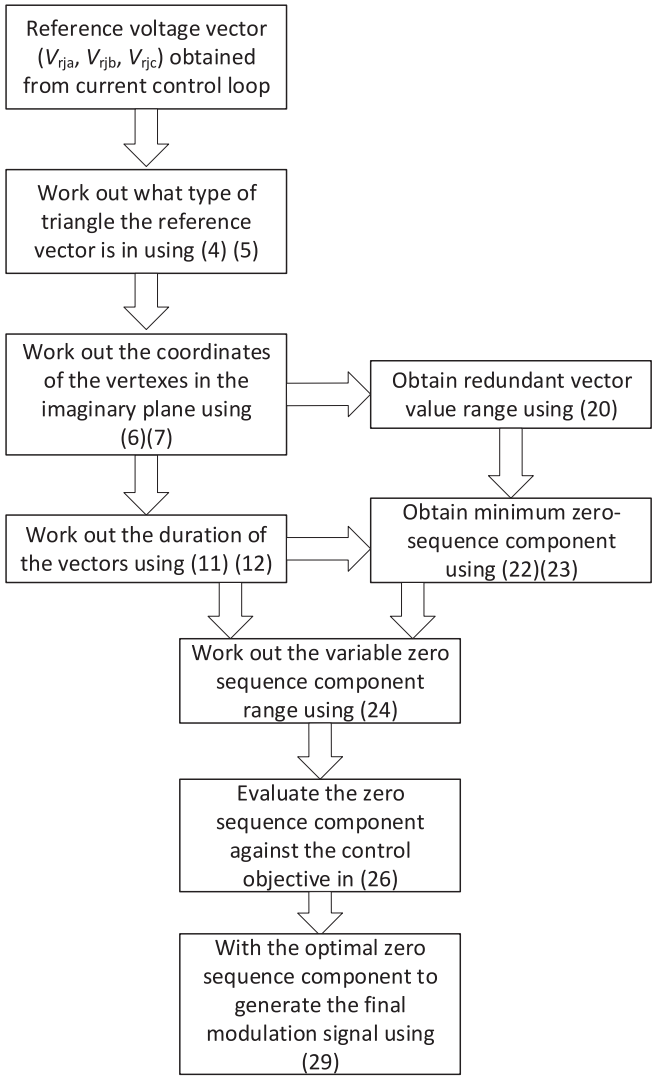


FIGURE 12. **Flowchart showing the full modulation process.**

(1)-(3), the reference vector can be transferred to the imaginary coordinate and the SVPWM process presented in this paper can be used.

The SVPWM presented in this paper can be used for various topologies, such as those with reduced device count [24], cascaded H-bridge converters [25]. First, it can generate the required voltage with extended modulation index. Then, how to select between the redundant switching states depends on the specific topology and control objective.

III. EXPERIMENTAL TEST AND RESULTS

The proposed modulation and control have been tested and used in various multilevel converter prototypes and products. Here, two examples are given to show the effectiveness of the presented method. The first is a 10 kW back-to-back three-phase three-level diode NPC converter as shown in Fig. 13. Three-level IGBT modules are used (SK 50 MLI 066 from Semikron) as the switching devices. The converter is tested with various switching frequencies from 10 kHz to 100 kHz.

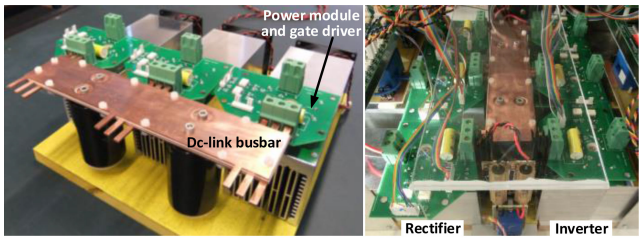


FIGURE 13. A three-level converter prototype. (a) Part of the converter. (b) Back-to-back converter prototype.

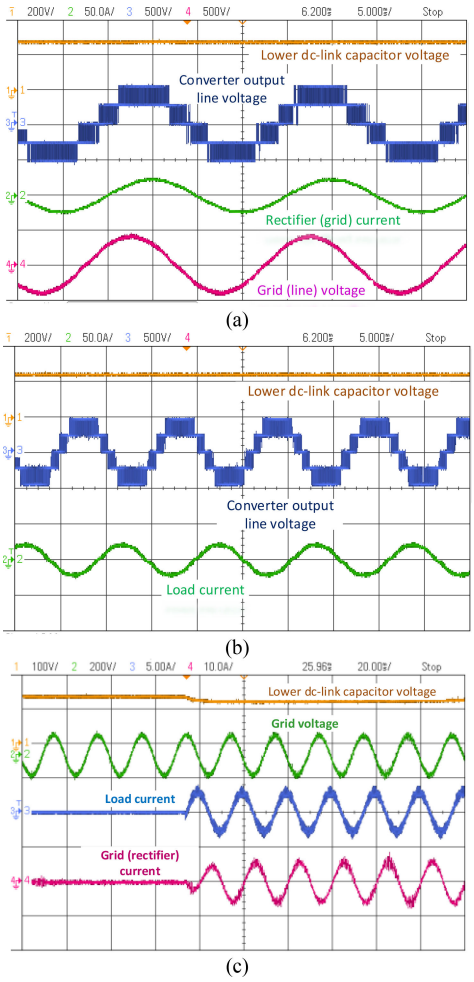


FIGURE 14. Three-level converter experimental results. (a) Rectifier operation. (b) Inverter operation. (c) Back-to-back operation during load increase.

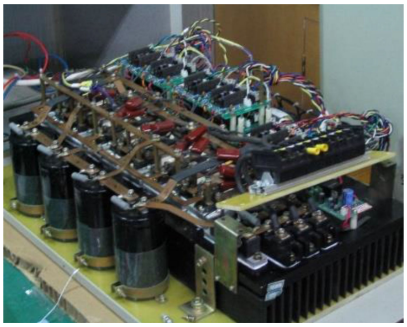


FIGURE 15. A five-level diode NPC converter.

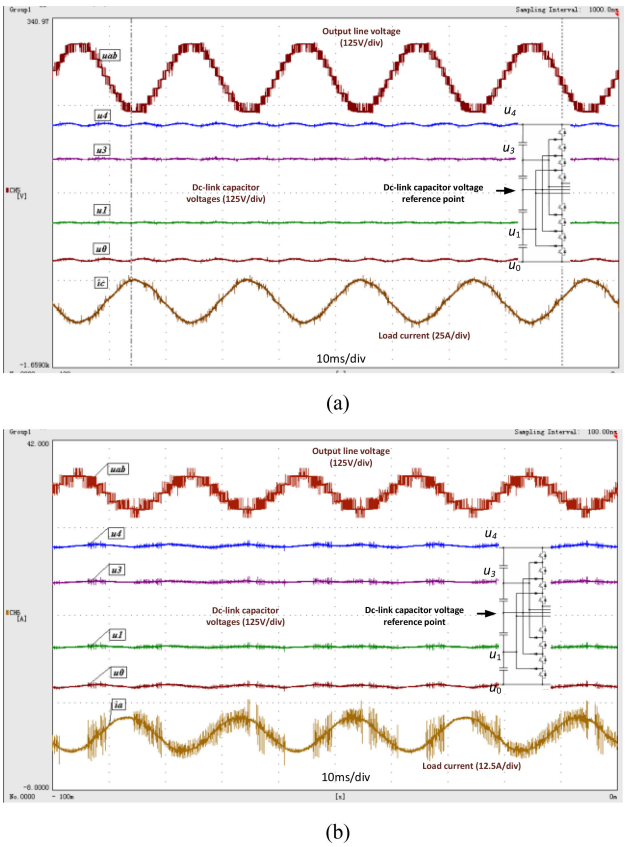


FIGURE 16. Experimental waveforms for the five-level diode NPC converter. (a) At modulation index=1 and zero power factor; (b) at modulation index=0.52 and power factor=1. Output line voltage, dc-link voltages at the reference points U_0, U_1, U_3, U_4 as denoted in the figure, load current.

For the rectifier mode with a unity power factor, the waveforms are shown in Fig. 14(a). As seen, the lower dc-link capacitor voltage is almost constant, which is half of the total dc-link voltage of 527 V. This shows the effectiveness of the control for regulating the dc-link capacitors' voltages. The converter output line voltage has five levels as expected for a three-level converter. The switching frequency is 40 kHz and the current (i_a) is controlled to be sinusoidal. The grid line voltage (u_{ab}) is also shown, which leads the Phase A current by 30 degree. Fig. 14(b) shows the waveforms of the inverter, where a R-L (11Ω, 0.24 mH) load has been used and the switching frequency is 60 kHz. All the waveforms are as expected which validates the modulation and control. Fig. 14(c) shows the back to back operation during load increase.

A five-level three-phase diode NPC converter as shown in Fig. 15 has also been built using Si IGBTs and diodes and tested using the proposed imaginary-coordinate based

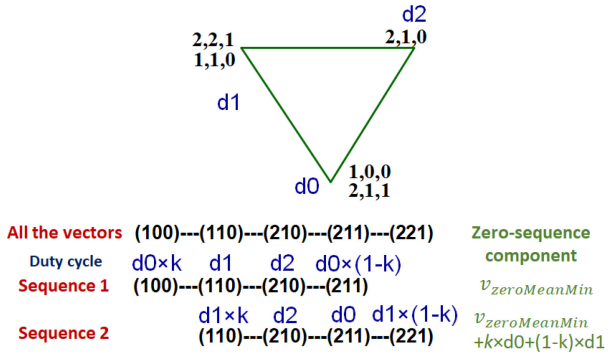


FIGURE 17. Illustration of adding zero-sequence components and its relation to redundant vectors for the three-phase mode modulation.

SVPWM and control. The total dc-link voltage is 200V and the switching frequency is 4 kHz. The five-level converter is tested under various power factors and modulation indexes. As known, at high modulation indexes, the voltages of the four dc-link capacitors can only be balanced for low power factor operation [17], [23] if the switching pattern in Fig. 1(a) is used. Here, a three-phase capacitive load with almost pure reactive power (zero power factor) is used to demonstrate the effectiveness of the modulation and control at modulation index=1, where the four dc-link capacitors' voltages can be well regulated at the reference of 50V each. The converter output line voltage has 9 levels as expected as shown in Fig. 16(a). Fig. 16(b) shows the operation at a modulation index=0.52 and unity power factor. Because this is a lower modulation index, the dc-link capacitor voltages can be well regulated even at unity power factor. There are harmonics in the current waveform, which was due to the measurement noise coupled to the probe. This test again has validated the effectiveness of the proposed SVPWM. The DSP controller for both the above two examples is TMS320F2812.

Regarding the dc-link voltage utilization, if the modulation index is defined as the peak of the phase voltage divided by half of the dc-link voltage, then sine PWM can achieve a modulation index of 1. And the proposed SVPWM can achieve a modulation index of 1.15, similar to other SVPWM schemes.

IV. CONCLUSION

This paper has provided a step-by-step guidance for implementing the imaginary-coordinate-based multilevel SVPWM. As shown, it can be used for multilevel converters with any number of levels and the complexity does not increase with the number of levels. The zero-sequence component that can be added and adjusted have been derived in this paper for both 'two-phase' mode and 'three-phase' mode, which avoids the transformation back to the original *a-b-c* or α-β coordinate to select the redundant vectors. The presented modulation and control have been validated on three-level and five-level converter platforms. It is the authors' hope that this paper can be archived as a milestone in the development of multilevel PWM methods and this paper can enable this method to be understood and adopted by more researchers given its advantages. Also, various other control objectives such as harmonics optimisation [26] can be further explored with this method for future work.

APPENDIX

The following shows the expressions of the minimum zero-sequence component and the variable zero-sequence components that can be added for the 'three-phase' mode modulation. Fig. 17 shows an example of the switching vectors, sequences and the corresponding zero-sequence component. Different from the 'two-phase' mode, in each switching sequence, four vectors are used. The starting and ending vector (e.g., 110 and 221) will share the time duration of d_0, where k is the ratio between the time shared between the two redundant vectors 110 and 221.

Following the same derivation process for the two-phase mode, for the three-phase mode, the minimum zero-sequence component can be calculated as

$$v_{zeroMeanMin} = \sum_{i=0}^{2} (v^{i}_{\text{zeroMin}} \cdot d_i) + d_0 \cdot (1-k) \tag{30}$$

From (30), when $k = 1$, meaning only 100 is used, which is effectively the two-phase mode, the expression of (30) becomes exactly the same as what has been shown for the two-phase mode in (23) so the two-phase mode can be seen as a special case of the three-phase mode.

The full zero sequence component can be expressed as

$$v_{\text{zeroMean}} = \sum_{i=0}^{2} (v^{i}_{\text{zeroMin}} \cdot d_i) + d_0 \cdot (1-k) + \sum_{l=0}^{SumVect-5} \left[k \cdot d_i + (1-k) d_{i+1}\right] |_{i=l\%3} \tag{31}$$

As seen, there are two degrees of control freedom here: the first is to choose different layers (l) of zero sequence components and the second is to choose the ratio k between the starting and ending vectors (again, different amount of zero sequence component). These two freedoms can be evaluated against the control objective to find the optimal zero-sequence component. The derived zero-sequence component expression in (31) is shown for the first time in literature. Also, the number of switching sequences of the three-phase mode is one less than the two-phase mode, so *sumVect*-5 is used in (31) instead of *sumVect*-4 in (24).

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