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23-level Single DC Source Hybrid PUC (H-PUC) Converter Topology With Reduced Number of Components: Real-Time Implementation With Model Predictive Control

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ABSTRACT In this paper, a new configuration of single DC source hybrid packed U-cell (H-PUC) converter with reduced number of components is proposed. The proposed H-PUC only requires one dc source, twelve power switches, and three capacitors to provide 23-level output voltage. It is comprised of two high voltage low frequency (LF) and low voltage high frequency (HF) sub-modules which leads to less power losses and higher efficiency of the proposed H-PUC converter. Moreover, a finite control set model predictive control (FCS-MPC) method is proposed to generate 23-level staircase output voltage with low THD and to regulate voltages of three capacitors to their desired values simultaneously. A real-time model of the proposed 23-level H-PUC converter and its suggested FCS-MPC are developed and implemented in OPAL-RT OP4510 platform to evaluate and validate the feasibility of the proposed H-PUC in grid-connected operation mode. The provided real-time implementation results verify and demonstrate the performance and viability of the proposed 23-level H-PUC and its associated FCS-MPC to provide low THD 23-level output voltage and all three capacitors voltages balancing.

INDEX TERMS Grid-connected converter, hybrid puc (h-puc), model predictive control (mpc), multilevel inverter (mli), packed u-cell (puc), real-time simulation, single dc source.

I. INTRODUCTION

The global adoption rate of renewable energy sources has been increasing significantly in the past years and shows no sign of slowing down. More specifically, solar energy is becoming increasingly popular in many parts of the world. As such, proper power electronic devices need to be developed in order to meet the appropriate grid power quality requirements [1]. Indeed, the main requirement for a photovoltaic system is a suitable voltage source inverter (VSI), which converts the DC voltage generated by the photovoltaic arrays to AC voltage that can be injected to the grid [2].

Furthermore, the injected current to the grid must meet requirements compelled by stringent standards in terms of harmonic content reduction, identified as total harmonic distortion (THD). One method of reducing this harmonic pollution on the grid is to use passive, active or hybrid filters as interfacing components connected between the inverter circuit and the grid at the point of common coupling (PCC) [3].

Nonetheless, it is possible to considerably reduce the harmonic content of the injected power without the use of additional filters by using multilevel types of inverters. The latter offer a better solution than conventional inverters as they are

capable of providing low THD staircase multilevel output voltage, low electromagnetic interference (EMI), low dv/dt, and lower switching frequency. This results in overall cleaner waveforms with less harmonic distortion, which in turn reduces or even eliminates the requirement for bulky passive or hybrid filters [4]–[8]. Some popular multilevel inverter topologies include the cascaded H-bridge (CHB), the neutral-point-clamped (NPC) and the active neutral-point-clamped (ANPC) inverters. However, these topologies are only feasible to provide lower number of output voltage levels and the number of required DC sources, power switches, diodes, and capacitors are significantly increased at higher number of output voltage levels [9]–[14].

A new breed of multilevel inverters, known as the packed U-Cell, is able to overcome the limitations previously mentioned. These inverters can generate a high number of voltage levels while using a smaller number of active switches and passive components [15]–[18]. In fact, some specific applications of the PUC converters have shown the ability to generate 7, 9 and even 15 voltage levels with a single DC source, isolated or generated by photovoltaic arrays [19]–[21]. These higher number of output voltage levels are attained by using more complex control methods that usually employ some form of sine pulse width modulation (SPWM) or space vector modulation (SVM) [22], [23].

Recently, hybrid multilevel inverters formed by cascade connection of two or more sub-modules are introduced in the literature. Applying asymmetrical ratio of isolated DC links to the sub-modules results in higher number of output voltage levels by employing reduced number of components in hybrid multilevel inverters [24], [25]. However, hybrid multilevel inverters require two or more isolated DC sources or high frequency links to provide multiple isolated DC links. Hence, the complexity and cost of hybrid multilevel inverters are increased [26].

To overcome the above mentioned frailties, this paper proposes the single DC source hybrid PUC (H-PUC) inverter and its suggested FCS-MPC to provide 23-level output voltage with less number of components. The 23-level output voltage with low THD and voltage balancing of all capacitors are obtained by employing the proposed FCS-MPC in the proposed H-PUC. Hence, the proposed H-PUC only needs one isolated DC source and the high frequency link is eliminated from this configuration. This paper is organized as follows. The general topology and its mathematical model are developed and presented in Section II. Then, in Section III, the model predictive controller is designed for 23 output voltage levels and tested in grid-connected mode. Subsequently, in Section IV, the real-time equivalent model of the proposed converter is discussed. Finally, the designed converter-controller is simulated in real-time and validated in Section V.

II. HYBRID PUC (H-PUC) INVERTER TOPOLOGY

A. PRESENTATION OF THE CIRCUIT TOPOLOGY

The proposed H-PUC configuration is comprised of two sub-modules that are based on the PUC topology, which was

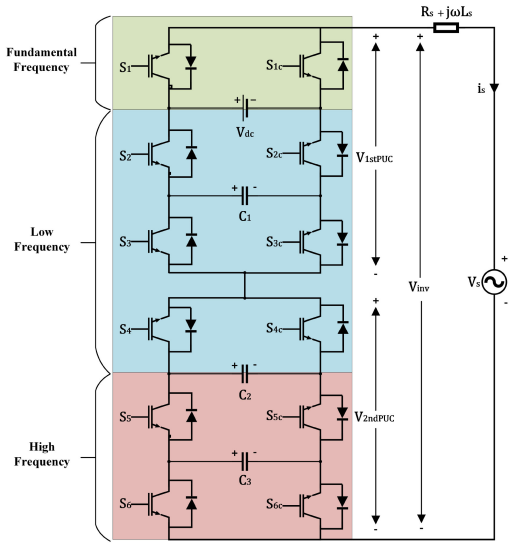

FIGURE 1. The Proposed Hybrid PUC (H-PUC) Inverter Topology with Single DC Source.

first introduced in [18]. It is composed of 6 active switches, one DC voltage source and one DC capacitor. This topology can be used in single-phase system configuration, operating in either inverter or rectifier modes. In single-phase inverter mode, the basic form of the converter, called PUC5, can generate five voltage output levels and has the ability to self-balance the DC capacitor voltage to one half of the main DC source without the use of voltage sensors thanks to appropriate modulation techniques [27]. In addition, the same converter topology is capable of generating 7 voltage output levels (PUC7) when paired to an appropriate control technique that regulates the DC capacitor voltage to one third of the main DC source [28]. The proposed single dc source H-PUC inverter is formed by cascade connection of two PUC5 sub-modules with quinary ratio.

In [29] and [30], multilevel converter composed of two cascaded PUC7 converters have been introduced, but they require two or more DC sources to achieve a high number of voltage output levels. Similarly in [31], the Q-HNPC is proposed as a modular approach to cascaded multilevel inverters based on HNPC and PUC5 converters has been presented, but again multiple DC sources are necessary for proper operation. In this paper, the proposed topology, shown in Fig. 1, is based on a cascade connection of two PUC5 inverters where the DC source of the second converter is replaced by a voltage regulated DC capacitor, which reduces the burden of using multiple isolated bidirectional DC sources. Additionally, as shown in Fig. 1, only 4 of the 12 switches operate at high switching frequency, whereas 6 switches operate at lower frequencies, and the first 2 complementary switches operate at fundamental frequency. This results in overall higher efficiency since higher voltages like V_{dc} are switched at lower frequencies.

The use of a model predictive controller requires prior knowledge of all possible switching states of the converter [32]–[34]. Since the proposed converter is composed of 6 pairs of complementary switches (S_1 to S_6

TABLE 1. Possible Switching States and Capacitor Charging States of 1st and 2nd PUC

1st PUC States					
State	**S1**	**S2**	**S3**	**C1**	V_{1stPUC}
1	0	0	0	–	0
2	0	0	1	↓	$-V_{c1}$
3	0	1	0	↑	$V_{c1}-V_{dc}$
4	0	1	1	–	$-V_{dc}$
5	1	0	0	–	V_{dc}
6	1	0	1	↑	$V_{dc}-V_{c1}$
7	1	1	0	↓	V_{c1}
8	1	1	1	–	0
2nd PUC States					
State	**S4**	**S5**	**S6**	**C2**	**C3**	V_{2ndPUC}
1	0	0	0	–	–	0
2	0	0	1	–	↓	$-V_{c3}$
3	0	1	0	↓	↑	$V_{c3}-V_{c2}$
4	0	1	1	↑	–	$-V_{c2}$
5	1	0	0	↑	–	V_{c2}
6	1	0	1	↓	↑	$V_{c2}-V_{c3}$
7	1	1	0	–	↓	V_{c3}
8	1	1	1	–	–	0

and S_{1c} to S_{6c}), there are in total $2^6 = 64$ possible switching states for this topology. However, individually each of the two PUC5 converters has $2^3 = 8$ possible switching states. Thus, for the sake of conciseness, only the states of each individual PUC5s (1st PUC and 2nd PUC) are shown in Table 1.

The overall 64 switching states can then be obtained by listing every combination of the two individual converters' states. The following definitions should be observed:

$$S_i = \bar{S}_{ic} = \begin{cases} 1 & \text{if } S_i \text{ is ON} \\ 0 & \text{if } S_i \text{is OFF} \end{cases} \qquad i = 1, 2, 3, 4, 5, 6 \quad (1)$$

where S_i ans S_{ic} are pairs of complementary switches that are never ON simultaneously in order to avoid short-circuiting the DC source.

B. DETERMINATION OF CAPACITOR VALUES

The selection of capacitor values is influenced by their peak current, their charging and discharging period, and their voltage ripple as expressed in the following equation:

$$C_i = \frac{I_{\text{peak}} \times \Delta t_{ci}}{V_{\text{ripple}}}, \quad i = 1, 2, 3 \quad (2)$$

where I_{peak} is load current peak value, V_{ripple} is desired capacitor voltage ripple and Δt_{ci} is the duration of charge and discharge of i-th capacitor. The values of I_{peak} and V_{ripple} are imposed by the user, but they still depend on Δt_{ci}. Thus, in Fig. 2 the charging and discharging currents of all three capacitors C_1, C_2 and C_3 are depicted over two fundamental cycles. It is observed that the charging and discharging periods of C_1 and C_3 are balanced with about sampling frequency (f_s), whereas the charging and discharging period of C2 is balanced with about 5 times of fundamental frequency ($5\times f_0$). As such, the values of Δt_c of C_1 and C_3 are much smaller than that of C_2 and consequently, considering (2), the selected values of C_1 and C_3 can be considerably smaller than the value of C_2. More specifically, the capacitor values utilized in this work are $C_1 = 500\,\mu$F, $C_2 = 1500\,\mu$F and $C_3 = 500\,\mu$F.

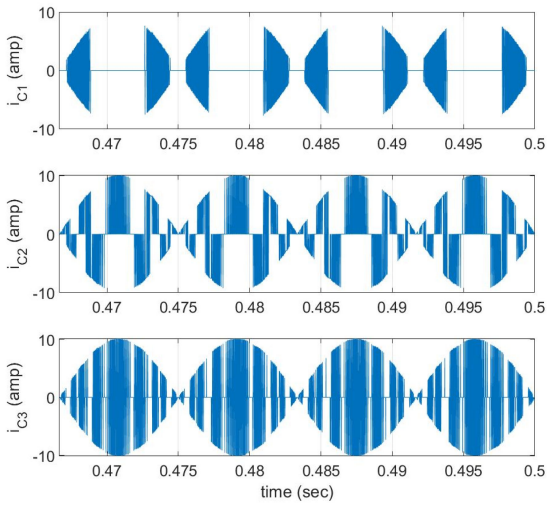

FIGURE 2. Charging and discharging currents of all three capacitors of the H-PUC converter during two fundamental cycles.

TABLE 2. Comparison of the Proposed 23 L H-PUC Converter with other Presented Converters in the Literature in Terms of the Number of Components

MLI Type	HF Switches	LF Switches	Diodes	Caps.	DC Sources
23L-CHB	44	-	-	-	11
21L Q-HNPC [31]	4	10	4	3	2
23L-PUC	22	2	-	10	1
23L-ANPC	22	4	-	12	1
25L H-ANPC [14]	8	6	-	3	3
Proposed 23L-H-PUC	8	4	-	3	1

C. COMPARISON OF THE H-PUC WITH OTHER MLI TOPOLOGIES

The proposed 23-level H-PUC converter is compared to other MLI converters in Table 2. The table lists the number of DC sources, capacitors, diodes, high frequency (HF) switches and low frequency (LF) switches for the CHB, Q-HNPC, PUC, ANPC and H-ANPC converters with similar numbers of voltage output levels.

As such, Table 2 demonstrates that the proposed H-PUC is able to considerably reduce the number of HF and LF switches when compared to other topologies, even decreasing the number of LF switches by two with respect to the 25-level H-ANPC [14] and by four with respect to the 21-level Q-HNPC [31]. In addition, the H-PUC requires only one DC source, three capacitors and no clamped diodes. Hence, the H-PUC inverter is capable of attaining a high number of output voltage levels with a reduced number of components.

III. THE PROPOSED FINITE CONTROL SET MODEL PREDICTIVE CONTROLLER (FCS-MPC)

A. MATHEMATICAL MODELLING OF THE INVERTER

It is necessary to define a mathematical model of the converter in order to use a model predictive controller effectively. This

TABLE 3. Simplified Switching States and Capacitor Charging States of 1st and 2nd PUC for MPC

1st PUC States				
State	**Sa**	**Sb**	**C1**	V_{1stPUC}
1	0	0	–	0
2	0	-1	↓	$-V_{c1}$
3	-1	1	↑	$V_{c1}-V_{dc}$
4	-1	0	–	$-V_{dc}$
5	1	0	–	V_{dc}
6	1	-1	↑	$V_{dc}-V_{c1}$
7	0	1	↓	V_{c1}
8	0	0	–	0
2nd PUC States				
State	**Sc**	**Sd**	**C2**	**C3**	V_{2ndPUC}
1	0	0	–	–	0
2	0	-1	–	↓	$-V_{c3}$
3	-1	1	↓	↑	$V_{c3}-V_{c2}$
4	-1	0	↑	–	$-V_{c2}$
5	1	0	↑	–	V_{c2}
6	1	-1	↓	↑	$V_{c2}-V_{c3}$
7	0	1	–	↓	V_{c3}
8	0	0	–	–	0

is because the basis of MPC is the prediction of the future state of the converter model [33]. Hence, a simple and discretized converter model based on the Forward Euler approximation is developed and presented in this section.

The first equation that can be defined is the overall inverter AC output voltage in the time domain as:

$$V_{inv}(t) = V_{1stPUC}(t) + V_{2ndPUC}(t). \tag{3}$$

Because the objective of the model predictive controller is to select an appropriate switching state, it is more useful to express V_{inv} as a function of the individual switches' states (S_1 to S_6). This approach was used in [33] and is reproduced here. Indeed, by examining the relationships between the states of the switches S_i and the converter output voltage, which is defined by the sum of V_{1stPUC} and V_{2ndPUC}, two switching functions can then be defined:

$$V_{1stPUC}(t) = (S_1 - S_2)V_{dc}(t) + (S_2 - S_3)V_{c1}(t) \tag{4}$$

$$V_{2ndPUC}(t) = (S_4 - S_5)V_{c2}(t) + (S_5 - S_6)V_{c3}(t). \tag{5}$$

These equations can be further simplified by introducing four new switching variables constructed by combining each two consecutive switching functions, namely:

$$S_a = S_1 - S_2 \tag{6}$$

$$S_b = S_2 - S_3 \tag{7}$$

$$S_c = S_4 - S_5 \tag{8}$$

$$S_d = S_5 - S_6. \tag{9}$$

Therefore, new simplified switching states are obtained based on the newly introduced intermediate switching states, as can be shown in Table 3. These new switching variables are used in the MPC to generate the appropriate output voltage level of the converter.

With the new variables defined in (6) to (9), it is then possible to combine equations (3) to (9) to write the following discrete expression

$$V_{inv}(k) = S_aV_{dc}(k) + S_bV_{c1}(k) + S_cV_{c2}(k) + S_dV_{c3}(k) \tag{10}$$

for the inverter output voltage, where $k = 0, 1, 2, 3\ldots$ is the discrete index chosen to denote the value of a variable at a given computation time step. One can observe that the output voltage is a combination of the switching variables that multiply each of the V_{dc} and the three capacitor voltages V_{c1}, V_{c2} and V_{c3}. Subsequently, the equations of the C_1, C_2, and C_3 capacitors currents as functions of the new switching variables along with the grid current $i_s(t)$ can be written as

$$i_1(t) = C_1\frac{dV_{c1}(t)}{dt} = -S_bi_s(t) \tag{11}$$

$$i_2(t) = C_2\frac{dV_{c2}(t)}{dt} = -S_ci_s(t) \tag{12}$$

$$i_3(t) = C_3\frac{dV_{c3}(t)}{dt} = -S_di_s(t). \tag{13}$$

Next, the derivative terms in equations (11) to (13) can be discretized by using the Forward Euler approximation

$$\frac{dV_{c1}(t)}{dt} = \frac{V_{c1}(k+1) - V_{c1}(k)}{T_s} \tag{14}$$

$$\frac{dV_{c2}(t)}{dt} = \frac{V_{c2}(k+1) - V_{c2}(k)}{T_s} \tag{15}$$

$$\frac{dV_{c3}(t)}{dt} = \frac{V_{c3}(k+1) - V_{c3}(k)}{T_s} \tag{16}$$

where T_s is the sampling time. Finally, by replacing (14), (15) and (16) into (11), (12) and (13), respectively, the equations for the predicted future values of the capacitor voltages as functions of the switching variables are obtained as:

$$V_{c1}(k+1) = V_{c1}(k) - \frac{T_sS_b}{C_1}i_s(k) \tag{17}$$

$$V_{c2}(k+1) = V_{c2}(k) - \frac{T_sS_c}{C_2}i_s(k) \tag{18}$$

$$V_{c3}(k+1) = V_{c3}(k) - \frac{T_sS_d}{C_3}i_s(k). \tag{19}$$

In the time domain, the inverter voltage as a function of grid current and grid voltage $V_s(t)$ is expressed as:

$$V_{inv}(t) = R_si_s(t) + L_s\frac{di_s(t)}{dt} + V_s(t). \tag{20}$$

The derivative term can be discretized by employing the Forward Euler approximation

$$\frac{di_s(t)}{dt} = \frac{i_s(k+1) - i_s(k)}{T_s} \tag{21}$$

and the equation for the predicted future value of the grid current is derived by combining (20) and (21)

$$i_s(k+1) = i_s(k) + \frac{T_s}{L_s}(V_{inv}(k) - V_s(k) - R_si_s(k)). \tag{22}$$

The next step in the MPC design is to define the control objectives.

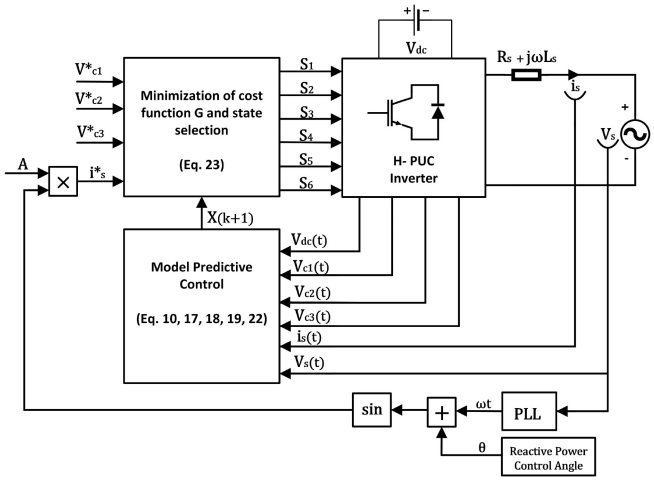

FIGURE 3. The Schematic Diagram of the Proposed FCS-MPC for the H-PUC Inverter.

B. CONTROL OBJECTIVES AND IMPLEMENTATION OF THE MPC

The proper operation of the proposed H-PUC converter depends on the regulation of the DC capacitor voltages and on the synchronization of the injected current with the grid voltage. Thus, there are four control objectives for the MPC: regulation of voltages V_{c1}, V_{c2}, V_{c3} and the synchronization of grid current i_s. Thus, the MPC cost function G takes the following form:

$$G(k) = k(i_s(k+1) - i_s^*)^2 + \frac{k}{5}(V_{c1}(k+1) - V_{c1}^*)^2 + \frac{k}{3}(V_{c2}(k+1) - V_{c2}^*)^2 + \frac{k}{2}(V_{c3}(k+1) - V_{c3}^*)^2 \tag{23}$$

where k is used as a weighted factor to decouple one objective from the other, and the variables denoted by a star (*) are the reference values. In this work, the weights attributed to the control of the three capacitor voltages are normalized with respect to the current gain k, and the specific gain ratios in (23) are determined by iteration to obtain satisfactory performance.

The schematic diagram of the proposed FCS-MPC method is shown in Fig. 3 along with a flowchart of the process in Fig. 4. At every time step, the MPC measures the present values of $V_{dc}, V_{c1}, V_{c2}, V_{c3}, i_s$ and V_s and uses them to compute the predicted future values based on equations (10), (17), (18), (19) and (22). These future values are represented by the vector $X(k+1)$ in Fig. 3. The controller computes the aforementioned predicted values for all 64 possible states of the switching variables S_a, S_b, S_c, S_d and determines which one of these states results in the minimum value of the cost function G. The selected state is then used to apply the corresponding pulses to the inverter switches' gates and the process is repeated for the next time step.

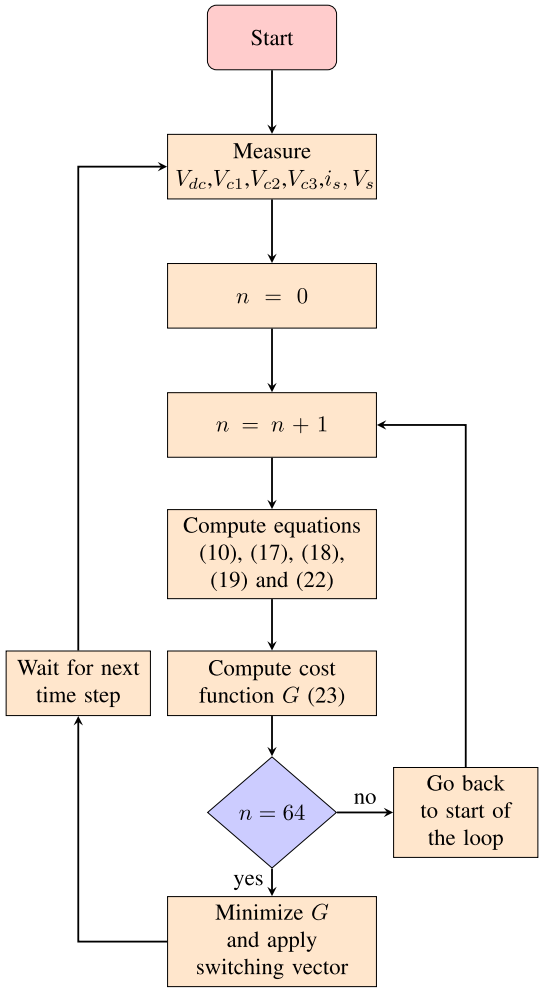

FIGURE 4. Flowchart of the Proposed FCS-MPC Process.

C. REFERENCE VALUES FOR 23 OUTPUT VOLTAGE LEVELS

In order to achieve the desired number of output voltage level, which is 23 in this case, it is important to apply the proper voltage ratio between the source V_{dc} and the DC capacitor voltage V_{c2}. In the H-PUC converter, the following formula can be used to calculate the number of output voltage levels

$$N = M_1 \times M_2 - 2 \tag{24}$$

where N is the number of output voltage levels, M_1 and M_2 are the number of output voltage levels of the first PUC and second PUC respectively, and the subtraction by 2 is for providing enough redundant switching states for voltage balancing of all capacitors. Then, the voltage ratio $\frac{V_{dc}}{V_{c2}}$ should be equal to the number of voltage output levels of the second PUC. In this case, because both converters are 5-level PUC5s, the ration is $M_2 = 5$ or:

$$V_{c2}^* = \frac{V_{dc}}{5}. \tag{25}$$

In (25), V_{dc} is the input DC source voltage. Furthermore, because each of the two converters are operated as 5-level PUC5

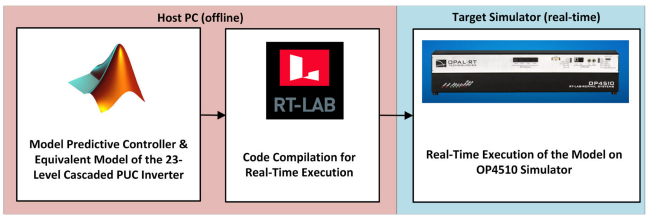

FIGURE 5. Schematic of the Simulation Process with OP4510.

inverters, the auxiliary DC capacitors should be regulated at half the value of the main DC voltage:

$$V_{c1}^{*} = \frac{V_{dc}}{2} \tag{26}$$

$$V_{c3}^{*} = \frac{V_{c2}^{*}}{2} = \frac{V_{dc}}{10}. \tag{27}$$

Moreover, as seen in Fig. 3, the sinusoidal current reference is obtained by measuring the grid voltage angle and generating a synchronized sine wave

$$i_s^{*} = A \times \sin(\omega t) \tag{28}$$

where A is the amplitude of the reference injected current to the grid and ωt is the measured grid voltage angle.

IV. CONVERTER MODELING FOR REAL-TIME SIMULATION ON THE OPAL-RT PLATFORM

A. SOFTWARE-IN-THE-LOOP SIMULATION

In a typical production process, the steps generally consist of some initial research, mathematical modeling, offline simulations and then hardware prototyping. Real-time simulation (RTS) is to be used as an intermediate step before any real hardware is developed. Indeed, real-time simulations offer the possibility of connecting the simulated system to a larger digital plant (e.g. distribution grid). This better flexibility is due to the fact that in RTS, one second of simulation represents one second of the real life system running. In other words, the simulation runs at the same rate as the real system would. This feature also allows for hardware-in-the-loop (HIL) simulations in which hardware components such as controllers can be introduced in the simulation loop. This helps in further reducing the complexity and cost of the production process [3], [35], [36].

Specifically, the type of real-time simulation employed in this work is called software-in-the-loop (SIL) simulation. It gets this name because there is no hardware controller or plant involved in the process, like there would be for HIL. Nonetheless, SIL still results in more true to life behaviour of the simulated system. A schematic of the SIL process is illustrated in Fig. 5. In the case of this paper, both the model predictive controller and the inverter are modeled in Matlab/Simulink, compiled on the RT-LAB software and then simulated in real-time on an OP4510 CPU.

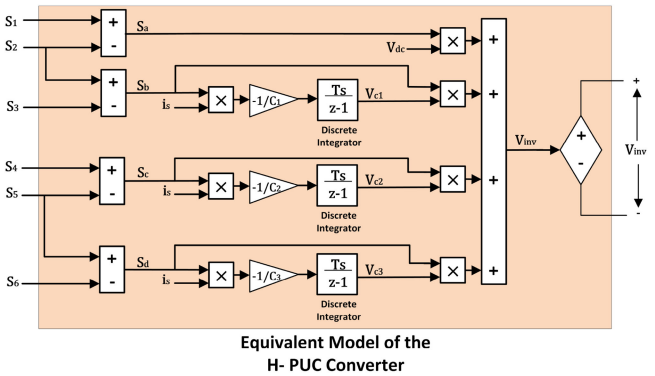

FIGURE 6. Diagram of the Equivalent H-PUC Model.

B. REAL-TIME MODEL OF THE H-PUC INVERTER

The large number of active switches in the proposed inverter makes it difficult to perform CPU-based real-time simulation with a low enough computation time step. A low time step is necessary because the performance of the MPC increases when the time step decreases. For this reason, an equivalent inverter model where the first and second PUC converters are replaced by a controlled voltage source is developed [37]. The diagram in Fig. 6 shows the aforementioned equivalent converter model. By using the switching vector (S_1 to S_6), the current measurement i_s and the value of the DC source V_{dc} as inputs, the inverter output voltage V_{inv} can be accurately reproduced thanks to equations (10), (11), (12) and (13). The rest of the circuit, namely the AC voltage source V_s and the line impedance $R_s + j\omega L_s$ depicted in Fig. 1, are modeled using SimPowerSystems (SPS) components. Finally, the model predictive controller is constructed with a Matlab Function block that stores the vectors of S_a to S_d and S_1 to S_6, and computes equations (10), (17), (18) (19), (22) and (23) and applies the selected switching vector to the equivalent converter model as shown in Fig. 6.

C. VALIDATION OF THE EQUIVALENT REAL-TIME MODEL OF THE H-PUC INVERTER

The equivalent voltage source model of the H-PUC inverter presented in the previous subsection is validated through offline simulations in Simulink. The circuit presented in Fig. 1 is constructed in two versions: one using IGBT power switches and capacitors from the SPS library and another one using the voltage source equivalent model. The simulation parameters for both versions are the same and are outlined in Table 4. In order to validate the accuracy of the proposed equivalent model, the waveforms of the measurements of both circuit versions are superimposed in the subsequent Fig. 7, Fig. 8 and Fig. 9.

Firstly, the system transient response is simulated. The results for the output voltage V_{inv} and the grid current i_s are shown in Fig. 7 while the three capacitor voltages V_{c1}, V_{c2}, V_{c3} are illustrated in Fig. 8. It can be observed from Fig. 7 and Fig. 8 that the equivalent model of the converter is able to

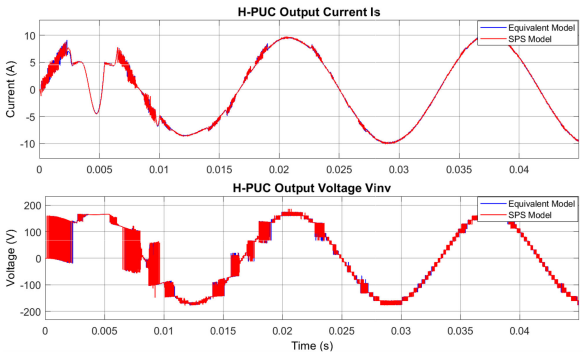

FIGURE 7. Output voltage and grid current transient response: comparison of SPS and equivalent model.

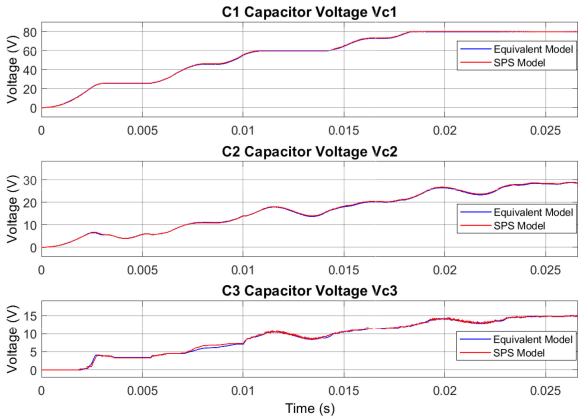

FIGURE 8. Capacitor voltages transient response: comparison of SPS and equivalent model.

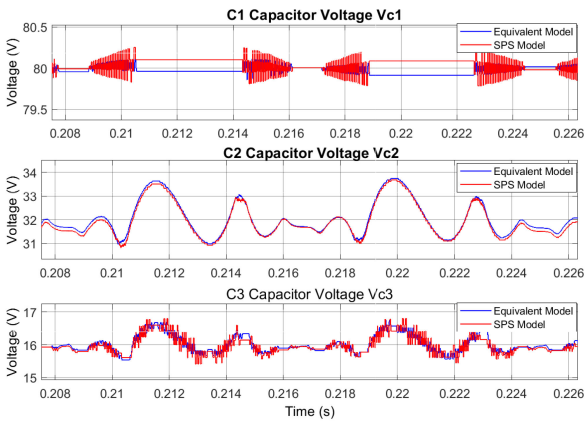

FIGURE 9. Capacitor voltages ripple: comparison of SPS and equivalent model.

closely match the behaviour of the circuit made from SPS power switches.

Secondly, a closer inspection of the capacitor voltages in steady-sate is performed as displayed in Fig. 9. These measurements demonstrate that even the small voltage ripples of the DC capacitors are well reproduced by the equivalent model. Hence, the equivalent H-PUC model is used to obtain real-time simulation results in the next section.

TABLE 4. Simulation Parameters

Parameter	Value
Grid Frequency	$f = 60Hz$
DC Source Voltage	$V_{dc} = 160V$
First DC Capacitor	$C_1 = 500\mu F$
Second DC Capacitor	$C_2 = 1500\mu F$
Third DC Capacitor	$C_3 = 500\mu F$
Grid Link Inductance	$L_s = 500\mu H$
Grid Link Resistance	$R_s = 0.1\Omega$
Grid Voltage	$V_s = 120Vrms$
Cost Function Gain	$k = 10$
Real-Time Simulation Time Step	$T_s = 10\mu s$

V. REAL-TIME SIMULATION RESULTS

The proposed 23-level grid-connected H-PUC inverter and associated model predictive controller have been implemented in OPAL-RT OP4510 real-time simulator and the RT-LAB real-time simulation software, which is based on the Matlab/Simulink platform. In addition to steady-state and transient results, a step change in the current amplitude reference is applied to demonstrate the dynamic performance of the system in tracking the reference injected current to the grid. Reactive power and voltage sag tests are also performed to further demonstrate the converter and controller performance. The parameters used for the simulation are listed in Table 4.

With the chosen 160 V DC source voltage, the DC capacitor voltages should be regulated at $V_{c1}^* = 80\,\text{V}$, $V_{c2}^* = 32\,\text{V}$ and $V_{c3}^* = 16\,\text{V}$ according to (25) to (27).

The steady-state waveforms for the inverter output voltage V_{inv}, the first and second PUC output voltages V_{1stPUC}, V_{2ndPUC} and the grid current i_s are depicted in Fig. 10 for a current reference of 10 A. The 23 output voltage levels are easily identified in the V_{inv} waveform. Furthermore, the behaviours of the two PUCs can be observed individually. In fact, the first PUC operates as a high voltage, low frequency five-level converter with high efficiency, whereas the second PUC operates at higher switching frequency and lower DC voltages to generate extra minor voltage levels between provided major voltage levels of the first PUC sub-module that are needed to achieve the required overall 23 voltage levels. In addition, the injected current to the grid is almost sinusoidal, which implies that its harmonic content is minimal. Another interesting feature of this topology is that the high frequency switches withstand much lower DC bus voltage while conducting the same load current, which leads to less power loss in the power switches and higher overall efficiency of the proposed H-PUC inverter.

The transient response of the three DC capacitors is also measured. In Fig. 11, the capacitor voltage waveforms form startup until they reach steady-state are displayed. The measurements confirm the accuracy of the controller and they also show the quick transient period of the capacitor voltages. Indeed, all three voltages reach steady-state in under 0.06 s.

The six gating signals S_1 to S_6 are also measured over one fundamental 60 Hz cycle once the system has reached steady-state. The results confirm the behaviour seen in Fig. 10.

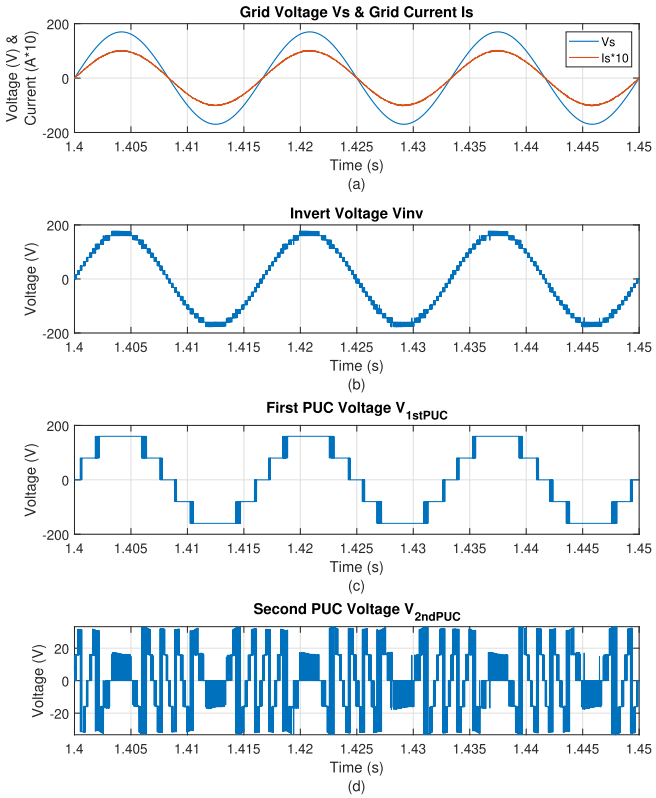

FIGURE 10. Real-time simulation results of the proposed H-PUC converter. (a) Grid voltage and current. (b) The output voltage of the proposed 23-level H-PUC inverter (c) The first PUC sub-module output voltage. (d) The second PUC sub-module output voltage.

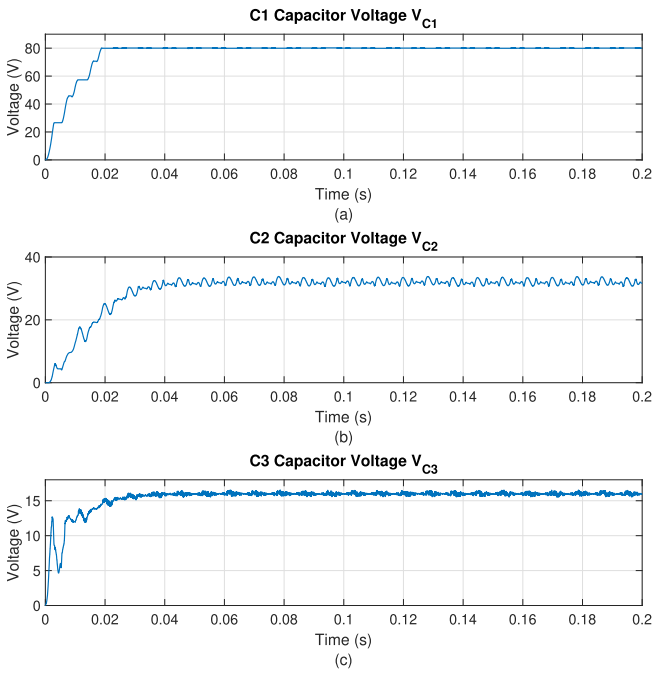

FIGURE 11. Transient response of (a) C1 capacitor voltage. (b) C2 capacitor voltage. (c) C3 capacitor voltage.

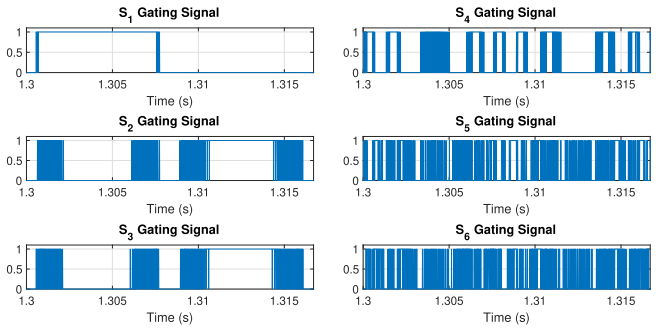

FIGURE 12. Gating Signals for Switches S1 to S6 Over a Steady-State 60 Hz Cycle.

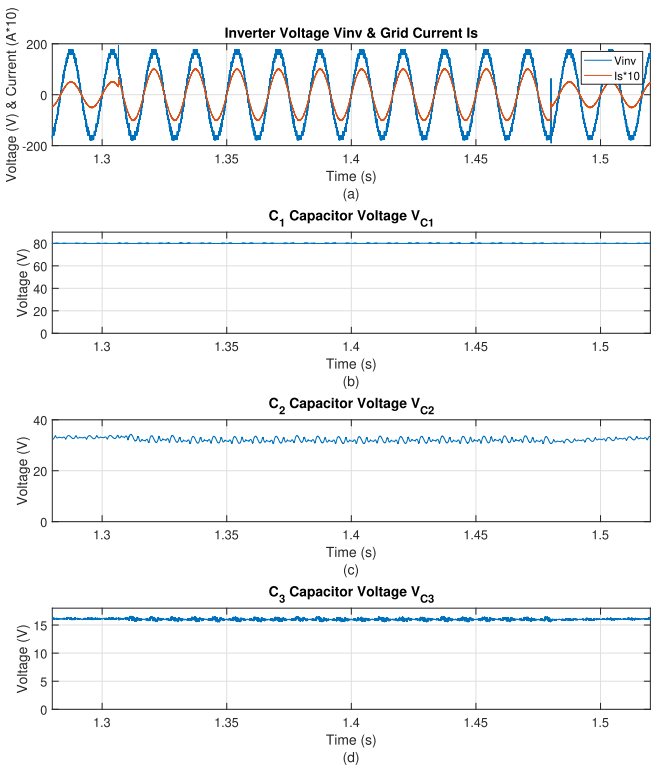

FIGURE 13. Response for the (a) inverter voltage and grid current, (b) C1 voltage, (c) C2 voltage, and (d) C3 voltage during a step current change.

Indeed, Fig. 12 indicates that the first PUC's switches operate at a much lower frequency than the second one, with S_1 switching at fundamental frequency. This behaviour results in overall lower switching losses since the higher DC voltages of the first PUC are switched at low frequencies and only the smaller DC voltages of the second PUC converter are switched at high frequencies.

The dynamic performance of the inverter is evaluated by applying a current amplitude reference change from 5 A to 10 A and thereafter back to 5 A. Fig. 13 shows the response of the three capacitor voltages, the inverter voltage and the grid current during the transients. The results demonstrate that the inverter voltage and DC voltages show little to no disturbance

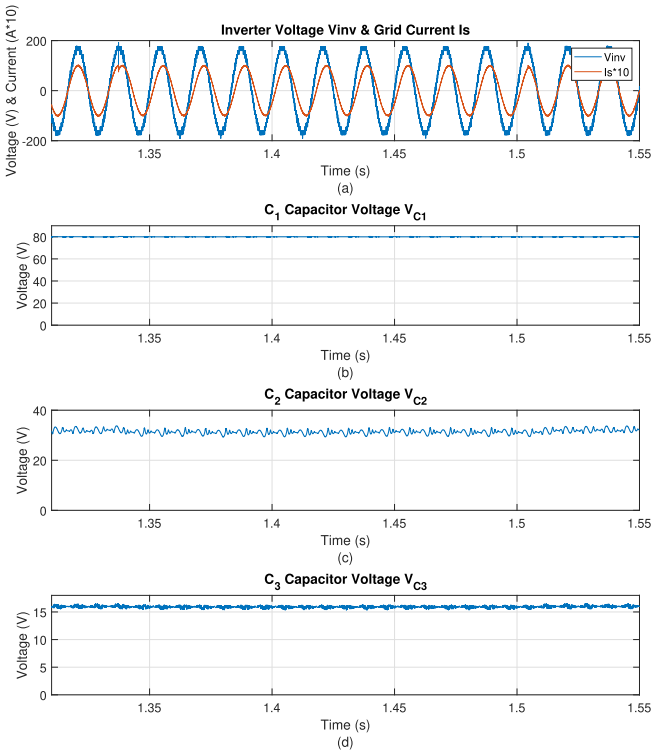

FIGURE 14. Response for the (a) inverter voltage and grid current, (b) C1 voltage, (c) C2 voltage, and (d) C3 voltage during a current phase change.

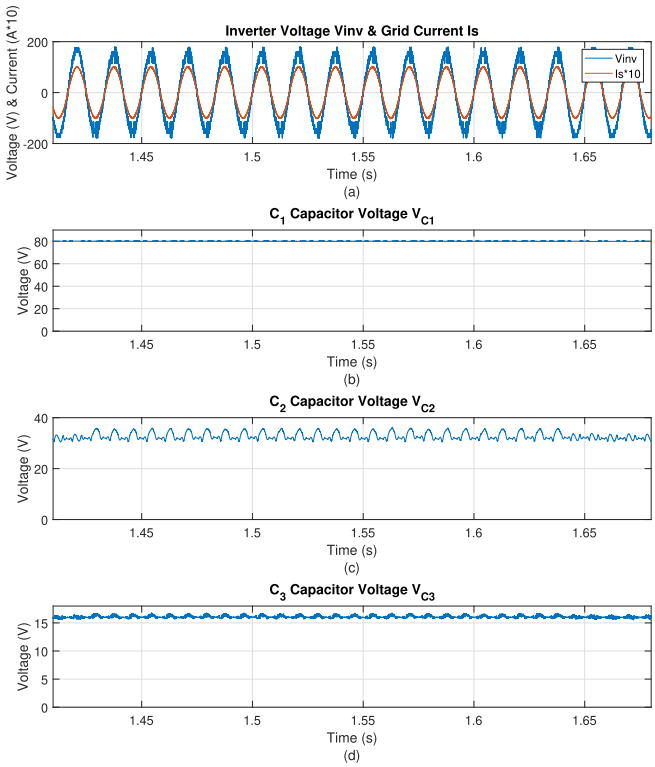

FIGURE 15. Response for the (a) inverter voltage and grid current, (b) C1 voltage, (c) C2 voltage, and (d) C3 voltage during a voltage sag test.

in response to the step change in current amplitude. The system is able to maintain constant voltage operation.

The converter's capacity to inject reactive power into the grid is also tested. This is done by adding an offset angle to the one measured by the PLL in Fig. 3. Indeed, the results in Fig. 14 are obtained when the angle of the reference current is shifted by 30° at 1.34 s, and subsequently brought back to zero at 1.51 s. The measurements show that the controlled variables respond well to the change in current angle. In fact, the only noticeable disturbance is in V_{c2}, which seems to decrease slightly below its target value. Nonetheless, the other DC capacitor voltages show almost no disturbance.

A voltage sag test is also done to illustrate the parameter sensitivity of the converter and controller. A simulation is run in which the grid voltage V_s amplitude is decreased by 10% at 1.42 s and then increased back to nominal value at 1.64 s. The results of this test are seen in Fig. 15. During the voltage sag, the DC capacitor voltages remain around their reference values, but they also start oscillating considerably and this is visible in the V_{inv} waveform. Despite this, the grid current is able to maintain a smooth sinusoidal shape.

Finally, the harmonic spectra and THD values for the inverter voltage and grid current are shown in Fig. 16 and Fig. 17 for a current reference of 10 A. The analyses show a THD of 4.38% for the inverter output voltage and a harmonic spectrum that seems relatively spread out. As for the current, the THD is only 1.35% with the highest individual harmonic

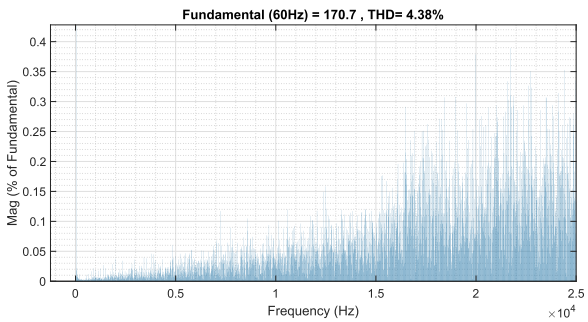

FIGURE 16. Inverter Voltage (Vinv) FFT Analysis.

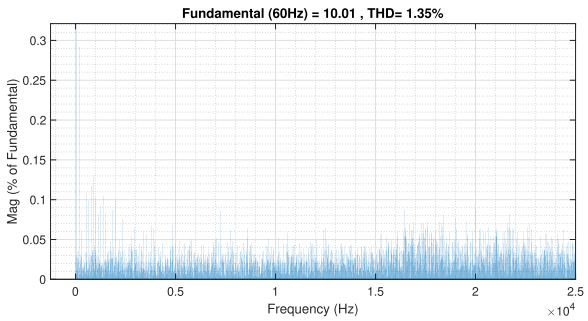

FIGURE 17. Grid Current (Is) FFT Analysis.

being the third order at 0.29% of the fundamental. This low current THD value is achieved despite the low value of the grid inductance (500 μH) thanks to the high number of output voltage levels.

Furthermore, to evaluate the conduction and switching losses of the proposed H-PUC converter, the conduction and switching loss models of C3M0120090D MOSFET has been developed in MATLAB/Simulink platform. Then, based on the switch loss model, the power loss model of the proposed H-PUC converter has been developed and the efficiency of the proposed H-PUC converter has been evaluated. The total efficiency of the proposed H-PUC converter operating at 120 VAC, 850 W, and sampling time of 10 μs is calculated as 93.56%.

Thus, the real-time simulation results demonstrated in this section confirm the effectiveness of the proposed model predictive controller in generating the desired number of output voltage levels in a cascaded PUC converter with a single DC source. The MPC also simplifies the controller design process since it does not require the use of a modulation technique. Moreover, the controller is capable of accurately tracking the reference DC capacitor voltages and grid current references even during step changes in current. Meanwhile, these results are obtained with minimized switching losses due to the hybrid inverter configuration in which higher DC voltages are switched at lower, close to fundamental frequencies.

VI. CONCLUSION

The single DC source 23-level H-PUC inverter with reduced number of components and its associated FCS-MPC were proposed in this paper. It is comprised of only one DC source, twelve power switches, and three capacitors to provide 23-level output voltage. The proposed H-PUC inverter is formed by cascade connection of two high voltage low frequency and low voltage high frequency PUC5 sub-modules which leads to less power losses and higher efficiency of the proposed H-PUC converter. The DC source of the second PUC5 sub-module was replaced by capacitor, then the single dc source hybrid multilevel inverter was achieved. Moreover, the proposed FCS-MPC method was applied to the H-PUC inverter to generate 23-level staircase output voltage with low THD and to regulate voltages of three capacitors to their desired values simultaneously. The real-time model of the proposed grid-connected H-PUC inverter and its associated FCS-MPC were implemented in OPAL-RT OP4510 real-time simulator. The provided real-time implementation results verified the feasibility and viability as well as steady-state and dynamic performance of the proposed grid-connected H-PUC inverter and its suggested FCS-MPC.

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