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Analysis and Design of a Class E Type High Frequency DC–DC Converter Based on Resonant Driving Circuit

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ABSTRACT In this paper, a class E type high frequency DC–DC converter is proposed. The detailed analysis and parameter optimal design method are depicted in this paper. Based on optimal parameters, the switch can operate in ZVS condition. Also, to reduce the driving losses, a multistage resonant driving circuit is adopted and analyzed in this paper, which can utilize the energy stored in the switch input capacitance. The ON/OFF control method is adopted to regulate output voltage and the enable signal frequency is 340 kHz. From the output side, the circuit can be seen as operating at enable signal frequency with high sampling frequency. A 20 MHz prototype is built in this paper, which verifies the feasibility of high frequency converter and control method.

INDEX TERMS High frequency, DC–DC converter, resonant driving circuit, Class E.

I. INTRODUCTION

In switching mode power system (SMPS), with the demand of high power density, the system operating frequency keeps increasing. High operating frequency can greatly reduce the volume of inductors and capacitors, meanwhile the dynamic characteristics can be improved [1]–[3]. However, many problems come with the high operating frequency, especially when it is above tens of MHz [4]–[6]. Here the conventional PWM converter with step-up/down function is taken as an example. Firstly, the circuit topology, such as SEPIC, has a bulk input inductor by which the input can be seen as a constant current source. Also, the operating modes cause hard switching of the switch and diode. As switching frequency increasing, the loss of the switches and magnetic components will increase quickly and circuit efficiency will be reduced [7]–[9].

Secondly in terms of control method, due to the low operating frequency of conventional converter, the output voltage can be regulated by pulse width modulation (PWM) [10], [11]. Another method is the pulse frequency modulation (PFM) [12], [13]. However, the above two control methods are not suitable for high frequency conditions such as tens of MHz. The switching period of the power converter is around hundreds of ns with the operating frequency above the MHz, which is very difficult to achieve PWM or PFM control [14], [15].

Thirdly for the driving circuit, there are many difficulties for high frequency power converters. In square wave driving method, the energy stored in the switch input capacitance is completely dissipated every cycle, which increases the driving circuit loss and reduces the efficiency significantly [16]–[19]. Especially in low power converters, driving loss greatly affects system efficiency. Thus the resonant driving circuit is developed in recent years, which uses the parasitic capacitance to resonate with an inductor, which helps to reduce the loss and improve system efficiency [20]–[23]. The simplest resonant driving circuit is to add a resonant inductor into the driving loop. However, the total driving current flows through resonant inductor and equivalent resistor of driving circuit, which causes corresponding loss.

To solve the aforementioned problems, a high frequency DC–DC converter with resonant driving circuit is proposed in this paper. Fig. 1 shows the power stage of the proposed high

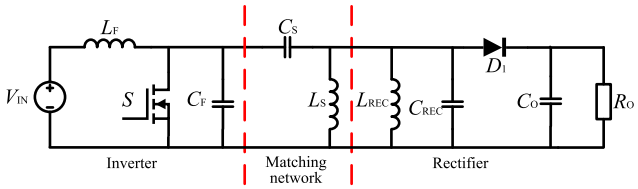


FIGURE 1. Proposed high frequency class E type converter.

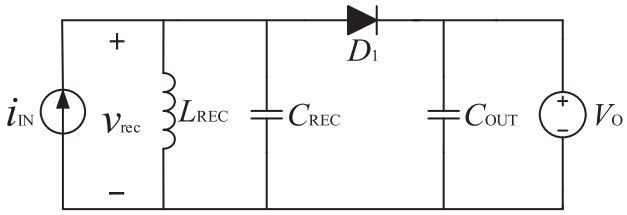


FIGURE 2. The circuit of high frequency resonant rectifier.

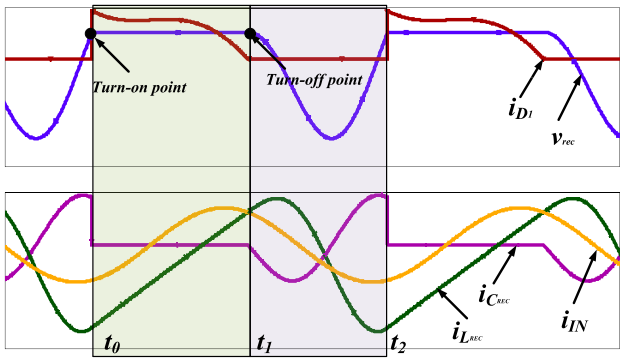


FIGURE 3. The operating mode of high frequency resonant rectifier.

frequency converter. The input part of the proposed circuit can be seen as a Class E inverter and the output part can be seen as a Class E rectifier. In the convention Class E inverter, the input inductor is a choke inductor. The input current needs to be seen as constant, thus, the inductor value is quite large. However, in the proposed circuit, the inductor L_F is no more a choke one, it is a resonant inductor with small value. The resonant inductor L_F resonates with the resonant capacitor C_F to create the soft-switching of the switch. Thus, the value the proposed converter can be greatly reduced and the volume can be reduced to quarter to one tenth of the choke one. With small value inductor, the copper loss can be reduced. Also, the aircore inductor can be adopted and the magnetic core loss will be avoided.

Meanwhile, the close-loop control is realized based on ON/OFF control method [24], [25], whose main idea is to use the low frequency signal as the outer loop, by changing the duty cycle of low frequency signal, the effective operating duty cycle of high frequency signal can be adjusted. Also, a resonant driving circuit with shunt branch is adopted in this paper, which can further reduce the driving loss of high frequency converters.

In this paper, a detailed analysis and design method of the proposed high frequency converter is discussed. In Section II, the operating principle and design method of the high frequency converter are described, and the driving circuit and control method are presented in Section III. A prototype is built and the experimental results are shown in Section IV. The conclusion is finally given in Section V.

II. WORKING PRINCIPLE OF THE PROPOSED CONVERTER

As shown in Fig. 1, the Class E type high frequency converter contains three subsystems: a resonant inverter, a matching network and a resonant rectifier, the design procedure is that designed each subsystem separately from the back to front, then coupling the three subsystems, finally retuning as necessary to account for nonlinear interactions with the three subsystems. The design steps of each subsystem will be discussed in the following section.

A. RECTIFIER STAGE

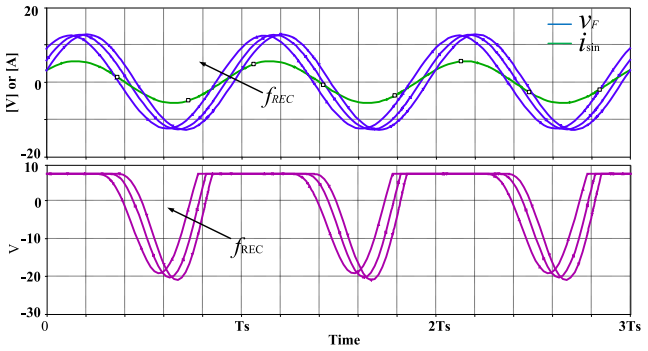
The design procedure of high frequency DC–DC converter starts with the resonant rectifier. The rectifier is adjusted in the specified output power and voltage to exhibit certain characteristics and behaviors. Once the equivalent impedance at the operating frequency is determined, the rectifier can be replaced with this impedance to a resonant inverter. The necessary impedance of the inverter stage can be calculated by V^2/P. Here V represents the amplitude of the inverter output voltage and P represents the power. In most conditions, these two impedances are not the same with each other.

Fig. 2 is the schematic diagram of the rectifier circuit which is driven by sinusoidal current source at the switching frequency, and it utilizes a resonant tank comprising a resonant inductor L_{REC} which provides a dc path for the output current and a resonant capacitance C_{REC} including the parasitic capacitance of the diode. The output is including the parasitic capacitance of the diode. The output is replaced by a constant voltage source V_O, which is equal to the constant voltage output. Each cycle of the rectifier can be divided into two modes, the mode analysis of the converter is shown as follows and the main waveforms are shown in Fig. 3.

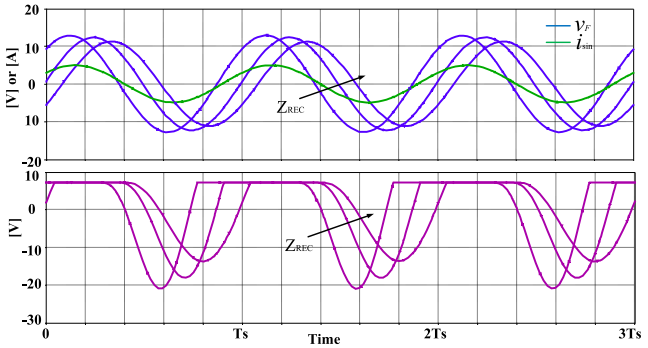
Mode 1 ($t_0 \sim t_1$): at time t_0, the voltage across the inductor L_{REC} rises to V_O, the diode D_1 turns on, and the current in the capacitor C_{REC} changes rapidly to the diode. The voltage across the inductor equals to the output voltage, thus, the inductor current i_{Lrec} keeps increasing. This mode ends at time t_1.

Mode 2 ($t_1 \sim t_2$): At time t_1, the inductor current reaches the same value of input current i_{IN}. So the diode current i_{D1} drops to zero and diode turns off, the capacitor C_{REC} begins to be resonant with the inductor L_{REC}. Until v_{rec} equals to V_O, diode D_1 turns on again and new cycle begins.

The design procedure of a rectifier starts with the sinusoidal drive current source. According to the rated output power and load, the approximate magnitude of the



(a) The waveforms of input voltage and current with different center frequency



(b) The waveforms of input voltage and current with different characteristics impedance

FIGURE 4. The current and voltage waveforms of resonant rectifier.

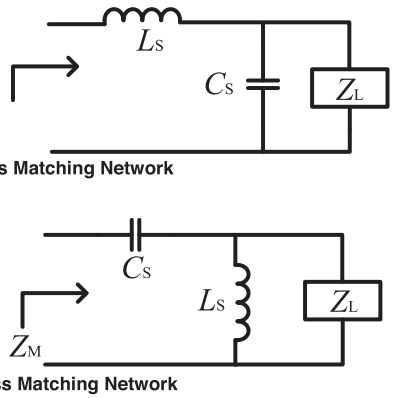
input current source I_{in} can be determined whose frequency is switching frequency. By changing the characteristic impedance $Z_{REC} = \sqrt{L_{REC}/C_{REC}}$ or the center frequency $f_{REC} = 1/2\pi\sqrt{L_{REC}C_{REC}}$ to determine whether the rectifier circuit is resistive.

Fig. 4(a) is the simulating waveforms of sweeping f_{REC} while keeping Z_{REC} constant, the phase angle between the fundamental voltage v_F and the input current i_{IN} changes corresponding. As keeping f_{REC} constant, sweeping f_{REC} not only changes the amplitude of the input fundamental voltage v_F, but also changes the phase angle between v_F and i_{IN}, as shown in Fig. 4(b). So the inductance and the capacitance coupling of the topology is still existing. A lot of parameter scanning is needed in parameter design to achieve resistive input characteristics.

B. MATCHING NETWORK

The matching network is a subsystem which connects the inverter and rectifier circuit, to reduce the equivalent impedance of rectifier circuit. Fig. 5 shows two examples of matching network, which has its own resonant frequency which is different from the switching frequency and it also has a great influence on the overall performance of the circuit.

Matching network has a great relationship with its own structure and working characteristics. The design purpose



(a) Low Pass Matching Network

(b) High Pass Matching Network

FIGURE 5. The diagram of high pass and low pass matching networks.

of matching network is to provide a particular impedance transformation rate at certain frequency. Since the matching network is composed of nonlinear elements, so when a matching network is selected, its impedance conversion rates often change with the resonant frequency varies. When the matching network has more than two nonlinear components, the overall circuit will become complex, increasing the difficulty of designing. Thus the high pass matching network of Fig. 5(b) is chosen and the parameters of the matching network are calculated as follows:

The equivalent impedance Z_M of the matching network can be calculated as follows:

$$Z_M = \frac{s^2 L_S C_S Z_L + s L_S + Z_L}{s^2 L_S C_S + s C_S Z_L} \tag{1}$$

where Z_L is the equivalent impedance of rectifier, Substituting s by $j\omega$ in the equation (1), where ω represents the angle switching frequency of the converter, and the equation (2) and (3) can be obtained.

$$Z_M = \frac{-\omega^2 L_S C_S Z_L + Z_L + j\omega L_S}{-\omega^2 L_S C_S + j\omega C_S Z_L} \tag{2}$$

The matching network is designed to achieve a resistance to resistance transformation, thus, the real part ratio between numerator and denominator should be the same as imaginary part ratio between numerator and denominator, the expression can be represented by (3).

$$Z_M = \frac{-\omega^2 L_S C_S Z_L + Z_L}{-\omega^2 L_S C_S} = \frac{L_S}{C_S Z_L} \tag{3}$$

So the inductance and capacitance value is calculated as follows:

$$L_S = \frac{Z_L}{\omega}\sqrt{\frac{Z_M}{Z_L - Z_M}} \tag{4}$$

$$C_S = \frac{1}{\omega\sqrt{Z_M\,(Z_L - Z_M)}} \tag{5}$$

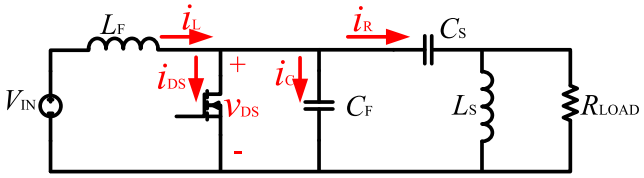


FIGURE 6. The equivalent circuit of proposed resonant converter.

C. INVERTER STAGE

Based on the design of rectifier circuit and matching network, the inverter circuit can be designed, the topology is shown in Fig. 6, where R_{LOAD} is equivalent resistance of rectifier circuit. This resonant inverter topology is similar to the Class E topology, but it is quite different. The main difference is that the input inductance is replaced by a small resonant inductance and the parasitic capacitance of the switch is absorbed by the external parallel capacitance, participating in the resonance. This small change of the inverter can achieve a faster transient response.

Meanwhile, in order to achieve the ZVS and zero dv/dt of switch, the resonant frequency of L_F and C_F must be carefully designed, which is analyzed in detail as follows. The analysis is based on the following assumptions:

1) Switch duty cycle $D = 0.5$.
2) The output current waveform of inverter is sinusoidal at the switching frequency with high quality factor.
3) The switch and all circuit components are assumed to be ideal.

According to the KCL and KVL principles, the basic equations (6) to (8) can be obtained.

$$i_R(\omega t) = I_R \cos(\omega t + \phi) \tag{6}$$

$$v_{DS}(\omega t) = V_{in} - v_L(\omega t) \tag{7}$$

$$i_L(\omega t) = i_{DS}(\omega t) + i_C(\omega t) + i_R(\omega t) \tag{8}$$

The voltage $v_{DS}(\omega t)$ across switch and its derivative $dv_{DS}(\omega t)/dt$ is designed to be zero when the switch is turned on, and the inductor current $i_L(\omega t)$ is continuous. During the off-state, the equation of drain-source voltage can be expressed as follows.

$$v_{DS}(\omega t) = V_{in} - \omega^2 L_F C_F \frac{d^2 v_{DS}(\omega t)}{d(\omega t)^2} + \omega L_F I_R \sin(\omega t + \phi) \tag{9}$$

A general solution of the (9) is shown in equation (10).

$$v_{DS}(\omega t) = V_{in} + A\sin(\omega t + \phi) + B\sin(\omega_1 t + \phi_1) \tag{10}$$

where $\omega_1 = 1/\sqrt{L_F C_F}$ is the resonant frequency of resonant inductor and capacitor. To achieve ZVS of switch, the equation (11) and (12) should be satisfied.

$$v_{DS}(0) = V_{in} + A\sin(\phi) + B\sin(\phi_1) = 0 \tag{11}$$

$$v_{DS}(\pi) = V_{in} - A\sin(\phi) + B\sin\left(\frac{\omega_1}{\omega}\pi + \phi_1\right) = 0 \tag{12}$$

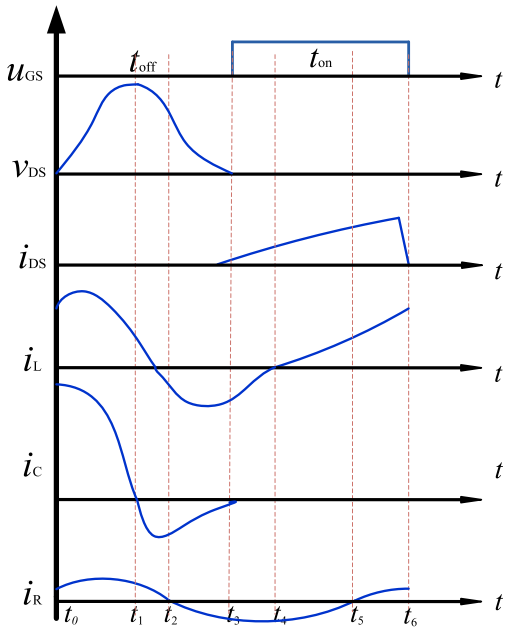


FIGURE 7. The main waveforms of proposed resonant converter.

To simplify the calculation, here assuming $\phi = 0$, then the equation (13) can be obtained.

$$\omega_1 = 2\omega \tag{13}$$

It means to achieve ZVS and zero dv/dt conditions, the resonant frequency must be twice of the operating frequency. Based on above analysis, the relationship between resonant inductor and capacitor can be obtained as follows.

$$L_F = \frac{1}{16\pi^2 f_s^2 C_F} \tag{14}$$

For the equivalent circuit with the inverter and matching network, it has six modes in a working cycle, as shown in Fig. 7, the steady-state analysis of the inverter is described as follows.

Mode 1 (t_0~t_1): at time t_0, the switch is turned off, the current i_{DS} changes rapidly to i_C which instantly increased from 0 to maximum and then decreased. Since the inductor current i_L does not change abruptly, after a short rise and began to decline. According to the Kirchhoff current law, the current i_C drops faster than i_L so that the current i_R shows a trend of increasing first and then decreasing, at the same time t_0, the voltage v_{DS} begins to rise, when i_C drops to 0, the voltage v_{DS} up to the maximum.

Mode 2 (t_1~t_2): from t_1, the capacitor C_F begins to discharge, v_{DS} decreases, i_C reverse increases. When $i_C = i_R$, i_L is reduced to 0 and reverse increase. Since C_F continuous discharge, when the capacitor C_S is fully charged, $i_R = 0$ and begins to reverse reduction.

Mode 3 (t_2~t_3): at time t_2, the capacitor C_S discharges, i_R reverse increases. When the discharge current of the capacitor C_F is reduced to 0, the voltage v_{DS} across the C_F is also

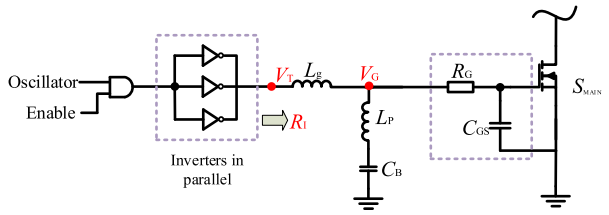


FIGURE 8. **The circuit of resonant driving circuit.**

just reduced to 0. At the moment, the switch is turned on to achieve ZVS. In above three modes, the switch voltage can be represented by (10).

Mode 4 (t_3~t_4): at time t_3, the switch S is turned on, the capacitor C_F is equal to the short circuit, the current i_{DS} begins to increase. Since i_L does not change abruptly, the reverse conduction continues until it falls to 0, at this time $i_{DS} = i_R$, and this mode ends.

Mode 5 (t_4~t_5): from time t_4, the current i_L has been reversed down to 0, the capacitor C_S continuous discharge until i_R reverses drop 0 and $i_L = i_{DS}$ at t_5 moment.

Mode 6 (t_5~t_6): the current i_R reverses to 0 and begins to increase slowly in the positive direction. When t_6 is arrived, the switch S is turned off again, the current i_{DS} rapidly drops to 0 and the new cycle begins.

In this paper, the inverter circuit derived from Class E amplifier so that it also has the same characteristic. The larger the capacitor, the more power is delivered by the inverter section. However, if the value of capacitor is too large, it will cause a large circulation in the circuit, increasing the current stress of the switch and causing extra switching loss. Thus, the value of C_F need to be compromised in the above two aspects. Ideally, not only can the power transfer requirements be met, but the loop current of circuit should be within the acceptable range. According to the transmission power to determine the capacitance C_F, the inductance L_F can be obtained as well. Meanwhile, based on simulation results, the value of C_S and L_s can be tuned to guarantee the switch operating in ZVS condition.

III. ANALYSIS OF RESONANT DRIVING AND CONTROL CIRCUIT

In this paper, a multi-stage resonant driving circuit is adopted as shown in Fig. 8, which contains a bank parallel of CMOS inverters and a resonant tank. The crystal oscillator generates a high-frequency square wave signal which connected with an enable signal in the AND gate. The enable signal will be introduced in the control method part. Then the signal passes through several parallel inverters to enhance the signal drive capability. Through the resonant network, the signal is transferred into a sinusoidal drive signal with a DC offset which equals to half of the square wave high level. In the multi-stage resonant driving circuit, a shunt branch (L_P and C_B) is added in the resonant tank, which can reduce the current flowing through paralleled inverters. The paralleled inverters can be

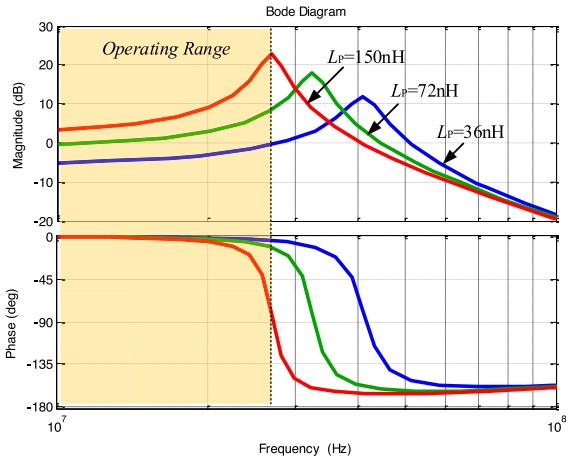


FIGURE 9. **The Bode plot of system driving circuit with different parallel inductor L_P.**

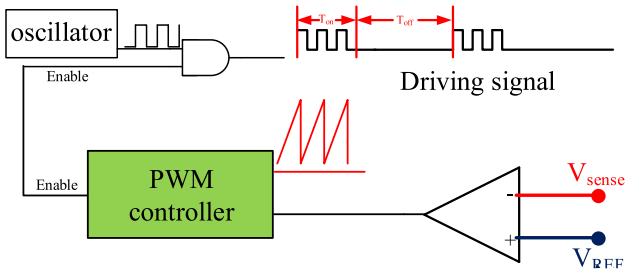


FIGURE 10. **The control diagram of the high frequency converter based on PWM controller.**

equivalent to a resistor R_I, thus small current helps to reduce the corresponding losses.

The turning method of passive components in resonant network is as follows: the input capacitance C_{GS} resonant with the inductor L_g at switching frequency, which can be adopted to determine the approximate value of L_g. The purpose of the shunt branch with L_P and C_B is to reduce energy losses. The branch of L_P and C_B is designed to be inductive at the switching frequency, where C_B is used as a dc block capacitor. The capacitor C_{GS} is in parallel with L_P, which can increase the impedance, comparing with the single gate capacitance condition. Higher gain of transfer function V_G/V_T can also be achieved as equation (15) shown.

When the inductance L_g is determined, the gain of transfer function V_G/V_T depends on the value of L_P. Fig. 9 shows the bode diagram of V_G/V_T with different L_P. The operating range of the driving circuit is expected within the zero phase range, which is highlighted as the shadow background shows. Within this range, as the L_P increases, the amplitude of V_G/V_T increase as well, while the phase is almost constant. Finally, the value of L_P can be calculated with a proper voltage gain for certain switch.

In this paper, the ON/OFF control method is adopted, and the control diagram can be seen as Fig. 10 shown. A low

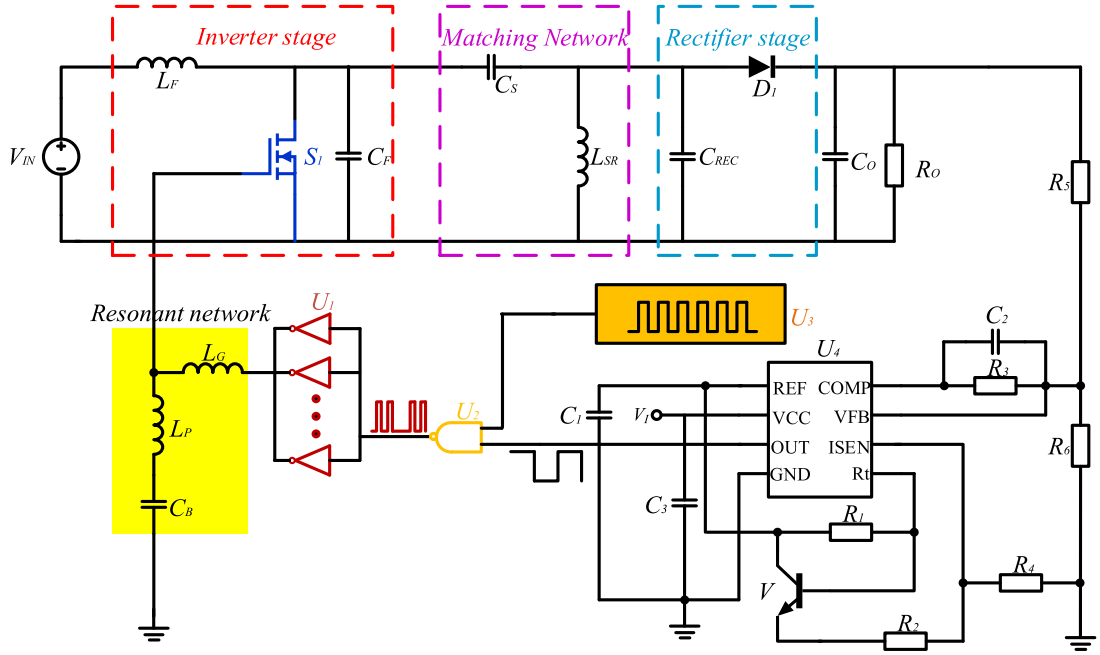


FIGURE 11. The control diagram of the high frequency converter based on PWM controller.

frequency enable signal is generated from a PWM controller, which frequency is constant. The low frequency enable signal and high frequency oscillator signal are two input signals of AND gate. When the output voltage is higher than the reference value, the on time of low frequency PWM signal increases, which can lengthen the equivalent operating time of switch. When the output voltage is lower than the reference value, the on time of low frequency PWM signal decreases. The output voltage ripple can be controlled by setting different PWM frequencies and output capacitance.

$$\frac{V_G}{V_T} = \frac{s^3 L_P R_G + s^2 \frac{L_P}{C_{GS}} + s\frac{R_G}{C_B} + \frac{1}{C_B C_{GS}}}{s^4 L_P L_g + s^3 R_G (L_P + L_g) + s^2 \left(\frac{L_g}{C_{GS}} + \frac{L_g}{C_B} + \frac{L_g}{C_{GS}}\right) + s\frac{R_G}{C_B} + \frac{1}{C_B C_{GS}}} \quad (15)$$

IV. SYSTEM DESIGN AND EXPERIMENTAL RESULTS

Based on above analysis, a 20 MHz high frequency DC–DC converter is built in the laboratory, the circuit is shown in Fig. 11. The input voltage is 10 V, output voltage is 5 V and the output power is 8 W. The prototype is designed for the application of DC module. According to the aforementioned design method, the parameter values in the circuit can be calculated.

Based on simulation result when the rectifier input current and voltage are in the same phase, the value of L_{REC} is 54.8 nH and the value of the resonant capacitor is 134 pF. By reducing the junction capacitance 30 pF of the diode, the discrete capacitor C_{REC} can be chosen around 100 pF. Then, the equivalent resistance of the rectifier stage can be calculated which is about 17 Ω. The required resistance of the inverter stage is about 5 Ω by calculating the desired power. Then according to (4) and (5), the value of L_S can be calculated to be 83 nH and the value of C_S can be calculated to 976 pF. For inverter stage, the value of resonant capacitor is chosen to be 480 pF, then the value of L_F can be calculated to be 33 nH based on (14). The discrete resonant capacitor C_F can be calculated by reducing the 320 pF parasitic output capacitance of the switch, which is around 160 pF. After small tuning by the simulation software, the final parameter values can be determined.

The current and voltage characteristics of circuit elements should be analyzed. For the inductor L_F in the inverter stage, the current linearly increases during the switch on state, the peak current can be expressed as:

$$I_{LF\_peak} = \frac{V_{in}}{L_F} DT \quad (16)$$

For the resonant part during switch off state, the expression is difficult obtained, thus, it is assumed to the symmetric with the rising part, thus, the average current can be estimated as:

$$I_{LF\_avg} = \frac{V_{in}}{L_F} D^2 T \quad (17)$$

For switch, the peak current flowing through it is the same value of peak current of L_F, and the average current value can be calculated as

$$I_{LF\_avg} = \frac{V_{in}}{2L_F} D^2 T \quad (18)$$

For the voltage stress of switch and resonant capacitor C_F, it can be seen from the simulation results which is about 3.5 times of input voltage.

For the rectifier stage, because of resonance, the diode peak current is difficult to calculated. However, the average current

TABLE 1. Main Components of the High Frequency DC–DC Converter

Device label	VALUE/TYPE	Device label	Value/Type
L_F	33nH	R_1	5kΩ
S_1	SI7454	R_2	30kΩ
C_F	180pF	R_3	100kΩ
C_s	1000pF	R_4	20kΩ
C_{REC}	100pF	R_5	13kΩ
D_1	STPS2H100A	R_6	15kΩ
C_O	5uF	C_B	0.1uF
V	Q2N4063	C_1	0.1uF
L_G	110nH	C_2	100pF
L_P	72nH	C_3	0.1uF
U_1	NC7WZ04	U_2	NC7S00
U_3	LTC1799	U_4	UC3842

flowing through the diode should be the same as the average output current.

For the voltage stress of the diode, it can be seen from the simulation results, the peak reverse voltage is about 4 to 5 times of the output voltage. For the voltage stress of the capacitor C_{REC}, it equals to the diode maximum voltage minus the output voltage, which is about 3 to 4 times of output voltage.

Also the multi-stage resonant driving circuit is adopted. The switch input capacitance can be approximately obtained from the switch datasheet, in the prototype, the value of L_P is tuned to achieve desired driving signal. The ON/OFF control method is based on PWM controller UC3842, and eight inverters are in parallel to enhance the driving ability, while maintain a proper equivalent resistor to reduce the diving circuit losses. Table 1 shows the system main components types and values.

Here, the inductor L_{REC} of rectifier stage and the inductor L_S are merged into one inductor L_{SR}. Thus, the value of L_{SR} is 43 nH, which is the paralleled value of the inductors. To determine the value of resonant capacitor C_F and C_{REC}, the parasitic capacitance of switch and diode have been taken into consideration. In higher operating frequency, the values of these capacitances can be further reduced. Then the discrete capacitors can be further reduced and even eliminated. However, for the parasitic capacitances of switch and diode, they are greatly affected by the voltage. And a nonlinear relationship is formed between the capacitance value and voltage.

The operating frequency of enable signal is set to 340 kHz, which can also be changed by adjusting the corresponding resistor and capacitor. The chip has a voltage reference amplifier with reference voltage of 2.5 V. The output voltage of the main circuit is divided by the sampling resistor and then connected to the inverting input terminal of the error amplifier. Then the output is compared with the inverting input sawtooth wave of the internal PWM comparator of the chip to adjust the control duty cycle, and the frequency of control signal is determined by $f_m = 1.72/R_1 \cdot C_4$. Therefore, it can be seen that the control method belongs to constant frequency control. The ratio of resistor R_2 to R_4 determines the maximum duty cycle that the control signal can achieve. Fig. 12 is a block diagram of the closed-loop control of the high frequency converter

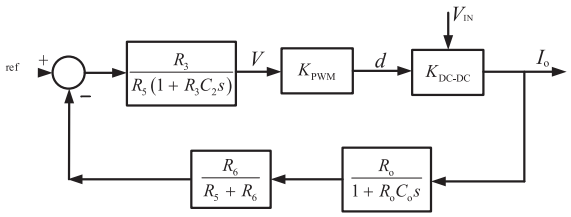


FIGURE 12. The closed-loop block diagram of the proposed converter.

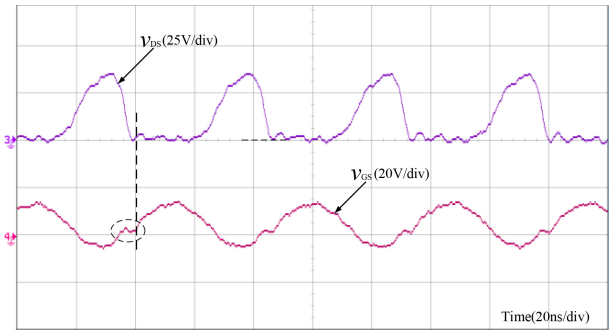


FIGURE 13. The waveforms of switch drain to source voltage and gate voltage.

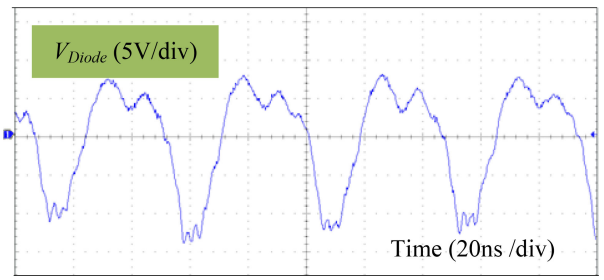


FIGURE 14. The waveforms of diode to ground voltage V_{Diode}.

studied in this paper. The K_{PWM} is the transfer function of the enable signal generator which controls the operating state of the main circuit switch to keep the output voltage constant. $K_{DC–DC}$ represents the transfer function of the proposed high frequency converter. The controller equation is shown in the feedback loop of the system.

Fig. 13 shows the switch drain to source voltage and gate voltage, it can be seen that the switch can turn on in ZVS condition, which greatly reduces the switching losses in high frequency condition. Because of the resonant tank of the resonant driving circuit, the driving voltage is in sine form which can make use of the energy stored in switch input capacitance. Fig. 14 shows voltage waveforms of the rectifier stage input voltage. There are voltage oscillations in the waveform, which is caused by the parasitic components. However, it still can be seen that the operating mode is similar to the analysis result. The transient waveforms when the Enable signal change from 0 to 1 and from 1 to 0 are shown in Fig. 15 and Fig. 16 respectively.

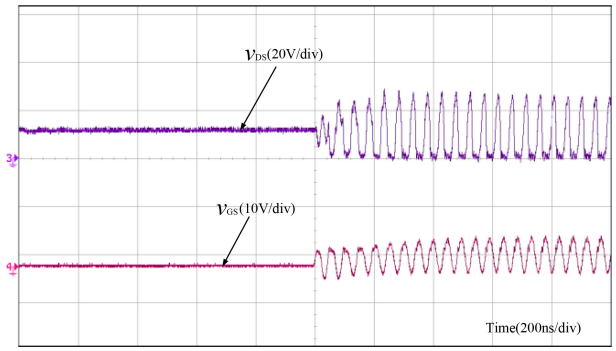


FIGURE 15. The transient waveforms when Enable signal changes from 0 to 1.

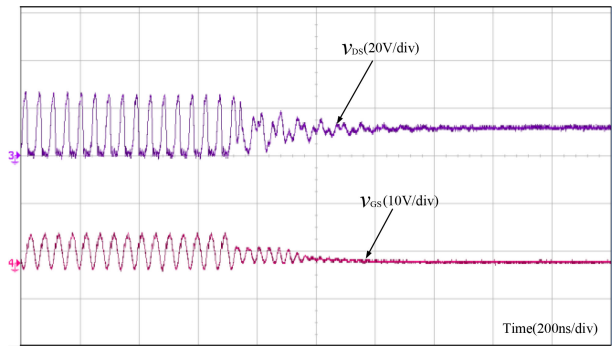


FIGURE 16. The transient waveforms when Enable signal changes from 1 to 0.

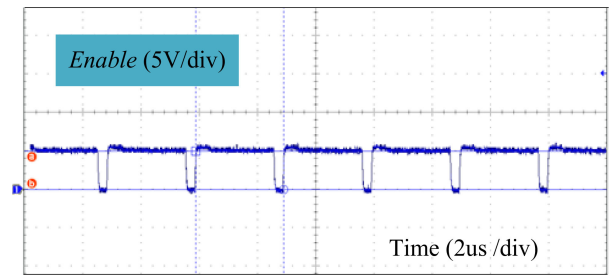


FIGURE 17. The waveforms of enable signal.

Fig. 17 shows the waveforms of enable signal generated by the PWM controller. Fig. 18 shows the output voltage ripple where the DC output voltage is 5 V. With the ON/OFF control method, according to these two figures, it can be seen that when the enable signal is in high level, the output voltage increases. When the enable signal is in low level, the system stops work and the output voltage decreases.

The system efficiency is 75.3% in 8 W rated output power condition. Also, the efficiency of the converter without the multistage resonant driving circuit is tested under rated output power, the efficiency is 71% which shows the feasibility of the resonant driving method.

The losses of the high frequency converter can be divided into inductor losses, diode losses, switch losses and driving circuit losses, which can be calculated as follows.

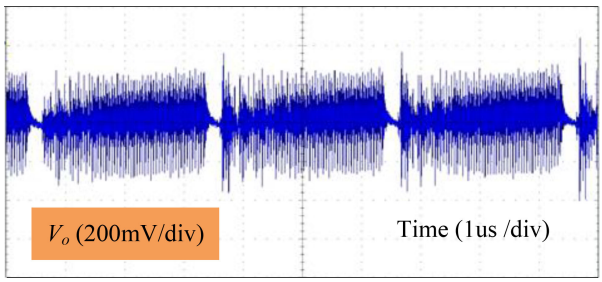


FIGURE 18. The waveforms of output voltage V_o (AC coupled).

In the prototype, all the inductors are aircore ones, thus, there is no magnetic loss. The conduction loss of inductor can be calculated as

$$P_L = I_{ac,rms}^2 \cdot R_{ac}. \tag{19}$$

Here, $I_{ac,rms}$ represents the root-mean square (RMS) value of inductor AC current, whereas R_{ac} represents the inductor AC resistance. In the high frequency condition, the losses of capacitor are ignored because of the high quality factor. Usually, the quality factor of a commercial inductor is around 100. From the datasheet, the corresponding AC resistance can be calculated. For inductor L_F, the loss is about 0.48 W and for inductor L_{SR}, the loss is about 0.04 W.

The losses of switch consist of conduction losses and switching losses. Based on the optimal design of components value, the switch can turn on in ZVS mode. Thus, the switching turn-on losses can be ignored. The conduction losses of the switch are taken into consideration as (20) shown.

$$P_S = I_{rms}^2 \cdot R_{DS,on} \tag{20}$$

where I_{rms} is the RMS value of switch current and $R_{DS,on}$ is the on resistance of the switch. Besides this, the turn-off loss can be estimated around 0.09 W according to simulation results. In the prototype, the switch loss is about 0.34 W.

The diode losses can also be divided into conduction losses and switching losses. In low output voltage condition, the conduction losses play a major role. Thus, the reverse conduction losses are ignored. The conduction losses can be calculated as

$$P_D = I_F \cdot V_F \tag{21}$$

where I_F is the diode average current and V_F is the forward voltage drop. In the prototype, the diode loss is about 0.8 W.

The resonant driving method can take advantage of the energy stored in switch input capacitance, which greatly reduces the losses in the driving circuit. The losses of the resonant driving circuit can be approximately calculated by

$$P_{gate} = 2R_g\pi^2 f^2 C_{iss}^2 V_{gs}^2 \tag{22}$$

where R_g represents the switch gate resistance, C_{iss} represents the switch input capacitance, and V_{gs} is the amplitude of the driving voltage. It can be seen that the driving circuit losses form a proportional relationship with the gate resistance and

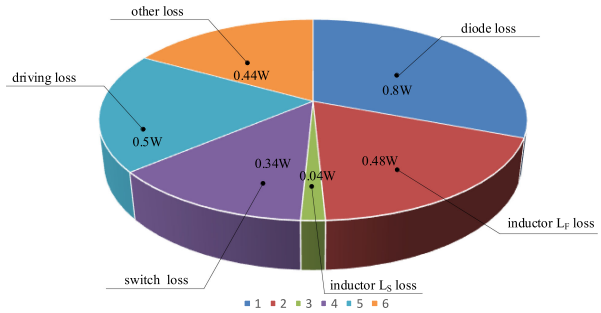


FIGURE 19. **The losses dissipation of the prototype.**

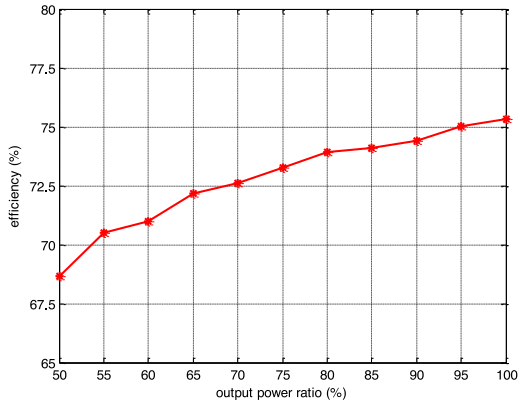


FIGURE 20. **System efficiency curve with the change of output power.**

input capacitance. In driving circuit, besides the gate resistance losses in (22), the losses of the paralleled CMOS inverters can be calculated as follows:

$$P_{inv} = n \cdot C_{PD} \cdot V^2 \cdot f \tag{23}$$

where n is the number of the paralleled inverters, C_{PD} is the power dissipation capacitance, and V is the supply voltage. The driving circuit loss is about 0.5 W.

Besides these calculation results, in the real prototype, there is other loss that we cannot totally take into consideration, such as the control circuit loss, the loss caused by the oscillations, the switch parasitic capacitance loss and so on, the total other loss is about 0.53 W.

Based on aforementioned equations, the losses dissipation of the high frequency converter can be estimated as shown in Fig. 19. It is analyzed at the rated output power condition where the output voltage is 5 V and the output current is 1.6 A. With the change of output power, the system efficiency curve is shown in Fig. 20. From above analysis, it can be seen that the diode loss, input resonant inductor loss, driving loss and other unexpected loss occupy the most part of the total loss. If we want to further increase the system efficiency, we can work from the following parts: 1. Using diode with lower forward voltage or synchronous switch; 2. Using resonant inductor with higher quality factor; 3. Reducing the driving voltage and using switch with small input capacitance; 4. Reducing the parasitic inductor or capacitor to suppress the ringing.

TABLE 2. **Performance Comparison of Similar Converters**

Ref.	Frequency	Power	Input/Output voltage	Efficiency
Proposed	20MHz	8W	10V/5V	75%
[26]	30MHz	50W	36V/24V	73.3%
[27]	46MHz	5.7W	230Vac/15V	78%
[28]	20MHz	10W	12V/5V	80%

The performance of the proposed converter has been compared with other topologies as Table 2 shows. The efficiency of proposed converter is higher than that in [26] even with lower power. Though the efficiency of [27] is higher than the proposed one, it operates at quite low current condition, which greatly reduces the diode forward loss. Because of the adoption of variable width aircore transformer, the high quality factor aircore inductor can also be adopted in the topology to further increase efficiency.

V. CONCLUSION

In this paper, a class E type high frequency DC–DC converter is proposed, which can be divided into three stages, namely inverter stage, matching network stage and rectifier stage. The detailed analysis of three stages are firstly conducted in this paper. With the optimal design, the switch in inverter stage can operate in ZVS condition. Also to further improve efficiency, a multistage resonant driving circuit is adopted to reduce the driving losses. The ON/OFF control method is adopted to regulate output voltage. A 20 MHz, prototype is built in this paper, which verifies the feasibility of high frequency converter. The system efficiency is 75.3% in 8 W rated output power condition.

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