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Passivity-Based Analysis and Design of Linear Voltage Controllers For Voltage-Source Converters

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ABSTRACT This article presents a systematic evaluation on the impedance passivity of voltage-controlled voltage-source converters. The commonly used single- and dual-loop control structures with different linear controllers are compared extensively, considering the effect of the time delay involved in the control loop. A virtual impedance control, co-designed with different voltage control schemes, is then proposed to eliminate the negative output resistance till half of the sampling frequency, which improves the system stability for grid-forming converters in grid-connected applications. Both frequency-domain analysis and experimental results validate the theoretical findings.

INDEX TERMS Voltage-source converter, voltage control, passivity, harmonic stability, impedance analysis.

NOMENCLATURE

L_g, L_{g1}, L_{g2}	Inductances in grid impedance
C_g	Capacitance in grid impedance
L_1	LC filter inductance of the voltage-source converter (VSC)
C_f	LC filter capacitance of the VSC
f_{LC}	LC resonant frequency
f_0/ω_0	Fundamental frequency/angular frequency
f_s (T_s)	Sampling frequency (sampling period)
f_{sw}	Switching frequency
v_g	Grid voltage
v	Capacitor voltage
i_1	VSC-side current flowing though L_1
i_2	VSC output current
G_v	Transfer function of the voltage controller
K_{pv}	Proportional (P) controller gain in G_v
K_{rv}	Resonant (R) controller gain in G_v
ζ	Damping factor in the R controller
K_{iv}	Integral (I) controller gain in G_v
PI-dominant	Controller can be approximated as a PI controller in the high-frequency response (e.g., PR controller)
I-dominant	Controller can be approximated as an I controller in the high-frequency response (e.g., R, PR-I, or IR controller)
K_P	Equivalent P controller gain of G_v in the high-frequency response
K_I	Equivalent I controller gain of G_v in the high-frequency response
G_i	Transfer function of the current controller
K_{pi}	P controller gain in G_i
G_d	Transfer function of the time delay
T_d	Total delay time in the digital control
f_c/ω_c	Critical frequency/angular frequency that changes the sign of $\cos(\omega T_d)$
H_v	Transfer function of the voltage feedback decoupling loop
Z_v	Transfer function of the virtual impedance
T_v	Loop gain of the voltage control
f_{mc}	Magnitude crossover frequency of T_v
T_i	Loop gain of the current control
GM	Gain margin
Z_o	VSC output impedance
R_o	Real part of the output impedance

$-R$ region Non-passive region, i.e., frequency range where the VSC has a negative resistance

I. INTRODUCTION

Voltage-source converters (VSCs) are widely used with renewable energy resources [1]. The grid-following control, which employs the voltage-oriented vector current control, has been dominant for the past decade for VSCs [2]. However, the increasing share of VSC-based resources is fundamentally changing the grid operation, and the grid-following control tends to have more instability issues, particularly seen in weak grids [3]. To tackle this challenge, the grid-forming control, which operates the VSC as a voltage-stiff source using vector-voltage control, is developed [4]–[8], and hence, the dynamic behavior of the vector-voltage control becomes important for the grid-forming VSCs.

The vector-voltage control has for long time since been used with uninterruptible power supplies [9], [10], energy storage systems [11], and converter-based micro-grids [12]–[14]. The voltage control schemes based on linear controllers have been extensively studied, which can be classified into two groups, i.e., the single-loop control [15]–[18] and the dual-loop control [19]–[23], in respect to the number of feedback control variables [24]. The single-loop control directly regulates the output voltage across the LC-filter capacitor [18], while the dual-loop control adds an inner feedback loop based on the inductor current [23]. The inner current loop allows preventing VSCs from overcurrent and embedding a virtual resistance to dampen the LC-filter resonance [22]. However, due to the time delay of the digital control (T_d), the virtual resistance emulated by the proportional current controller becomes negative in the frequency range above the critical frequency, i.e., $1/(4T_d)$ [25], which jeopardizes the stability of the inner current loop. Furthermore, the stability of outer voltage loop can be also threatened, since the phase of the voltage loop gain considering the time-delay impact tends to cross over 180° around the LC resonant frequency [18]. Therefore, the single-loop voltage control is usually preferred in the low pulse-ratio (i.e., the ratio of the VSC switching frequency to the fundamental frequency) applications, e.g., the aircraft power supplies at the fundamental frequency of 400 Hz [16], [17].

To address the adverse effect of the time delay and widen the frequency region of stable operation, several voltage controllers have been reported recently. For single-loop control structure, instead of using the conventional proportional + integral (PI) controller in the dq frame or P + resonant (PR) controller in the $\alpha\beta$ frame, only the R controller tuned at the fundamental frequency in the $\alpha\beta$ frame is developed in [17] to widen the stability region. Alternatively, a PR-I controller co-designed with a low-pass filter added into the voltage feedback decoupling loop is proposed in [18], which further widens the stability region. The prominent features of those controllers include: 1) the resonant behavior at the fundamental frequency to guarantee zero steady-state tracking error in the $\alpha\beta$ frame; 2) the dominant integral (I-dominant) behavior in the high-frequency range, which adds a phase lag to prevent the phase of the loop gain from crossing over 180° around the LC resonant frequency [18]. The same benefit applies also to the dual-loop control, which can alternatively be realized by different I-dominant controllers as discussed in [24].

Within the dual-loop control structure, the additional feedback decoupling loop from the capacitor voltage to the output of the inner current controller can also be embedded, which not only mitigates the effect of time delay, but also leads to better damping and improved transient response [26]. Besides the voltage-feedback decoupling control, the output-current feedforward control has also been utilized to synthesize various virtual impedances for VSCs [27]–[32]. However, most of those control schemes are focusing on the stability and waveform quality of the voltage control under the LC filter resonance, the nonlinear and unbalanced loads. The impedance passivity of the voltage control, i.e., the negative output resistance (damping) contributed from the voltage-controlled VSCs to the connected electrical systems [33], is seldom discussed.

The impedance passivity is a frequency-domain interpretation of a system passivity from the input-output viewpoint for an n-port linear time-invariant system [34]. Differing from the time-domain analysis based on energy storage functions [35]–[37], the passivity analysis based on frequency-domain impedance models allows for a control design-oriented analysis for small-signal stability enhancement [38], thus it has been extensively studied with current-controlled VSCs in grid-connected applications [39]–[46]. It has been pointed out that the time delay together with the current controller can lead to negative resistance of the VSCs in the high-frequency range, which could result in harmonic oscillations when interacting with the grid impedances [38]. Several passivity enhancement solutions have been put forward for current-controlled VSCs. A voltage feedforward control by a differentiator can be used to widen the passive region till half of the sampling frequency [41], whose performance is further discussed by passivity indices from the perspective of the entire system [42]. However, this derivative feedforward control method is merely applicable for the converter-side current control. A damping injection method by embedding a discrete derivative controller into the current controller is thus studied for passivity enhancement, which applies to both converter-side and grid-side current control [43]. However, the analysis relies on a detailed discrete-domain model, which leads to a difficult parameter tuning effort. The non-passivity caused by resonant current controllers can be mitigated by implementing the delay compensation method [44] or embedding a predictive current controller [45]. In addition to controller design, a co-design method of LCL filters is put forward for paralleled VSCs, by which the non-passive region can be canceled [46]. These passivity-based studies mainly focus on the single-loop current control, where the control interactions are relatively simple, thus they cannot be readily applied to voltage-controlled VSCs with multiple feedback control loops.

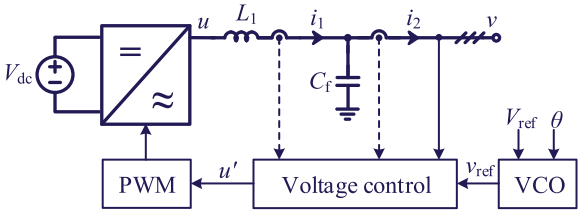

FIGURE 1. **Voltage-controlled VSC with LC filter.**

Only a few attempts to improve the impedance passivity of voltage-controlled VSCs can be found in [47], [48]. A passivity-oriented voltage control scheme is reported in [47]. Yet, the modeling and controller design are based on the discrete-domain model, by which it is difficult to reveal the explicit relationship between the passivity and the voltage control. With the continuous-domain modelling, the non-passive region for voltage-controlled VSCs can be analytically derived in the frequency domain [48]. However, this work only considers a specific dual-loop control scheme. The impedance passivity affected by the diversity of voltage control schemes still remain unclear, such as the single-loop control and the dual-loop control considering the voltage-feedback decoupling loop.

This paper thus presents a systematic evaluation of the impedance passivity of voltage-controlled VSCs. It begins with general modeling of both the single-loop and dual-loop control schemes, from which the preference of employing a high-frequency I-dominant controller for the voltage loop is pointed out. The impedance passivity for both control structures is further analyzed with an explicit non-passive region derived. Next, a passivity-based virtual impedance control is proposed, which is co-designed with the high-frequency I-dominant voltage controllers or the dual-loop control with voltage feedback decoupling loop. The method allows widening the passive region till half of the sampling frequency, which applies to different control schemes. Finally, stability analysis and experimental results are given to validate the effectiveness of the controller design.

II. SYSTEM DESCRIPTION AND MODELLING

Fig. 1 shows a single-line diagram of a voltage-controlled VSC with an LC filter. The capacitor voltage v is controlled by a voltage controller, and the voltage reference v_{ref} is generated by a voltage control oscillator (VCO). i_1 and i_2 denote the inductor current and the VSC output current, respectively. It is noted that even though the LCL filter is usually installed in real applications, the grid-side filter represents the external disturbance for the voltage control, therefore, it is not considered in the following VSC modeling and control design. A constant dc-link voltage is assumed. The system configuration and control scheme apply to both single- and three-phase converters. In addition, there can be any outer-loop power control used for voltage reference generation, whose slower dynamics are neglected. Therefore, the following modeling and analysis only focus on the high-frequency dynamics of the VSC.

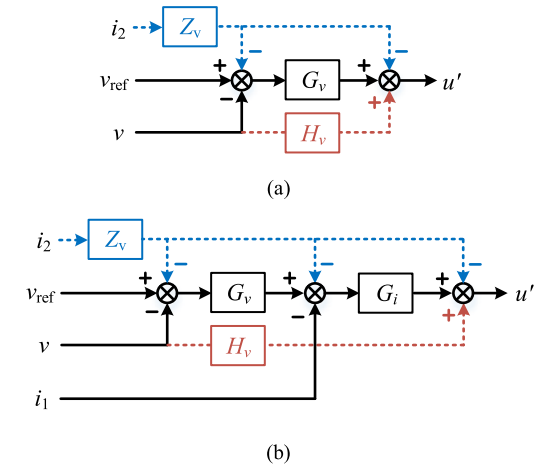

FIGURE 2. **Voltage control schemes in VSCs. (a) Single-loop control; (b) Dual-loop control.**

TABLE 1. **Main System Parameters For the Studied VSC in Fig. 1**

Quantity	Symbol	Value
DC-link voltage	V_{dc}	700 V
Filter inductance (resistance)	L_1 (ESR)	2 mH (0.1 Ω)
Filter capacitance	C_f	3 μF [a] / 10 μF [b]
LC resonant frequency	f_{LC}	2.06 kHz [a] / 1.13 kHz [b]
Voltage reference magnitude	V_{ref}	190 V
Switching / sampling frequency	f_{sw} / f_s	10 kHz / 10 kHz

[a]Single-loop control; [b]Dual-loop control.

Fig. 2 illustrates the general structures of the single-loop control and the dual-loop control. The single-loop control directly regulates the capacitor voltage by G_v, while the dual-loop control adds an inner inductor current control loop using G_i. In addition to the two feedback loops, feedforward loops or feedback decoupling loops can be alternatively added for the improved dynamic performance [9]. The feedforward control is based on the output current, which is also known as the virtual impedance control represented by Z_v in the blue dashed paths. It is noted that Z_v can be flexibly fed forward to different locations with various forms of controllers. The capacitor voltage feedback decoupling control is added to the modulated voltage through H_v in the red dashed paths.

The main system parameters of the studied VSC are listed in Table 1. The following derivations are carried out by assuming that the VSC switching frequency is equal to the sampling frequency (f_s) and the total delay time (T_d) is $1.5T_s$ ($T_s = 1/f_s$), but the conclusions can be extended to the VSCs with unequal switching and sampling frequencies and different delay time, which will be discussed in Section IV. Since the stable frequency region of the LC filter resonant frequency (f_{LC}) for the single-loop control is ($f_s/6$, $f_s/2$) with $T_d = 1.5T_s$ [18], and that for the dual-loop control is (0 Hz, $f_s/6$) [23], two sets of capacitances are selected for C_f.

The VSC can be treated as a linear time-invariant system with a constant dc-link voltage [49], whose small-signal

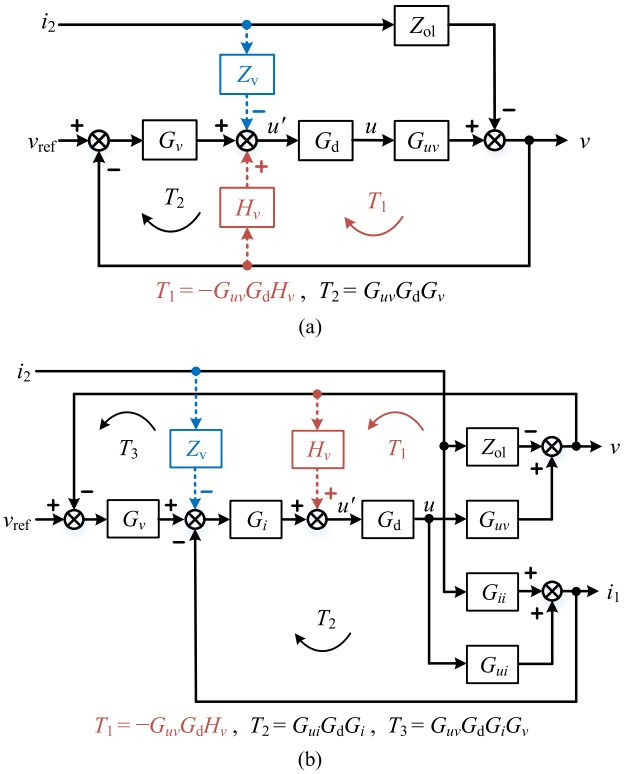

FIGURE 3. Small-signal models of VSC. (a) Single-loop control; (b) Dual-loop control.

models with the single-loop or dual-loop control are shown in Fig. 3, where the feedforward control loop Z_v is optionally added at the output of the voltage controller. All the transfer functions are represented in the continuous domain, yet with the Laplace transform variable "s" omitted for brevity. Since the transfer functions of the plant and controllers are symmetrical in the $\alpha\beta$ frame, the system dynamics can be represented by a single-input and single-output (SISO) model. Z_{ol} (open-loop impedance), G_{uv}, G_{ii}, and G_{ui} are the transfer functions derived from the plant, which are

$$Z_{ol} = \frac{Z_{L1}}{1 + Z_{L1}Y_{Cf}}, \tag{1}$$

$$G_{uv} = \frac{1}{1 + Z_{L1}Y_{Cf}}, \tag{2}$$

$$G_{ii} = \frac{1}{1 + Z_{L1}Y_{Cf}}, \tag{3}$$

$$G_{ui} = \frac{Y_{Cf}}{1 + Z_{L1}Y_{Cf}}, \tag{4}$$

where Z_{L1} is the impedance of L_1 and Y_{Cf} is the admittance of C_f. G_d denotes the transfer function of time delay, which is given by

$$G_d = e^{-sT_d} = e^{-1.5sT_s} \tag{5}$$

TABLE 2. Control Parameters For the Studied VSC

Single-loop control (Fig. 3(a))						
Control type	Voltage loop					
PR	K_{pv}	0.025	K_{rv}	1000 s^{-1}		
R	K_{rv}		2400 s^{-1}			
PR-I	K_{pv}	2400	K_{rv}	20000 s^{-1}		
IR	K_{iv}	1200	K_{rv}	1200 s^{-1}		
Dual-loop control (Fig. 3(b))						
Control type	Current loop		Voltage loop			
PR	K_{pi}	8 Ω	K_{pv}	0.012 S	K_{rv}	50 S/s
R	K_{pi}	8 Ω	K_{rv}		350 S/s	
PR-I	K_{pi}	8 Ω	K_{pv}	350 S/s	K_{rv}	35000 S/s^2
IR	K_{pi}	8 Ω	K_{iv}	175 S/s	K_{rv}	175 S/s
PR&H_v	K_{pi}	12 Ω	K_{pv}	0.06 S	K_{rv}	10 S/s

The voltage loop gain and the VSC output impedance for the single-loop control are then derived from Fig. 3(a) as

$$T_v = \frac{T_2}{1 + T_1} = \frac{G_{uv}G_dG_v}{1 - G_{uv}G_dH_v}, \tag{6}$$

$$Z_o = -\frac{v}{i_2} = \frac{Z_{ol} + G_{uv}G_dZ_v}{1 + T_1 + T_2} \tag{7}$$

The voltage-loop gain and the control output impedance for the dual-loop control are derived from Fig. 3(b) as

$$T_v = \frac{T_3}{1 + T_1 + T_2} = \frac{G_{uv}G_dG_iG_v}{1 - G_{uv}G_dH_v + G_{ui}G_dG_i} \tag{8}$$

$$Z_o = -\frac{v}{i_2} = \frac{Z_{ol}\,(1 + T_2) + G_{uv}G_dG_iG_{ii} + G_{uv}G_dG_iZ_v}{1 + T_1 + T_2 + T_3} \tag{9}$$

In (6)–(9), the terms represented by Z_v model the dynamic effects of the feedforward control loops, while the terms represented by T_1 denote the effects of the feedback decoupling control loops. It is seen that the feedforward control loop merely shapes the control output impedance without impacting the voltage-loop gain, while the feedback decoupling control loop influences both the voltage-loop gain and the control output impedance.

III. VOLTAGE CONTROL EVALUATION

In this section, the impacts of controllers on the voltage-loop gain are evaluated first for both single-loop control and dual-loop control, and the design guideline for improving the voltage control performance is summarized. The virtual impedance control is not considered in this section, since it does not affect the voltage loop gain. All the control parameters used for the following analysis are listed in Table 2. How they are selected will be introduced in the following analysis.

The control is implemented in $\alpha\beta$ frame, thus R controllers [50] are utilized, whose transfer function is defined as

$$K_rR(s) = \frac{K_rs}{s^2 + 2\zeta\omega_0 s + \omega_0^2}, \tag{10}$$

TABLE 3. Different Voltage Controllers and Their Approximations

Controller Type	Transfer Function	High-frequency approximation
PR	$G_v = K_{pv}+K_{rv}R(s)$	$G_v \approx K_P+K_I/s = K_{pv}+ K_{rv}/s$
R	$G_v = K_{rv}R(s)$	$G_v \approx K_I/s = K_{rv}/s$
PR-I	$G_v = (K_{pv}+K_{rv}R(s))/s$	$G_v \approx K_I/s = K_{pv}/s$
IR	$G_v = K_{iv}/s+K_{rv}R(s)$	$G_v \approx K_I/s = (K_{iv}+K_{rv})/s$

where K_r is the R controller gain, ζ is the damping factor, and ω_0 is the central angular frequency. In this work, ζ is selected as 0.01 to consider a bandwidth of 1 Hz for the R controller in case of any frequency drift in ω_0 [51]. The R controller provides sufficiently large gain at ω_0 and introduces an integral behavior in the high-frequency range larger than ω_0. It is worth noting that if the control is implemented in the dq frame, all R controllers should be replaced with I controllers, and the controller transfer functions can then be transformed into the $\alpha\beta$ frame for modeling and analysis. Then, the frequency shift caused by the inverse Park transformation needs to be considered in controller transfer functions [52].

For the voltage control design, different factors, such as gain margin (GM), phase margin, and magnitude crossover frequency (f_{mc}), can be considered. This section focuses on discussing the stability limitations of different voltage control schemes. Thus, the same stability margin is designed in order to compare the maximum magnitude crossover frequencies. All cases are designed with the same GM of 3 dB.

A. SINGLE-LOOP CONTROL

For the single-loop control, the controller is designed by analyzing the voltage loop gain directly. If G_v is a P controller, it will be merely stable when f_{LC} belongs to $(f_s/3, f_s/2)$, while if G_v is I-dominant in the high-frequency range, the stable region of f_{LC} will be widened to $(f_s/6, f_s/2)$ [18]. Thus, the conventional proportional and resonant (PR) controller, which behaves as a PI controller in the high-frequency range, will have a stable region in between the aforementioned two frequency ranges. Hence, the high-frequency I-dominant controller is preferred for the single-loop control, which can be realized by different controllers, such as the R controller only, the PR-I controller, or the IR controller [24]. These controllers and their high-frequency approximations are listed in Table 3.

The Bode diagrams of voltage-loop gains with different controllers are plotted for the single-loop control in Fig. 4. They are all designed with GMs of 3 dB, which are denoted by the solid circles in the magnitude plot. Then, the maximum magnitude crossover frequencies can be compared. According to (6), when the feedback decoupling loop is disabled ($H_v = 0$), G_{uv} introduces an LC resonant peak in the high-frequency range at f_{LC}, while G_v can shape the loop gain differently according to the controller types given in Table 3. In (6), the total phase lag of T_v is contributed by the sum of phase

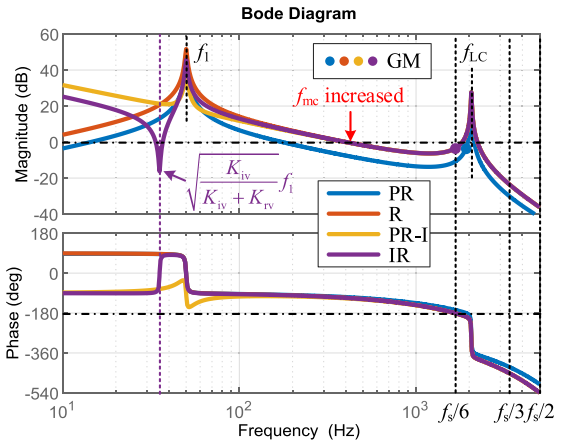

FIGURE 4. Bode diagram of voltage loop gain for single-loop control (Fig. 3(a)) using different controllers.

lags of G_v, G_d, and G_{uv}. G_d introduces phase lag gradually as the frequency increases, which reaches to $-90°$ at $f_s/6$, and G_{uv} leads to a phase drop of $-180°$ at f_{LC}. If G_v is PI-dominant (PR) in the high-frequency range, by adding their phase lags up, the phase response of T_v can easily cross over $-180°$ at f_{LC}. Consequently, due to the poorly damped LC resonance, a low enough gain of G_v is required to guarantee a positive GM. This explains why the PR control results in a low magnitude-crossover frequency, i.e., f_{mc}. It is noted that this indicates a different single-loop control design rule compared with L-filtered current-controlled VSCs, where usually a high bandwidth around 1/10 of the switching frequency is achievable with enough stability margin [53]. The other three high-frequency I-dominant controllers (R, PR-I, IR) introduce more phase lag than the PR controller, by which the phase response of T_v can cross over $-180°$ exactly at $f_s/6$. Then at $f_{LC} > f_s/6$, the phase response has already exceeded $-180°$, thus the gain of G_v can be designed relatively larger, leading to a higher f_{mc} and a better control performance. Moreover, both the PR-I and IR controllers feature a higher gain in the low-frequency range than the R controller. The IR controller yields a pair of conjugate zeros below the fundamental frequency, yet it does not affect much on the voltage control performance.

In the single-loop voltage control, the feedback decoupling loop by a lower-pass filter can be used to further widen the stability region to $f_{LC} > f_s/4$ [18]. This damping control is unnecessary for the case when $f_{LC} > f_s/6$ is satisfied, as shown in Fig. 4, thus it is not discussed further in this article.

B. DUAL-LOOP CONTROL

In the dual-loop control, the inner current loop is designed first. It is assumed to be merely with P controller in the stability analysis, due to the negligible effect of the R controller in the high-frequency range [53], i.e., $G_i = K_{pi}$. The current loop gain is derived as

$$T_i = \frac{T_2}{1+T_1} = \frac{sC_f G_d K_{pi}}{1+s^2 L_1 C_f - G_d H_v} \tag{11}$$

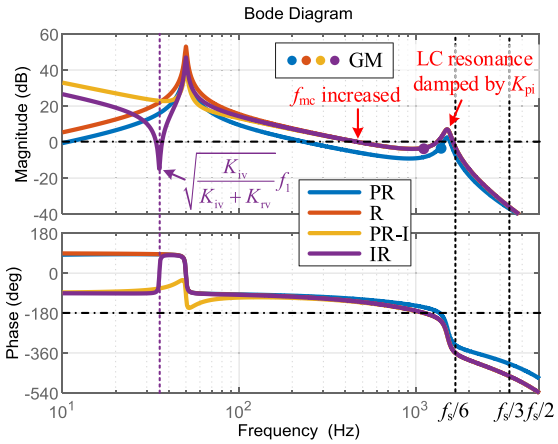

FIGURE 5. Bode diagram of voltage loop gain with different voltage controllers for dual-loop control (Fig. 3(b)).

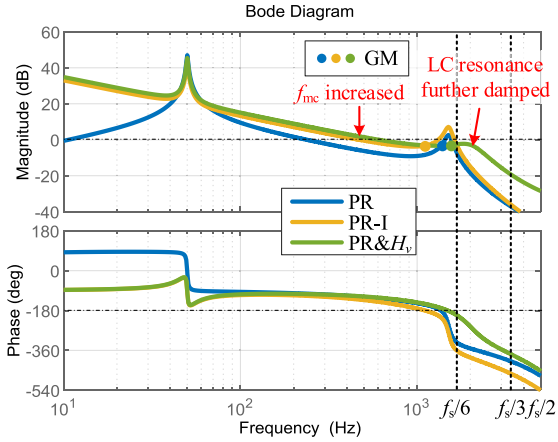

FIGURE 6. Bode diagram of voltage loop gain for dual-loop control (Fig. 3(b)) with and without feedback decoupling.

It is worth noting that the current loop should be designed to be stable first. Otherwise, the outer voltage loop will have a non-minimum phase response, which cannot be stabilized [23]. Consequently, the current-loop gain is designed to achieve a positive GM. In this work, $K_{\rm pi} = 8\ \Omega$ is chosen to achieve a GM of 3 dB for $H_v = 0$, based on the parameters given in Table 1.

Then the voltage loop is designed by closing the current loop. The voltage loop gain can be further represented as

$$T_v = \frac{T_3}{1+T_1+T_2} = \frac{G_{\rm d}K_{\rm pi}G_v}{1+s^2L_1C_{\rm f}+sC_{\rm f}G_{\rm d}K_{\rm pi}-G_{\rm d}H_v} \quad (12)$$

1) NO VOLTAGE FEEDBACK DECOUPLING

From (12), when H_v is disabled, the current controller gain as well as the time delay provides active damping to the LC resonance, yet the resultant voltage loop gain is still similar to that of the single-loop control given by (6). Therefore, the design of the dual-loop voltage control follows the same rule as that for the single-loop control, i.e., using a high-frequency I-dominant controller to obtain a higher magnitude-crossover frequency [24]. The Bode diagrams for the designed voltage loop gains are shown in Fig. 5, which only differ from Fig. 4 around the LC resonant frequency, where the magnitude responses are damped by the current controller and the phase drops are slightly shifted due to the time delay effect.

2) WITH VOLTAGE FEEDBACK DECOUPLING

With H_v enabled by a unity gain [26], the voltage loop gain in the low-frequency range can be approximated as

$$T_v = \frac{T_3}{1+T_1+T_2} \underset{s=j\omega}{\overset{\text{low}f}{\approx}} \frac{K_{\rm pi}G_v}{j\omega\left(T_{\rm d}+C_{\rm f}K_{\rm pi}\right)} \quad (13)$$

where an integral behavior in the low-frequency range is coming from the cancellation effect of $1-G_{\rm d}H_v$. It is noted that this low-frequency range for the integral behavior is wide enough almost till one tenth of the sampling frequency. Consequently, there is no need to use a high-frequency I-dominant controller for G_v to increase the low-frequency magnitude of the loop gain, and thus the conventional PR controller is sufficient to achieve a larger $f_{\rm mc}$. This control is referred to as PR&H_v control for brevity in the following analysis.

The decoupling effect of $1-G_{\rm d}H_v$ also applies to the inner current loop gain according to (11), thus $K_{\rm pi}$ can be designed with a larger value than without H_v, for the same GM of the current loop, which provides more active damping to the LC resonance. In this case, $K_{\rm pi}$ can be increased to 12 Ω with a GM of 3 dB. The Bode diagram of the voltage loop gain for the PR&H_v control is plotted in Fig. 6. It is clear that compared with the PR control and PR-I control, the PR&H_v control further dampens the LC resonance with the increased $K_{\rm pi}$. And the decoupling effect of $1-G_{\rm d}H_v$ results in a similar reference tracking effect to the PR-I control.

C. SUMMARY

In summary, the LC-filter resonance together with the time delay can easily result in phase crossing over 180° around $f_{\rm LC}$ for the voltage-controlled VSC, which poses challenges to the design of a fast voltage control loop using conventional PR controller only. Hence, there are several ways to enhance the voltage control performance:

a) A conventional way is to add the inner current control loop to provide active damping to the LC resonance. This is the major difference between the single-loop control and the dual-loop control in respect to the voltage control loop gain, yet the improvement is limited by the time delay.
b) Using high-frequency I-dominant voltage controllers to provide additional phase lag, such that the loop-gain phase crossing over 180° can be prevented around the LC resonant frequency. Such a way can significantly increase the magnitude-crossover frequency and apply for both the single-loop control and the dual-loop control.
c) Applying the voltage feedback decoupling loop with unity gain for dual-loop control. On one hand, due to the

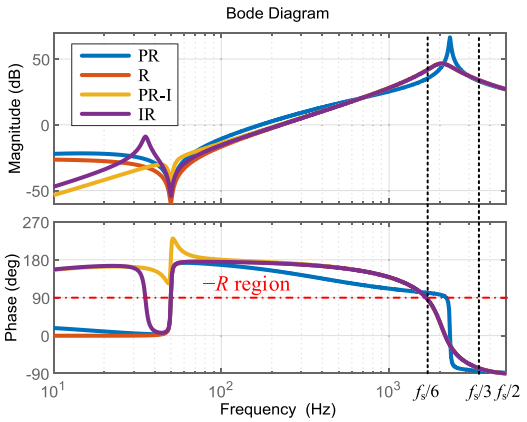

FIGURE 7. Bode diagram of closed-loop output impedance for single-loop control using different controllers.

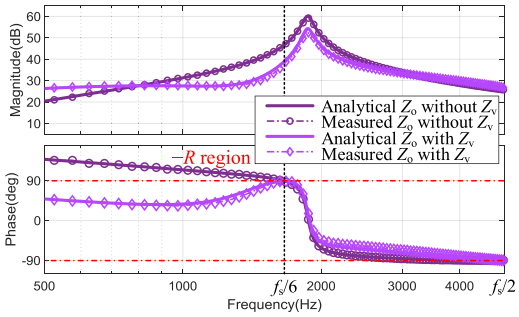

FIGURE 8. Closed-loop output impedances without / with virtual impedance control Z_v for single-loop control obtained analytically and by frequency scan.

compensation effect of time delay in the low frequency range, the current-loop P controller can be designed larger to provide more damping to the LC resonance. On the other hand, the low-frequency integral behavior is naturally introduced in the voltage loop gain, which helps to widen the control bandwidth.

IV. PASSIVITY ANALYSIS AND DESIGN

The impedance passivity of the voltage-controlled VSC implies that the control output impedance Z_o has non-negative real part, i.e., the phase response of Z_o is within $[-90°, +90°]$ [38]. Based on the controller design in Section III, the impedance passivity of both the single-loop and dual-loop are discussed in this section. The virtual impedance control is optionally considered because of its shaping impact on the output impedance profile. The passivity-based virtual impedance control, co-designed with various voltage control schemes, is then proposed.

A. SINGLE-LOOP CONTROL

1) PASSIVITY ANALYSIS

For the single-loop control, supposing that $G_v \approx K_P + K_I/s$ is valid for the high-frequency approximation, it can be derived that the sign of the real-part of Z_o, i.e., R_o, is determined by

$$\mathrm{sgn}\{R_o(\omega)\} = \mathrm{sgn}\{-K_P\omega L_1 \sin(\omega T_d) - K_I L_1 \cos(\omega T_d)\} \tag{14}$$

where sgn{•} is the sign function. It can be seen that R_o changes with the frequency and its sign is influenced by the time delay, the control parameters and the L filter. When the high-frequency I-dominant controllers are used with G_v, assuming $K_P = 0$, the sign of R_o is merely dependent on the sign of $\cos(\omega T_d)$. The critical frequency is thus defined as the frequency where the sign of $\cos(\omega T_d)$ changes, i.e., $f_c = 1/(4T_d)$, which is $f_s/6$ when $T_d = 1.5T_s$. Consequently, $R_o < 0$ for $f < f_s/6$, while $R_o > 0$ for $f_s/6 < f < f_s/2$. That is to say, the single-loop voltage control can result in a negative resistance in the low-frequency range.

Fig. 7 compares the closed-loop output impedances for the single-loop voltage control with different controllers. If the effect of different controllers near the fundamental frequency is neglected, it is found that the non-passive $(-R)$ region appears in a wide low-frequency range. The PR control results in a wider $-R$ region, while the other three high-frequency I-dominant controllers reduce the $-R$ region to $f < f_s/6$.

2) PASSIVITY DESIGN BY VIRTUAL IMPEDANCE

It is indicated by (7) that the virtual impedance control can reshape the output impedance and it is thus used to mitigate the non-passive region of the control output impedance.

Since high-frequency I-dominant controllers can widen the voltage control bandwidth and simplify the $-R$ region to $f < f_s/6$, the virtual impedance control is co-designed with $G_v \approx K_I/s$ for the high-frequency response. Supposing first that Z_v adopts a P controller, it can be derived that

$$\mathrm{sgn}\{R_o(\omega)\} = \mathrm{sgn}\left\{\left[Z_v\left(1-\omega^2 L_1 C_f\right) - K_I L_1\right]\cos(\omega T_d)\right\} \tag{15}$$

which is determined by the multiplication of $\cos(\omega T_d)$ and a frequency-dependent coefficient. If such a coefficient can be designed to have the same sign with $\cos(\omega T_d)$ till $f_s/2$, then the passivity of Z_o will be guaranteed till $f_s/2$. Hence, the sufficient condition of the passivity is

$$Z_v = \frac{K_I L_1}{1-\left(\frac{\pi}{2T_d}\right)^2 L_1 C_f} = \frac{K_I L_1}{1-\left(\frac{\omega_s}{6}\right)^2 L_1 C_f} > 0 \tag{16}$$

for the single-loop voltage control with high-frequency I-dominant controllers. It is noted that $\pi/(2T_d)$ is the critical angular frequency, i.e., ω_c ($\omega_s/6$ in this case), that changes the sign of $\cos(\omega T_d)$.

Fig. 8 shows the impact of virtual impedance control on the output impedance of the single-loop control with a high-frequency I-dominant controller, where an IR controller is used as an example. The analytical results are calculated by (7), and the measured results are also provided by means of the frequency scan in simulations using switching models, which prove the accuracy of the modeling. It can be seen that the virtual impedance control can eliminate the $-R$ till half of the sampling frequency.

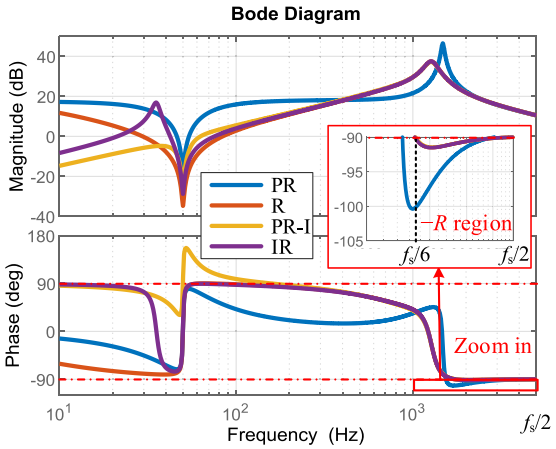

FIGURE 9. Bode diagram of closed-loop output impedance for dual-loop control using different controllers.

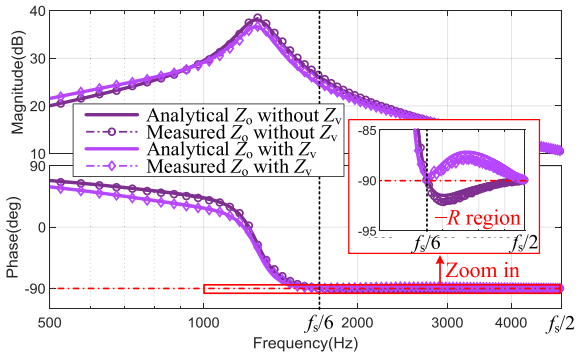

FIGURE 10. Closed-loop output impedances without / with virtual impedance control Z_v for dual-loop control obtained analytically and by frequency scan.

B. DUAL-LOOP CONTROL

1) PASSIVITY ANALYSIS

The passivity of Z_o for the dual-loop control is analyzed in the same way by supposing that $G_v \approx K_P + K_I/s$ for the high-frequency approximation, which yields

$$\begin{aligned}&\operatorname{sgn}\{R_o(\omega)\}\\&= \operatorname{sgn}\Big\{-\omega L_1 K_{pi} K_P \sin(\omega T_d) + K_{pi}(1 - K_I L_1)\cos(\omega T_d)\\&\quad + K_{pi}^2 K_P\Big\}\end{aligned} \tag{17}$$

Similarly, the time delay and controller parameters impact the –R region. When $K_P = 0$, the sign of R_o is also merely dependent on the sign of $\cos(\omega T_d)$. Hence, the high-frequency I-dominant controllers can simplify the –R region for the dual-loop control. Due to $K_I L_1 < 1$, it can be further derived that –R appears for $f_s/6 < f < f_s/2$ when $T_d = 1.5\ T_s$. This is in oppose to the result of single-loop control.

Fig. 9 compares the closed-loop output impedances for the dual-loop control with different voltage controllers. It can be found that the high-frequency I-dominant controllers also significantly reduce the –R region compared with the PR controller.

2) PASSIVITY DESIGN BY VIRTUAL IMPEDANCE

Considering the virtual impedance control, the –R region for the dual-loop control based on high-frequency I-dominant controllers can be determined by

$$\begin{aligned}&\operatorname{sgn}\{R_o(\omega)\}\\&= \operatorname{sgn}\left\{K_{pi}\left[1 - K_I L_1 + Z_v\left(1 - \omega^2 L_1 C_f\right)\right]\cos(\omega T_d)\right\}\end{aligned} \tag{18}$$

To make Z_o passive till $f_s/2$, the sufficient condition is derived as

$$Z_v = \frac{1 - K_I L_1}{\left(\frac{\pi}{2T_d}\right)^2 L_1 C_f - 1} = \frac{1 - K_I L_1}{\left(\frac{\omega_s}{6}\right)^2 L_1 C_f - 1} > 0 \tag{19}$$

Fig. 10 shows the impact of virtual impedance control on the output impedance of the dual-loop control, where an IR controller is used as an example. From the zoom-in view in Fig. 10, it is clear that the –R region within $(f_s/6, f_s/2)$ can be eliminated by the virtual impedance control.

3) PASSIVITY DESIGN WITH VOLTAGE FEEDBACK DECOUPLING

As elaborated in Section III, the unity voltage feedback decoupling loop essentially introduces an integral behavior in the low-frequency range, which leads to a similar voltage control performance to the PR-I control. The passivity-based design for the PR&H_v control is thus discussed further in the following.

Supposing that $G_v \approx K_P + K_I/s$ for the high-frequency approximation and considering the virtual impedance control, the sign of R_o can be determined by

$$\begin{aligned}&\operatorname{sgn}\{R_o\}\\&= \operatorname{sgn}\left\{\begin{array}{l}-\omega L_1\left(K_{pi}K_P - H_v\right)\sin(\omega T_d)\\+K_{pi}\left[1 - K_I L_1 + Z_v\left(1 - \omega^2 L_1 C_f\right)\right]\cos(\omega T_d)\\+K_{pi}(1 + Z_v)\left(K_{pi}K_P - H_v\right)\end{array}\right\}\end{aligned} \tag{20}$$

It can be seen that only if $K_{pi}K_P = H_v$, the –R region can be simply determined by the term of $\cos(\omega T_d)$, and then the passivity of Z_o can be guaranteed till $f_s/2$ by using (19).

Fig. 11 examines the impedance passivity for the PR&H_v control. To realize a passivity design, $K_{pi} = 10\ \Omega$ and $K_P = K_{pv} = 0.1$ S is chosen such that $K_{pi}K_P = H_v = 1$. It can be seen that the –R region within $(f_s/6, f_s/2)$ can also be effectively eliminated by the virtual impedance.

C. DISCUSSION

1) PARAMETER VARIATION

The proposed passivity-based design in (16) and (19) relies on the controller gain, time delay, and LC filter parameters. The controller gain and time delay are relatively constant, yet the LC filter parameters can vary from manufacturers and

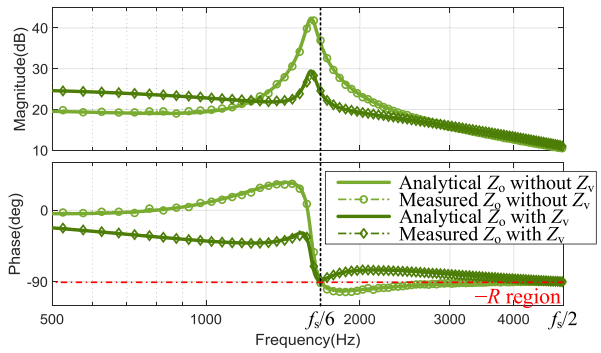

FIGURE 11. Closed-loop output impedance without / with virtual impedance control Z_v for PR&H_v control obtained analytically and by frequency scan.

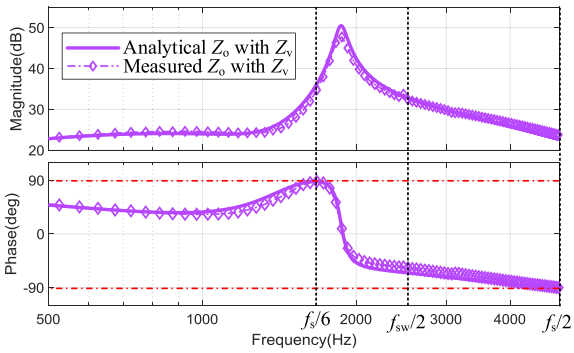

FIGURE 13. Closed-loop output impedance for single-loop control obtained analytically and by frequency scan with $f_{sw} = 0.5f_s$ and $T_d = 1.5T_s$.

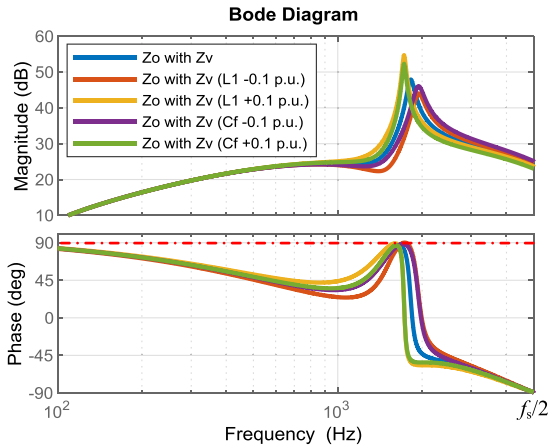

FIGURE 12. Closed-loop output impedance with virtual impedance control Z_v for single-loop control considering LC parameter variation.

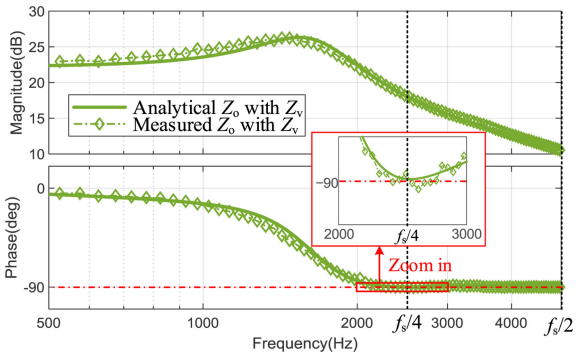

FIGURE 14. Closed-loop output impedance for dual-loop PR&H_v control obtained analytically and by frequency scan with $f_{sw} = f_s$ and $T_d = T_s$.

operating points. Also, the filters may wear out during lifetime. These variations of filter parameters could affect the passivity, which is thus discussed further. The parameter variation in LC filters can mainly come from the equivalent series resistance (ESR) and the deviation in inductance or capacitance from the nominal values, e.g,. due to aging.

Theoretically, R_o reaches zero critically at $f_s/6$, which is the worst point for passivity. If any ESR is considered in the LC filter, it dissipates energy, which always provides more active damping. Therefore, the ESR does not threaten the passivity design.

As for the inductance or capacitance error, it is inevitable in real applications, which can lead to a slight shift of the LC resonant frequency. The impacts of the inductance and capacitance variation on the impedance passivity are investigated further. The parameter variations of ± 0.1 p.u. on L_1 and C_f are considered, and an ESR of 0.1 Ω in L_1 is considered at the same time. Fig. 12 shows the VSC output impedances with virtual impedance control for the single-loop control as an example. The control parameters are designed based on nominal values of the LC filter, while the impedances are calculated considering the LC parameter variation.

The ESR effect on passivity can be seen from the blue line, where the phase of Z_o does not reach to $+90°$ at $f_s/6$, implying a better passivity. Considering the parameter variation of L_1 and C_f, it is found that the passivity is slightly worse, since the phase response near $f_s/6$ gets closer to or even exceeds $+90°$. The variation of $\pm$ 0.1 p.u. on L_1 or C_f leads to the same frequency shift of f_{LC}, but the passivity change is more sensitive to the variation of L_1, since the passivity impacted by the L_1 variation is worse than that impacted by C_f variation. However, due to the active damping provided by the ESRs in the circuit, the passivity-based virtual impedance design can tolerate the LC parameter variation to some extent, as seen from Fig. 12 that the passivity is almost guaranteed even with the LC parameter variation.

2) APPLICABILITY OF PASSIVITY-BASED CONTROL

The previous analysis is based on the assumptions that $f_{sw} = f_s$ and $T_d = 1.5T_s$. The proposed passivity-based control is also applicable when $f_{sw} \neq f_s$ or $T_d \neq 1.5T_s$.

Two more cases are studied for the validation of the proposed control [54]. Fig. 13 shows the frequency-scanned impedance with $f_{sw} = 0.5f_s = 5$ kHz and $T_d = 1.5T_s$ for the single-loop control, where the sampling frequency is selected twice as the switching frequency and the double PWM update is considered within a switching period. Fig. 14 shows the

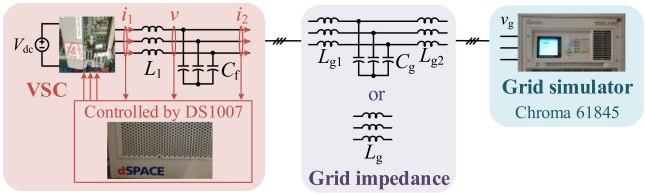

FIGURE 15. Experimental setup for grid-connected VSC for stability analysis.

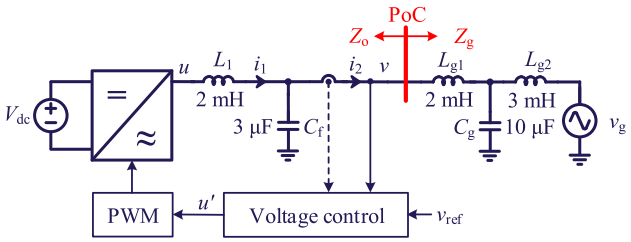

FIGURE 16. Grid-connected VSC through a resonant grid impedance for stability analysis of single-loop control.

result when $f_{sw} = f_s = 10$ kHz and $T_d = T_s$ for the dual-loop PR&H_v control, where the critical frequency becomes $f_s/4$. This case can be realized by shifting the sampling instant toward the PWM update instant in order to reduce the calculation delay as $0.5T_s$ [55]. Then with the PWM delay of $0.5T_s$ considered, the total delay is reduced as one sampling period. In both cases, it can be seen that the passivity can be well designed till half of the sampling frequency.

V. STABILITY VALIDATION

In this section, the passivity analysis is validated by the impedance-based stability analysis [56] and experimental tests on a grid-connected, voltage-controlled VSC.

Fig. 15 shows the experimental setup. A grid simulator, Chroma 61845, is utilized to emulate the ideal grid. A three-phase VSC with LC filter is controlled by DS1007 as a voltage source, which is connected to the grid through the grid impedances. The switching and sampling frequencies are selected as 10 kHz. Two cases with different grid impedances are studied for the stability analysis of single-loop control and dual-loop control, respectively.

A. SINGLE-LOOP CONTROL

It is found from Fig. 7 and Fig. 8 that Z_o has an inductive behavior in the low-frequency range with $-R$, which can lead to harmonic oscillations when the VSC interacts with another electrical system that has a capacitive impedance. Hence, a resonant grid impedance is tested. The system configuration and nominal values of the passive components are shown in Fig. 16.

The high-frequency I-dominant voltage controller is utilized, which allows for the passivity-based design by virtual impedance. The VSC output impedance Z_o and the grid impedance Z_g seen at the point of connection (PoC) are plotted

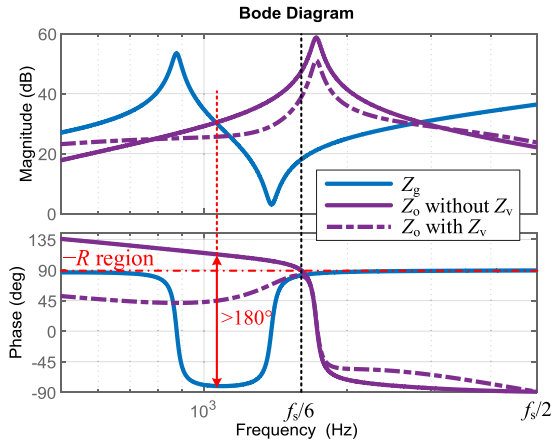

FIGURE 17. Impedance-based stability analysis for single-loop control without and with the virtual impedance control.

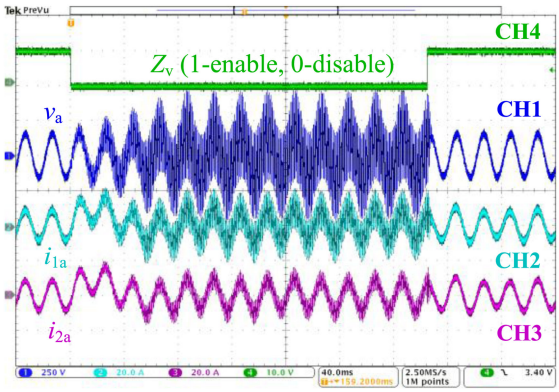

FIGURE 18. Experimental results for single-loop control without and with the virtual impedance control.

in Fig. 17. The VSC controller design is based on the nominal values of the LC filter, which are the same as given in Table 2. The impedance Bode plots are calculated based on actual values of all the passive components in the experiments, including their ESRs (around 0.4 Ω for each inductor), which can be tested in advance by a network analyzer. The major difference is that all the inductors have an actual inductance 0.1 p.u. larger than the nominal values. It can be seen without the virtual impedance control, the non-passivity of Z_o makes the phase difference between Z_o and Z_g to exceed 180° at their impedance-magnitude crossover frequency, which indicates instability according to the Nyquist stability criterion. In contrast, the $-R$ can be eliminated till $f_s/2$ by the virtual impedance control, and thus the system is stabilized.

The experimental results are shown in Fig. 18. The channels CH1, CH2, and CH3 show the capacitor voltage, the inductor current, and the output current, respectively, for the phase-a. The channel CH4 shows the Enable signal for the virtual impedance control. With the virtual impedance control disabled, the system becomes unstable, which verifies the impedance-based stability analysis in Fig. 17.

TABLE 4. Controller Evaluation For Passivity Analysis and Design of Voltage-Controlled VSCs

Control Scheme	Voltage controller synthesis	$-R$ region	Passivity-based design by virtual impedance (till $f_s/2$)
Single-loop control	G_v: PR	$f \in (0, f_{cR})$ $f_{cR} > f_c$	Not applicable
	G_v: R, PR-I, or IR (high-frequency I-dominant)	$f \in (0, f_c)$	$Z_v = \dfrac{K_I L_1}{1-\omega_c^2 L_1 C_f} > 0$
Dual-loop control	H_v=0, G_v: PR	$f \in (f_{cR}, f_s/2)$ $f_{cR} < f_c$	Not applicable
	H_v=0, G_v: R, PR-I, or IR (high-frequency I-dominant)	$f \in (f_c, f_s/2)$	$Z_v = \dfrac{1-K_I L_1}{\omega_c^2 L_1 C_f - 1} > 0$
	$H_v = K_{pi}K_{pv}$ G_v: PR	$f \in (f_c, f_s/2)$	

Notes: f_c (ω_c)– critical frequency (angular frequency) that changes the sign of $\cos(\omega T_d)$, i.e., $f_c = 1/(4T_d)$; f_{cR} – critical frequency that changes the sign of R_o; K_I – equivalent high-frequency integral gain of the voltage controller.

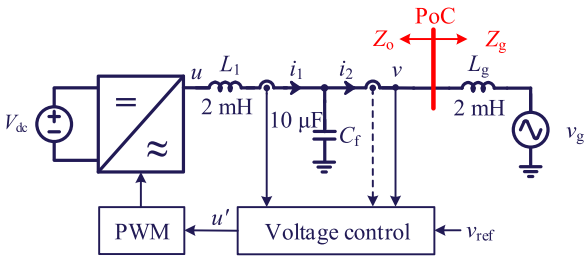

FIGURE 19. Grid-connected VSC through an inductive grid impedance for stability analysis of dual-loop control.

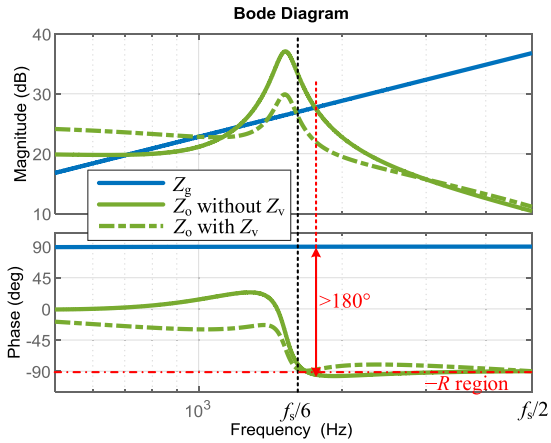

FIGURE 20. Impedance-based stability analysis for PR&H_v dual-loop control without and with the virtual impedance control.

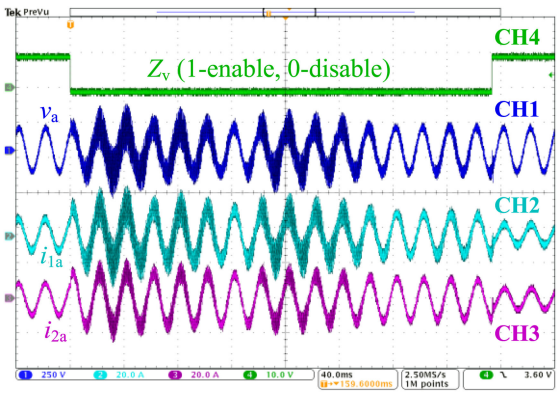

FIGURE 21. Experimental results for PR&H_v dual-loop control without and with the virtual impedance control.

B. DUAL-LOOP CONTROL

For the dual-loop control, Z_o has a capacitive behavior in the high-frequency range with $-R$, which thus can lead to harmonic instability when the VSC interacts with another system that has an inductive impedance. Hence, an inductive grid impedance is tested for the stability validation. Fig. 19 shows the system configuration and circuit parameters with nominal values.

The passivity for the dual-loop control is validated based on the PR&H_v control. The frequency responses of the grid impedance and the VSC impedance are plotted in Fig. 20. It is seen that the system is unstable without virtual impedance control, since the phase difference is larger than 180° at the impedance magnitude crossover frequency. This instability can be prevented by the virtual impedance control based on the design of $K_{pi}K_{pv} = H_v$ as discussed in Section IV. Experimental results are provided in Fig. 21, which also verifies the stability analysis.

VI. CONCLUSION

This paper studies the passivity-based controller design for voltage-controlled VSCs. Both the single-loop and dual-loop voltage control schemes have been discussed. It has been revealed that the control performance can be significantly

enhanced by the high-frequency I-dominant controllers. The major findings with the passivity analysis and control design for different control schemes are summarized in Table 4:

a) The explicit $-R$ regions have been compared. It is seen that the $-R$ appears in the low-frequency range for the single-loop control, and appears in the high-frequency till $f_s/2$ for the dual-loop control. The critical frequency $f_c = 1/(4T_d)$, which is determined by time delay, plays an important role in the width of the $-R$ region.
b) The virtual impedance controller gain, which is co-designed with the voltage controllers to realize the passivity till half of the sampling frequency, has been analytically derived. The value of Z_v is determined by the LC filter, the time delay, and the equivalent high-frequency integral gain of the voltage controller.

Experimental tests have validated the effectiveness of the passivity-based design. Compared with the exiting methods, the proposed method does not need much parameter tuning efforts and applies well to various voltage control schemes.

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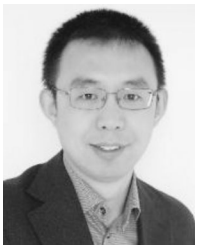

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