IEEE Open Journal of the
Industrial Electronics Society

Received 4 February 2020; revised 3 April 2020; accepted 8 May 2020. Date of publication 11 May 2020;
date of current version 12 June 2020. The review of this paper was arranged by Associate Editor Hong Li.

Digital Object Identifier 10.1109/OJIES.2020.2994142

A Modified Higher Operational Duty Phase Shifted Full Bridge Converter for Reduced Circulation Current

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ABSTRACT Besides many advantages, the reduction in the operational duty of a traditional phase shifted full converter limits its scope in applications where a wide range of input voltage is the main requirement. Operation with low duty cycle extends freewheeling interval, which results in degraded performance such as more circulating current, increased conduction loss in power devices, narrow range of zero voltage switching and increased EMI. To overcome these drawbacks, this work suggests a modified phase shifted full bridge converter that keeps the operational duty of the converter high for a wide range of input voltage. This cuts the freewheeling interval and improves performance. The proposed converter consists of four low profile transformers having a structure of reconfigurable interconnections. There are two distinct reconfigurable operational modes, a low-gain mode and a high-gain mode, which can be adopted following the variation in line voltage. The proposed work is validated in LTspice simulation and hardware characterization for a wide range of input voltage 100–400 V_{dc}/ 12 V_{out} and up to the load power of 1.2 kW.

INDEX TERMS Wide range converter, low freewheeling, reduced circulation current, high duty cycle, ZVS, resonant converter, multiple transformers, series transformers, PSFB converter, reconfigurable converter.

I. INTRODUCTION

The phase shifted full bridge (PSFB) converter is a promising choice of the power electronics industry for high to medium power applications [1]–[4] due to its attractive features such as zero voltage switching (ZVS), simplified design structure, high conversion ratio, and low electromagnetic interference. Typically, the operational duty of power converters is set to maximum at the minimum level of the input voltage. Therefore, the reduced duty cycle at high input voltage degrades performance of the converter. Similarly, when it comes to extending the operational range, PSFB topology also has few drawbacks [5]–[8] such as loss of duty cycle, extended freewheeling period, circulation current, narrow range of ZVS operation and high voltage spikes. As a comparison, extended freewheeling period due to reduced duty cycle contributes more in the degradation of the performance. As explained in Fig. 1(a), when the supply voltage increases, to keep the output voltage constant it is required to decrease the duty cycle. As a result, circulation current flows for a longer period. The concept of the flow of circulation current is given as Appendix-A. The increased circulation current results in more conduction losses, and more overshoot/ ringing occur on the secondary devices.

In [5], [9], [10], the circulating current is reduced by the addition of an auxiliary circuit. This resets the circulating current down to zero during the freewheeling period. On the other hand, the lagging leg enters into hard switching. To overcome this, authors [10] propose zero current switching for the lagging leg by the replacement of MOSFETs with IGBTs. However, the tail current associated with IGBTs becomes the main constraint in increasing the switching frequency of the converters [11]. This makes the approach less feasible for today's space constraint applications. In [12], [13], adopting a control strategy according to the load condition minimize the circulation current loss only under light load condition; moreover, it makes the design more complex. The addition of

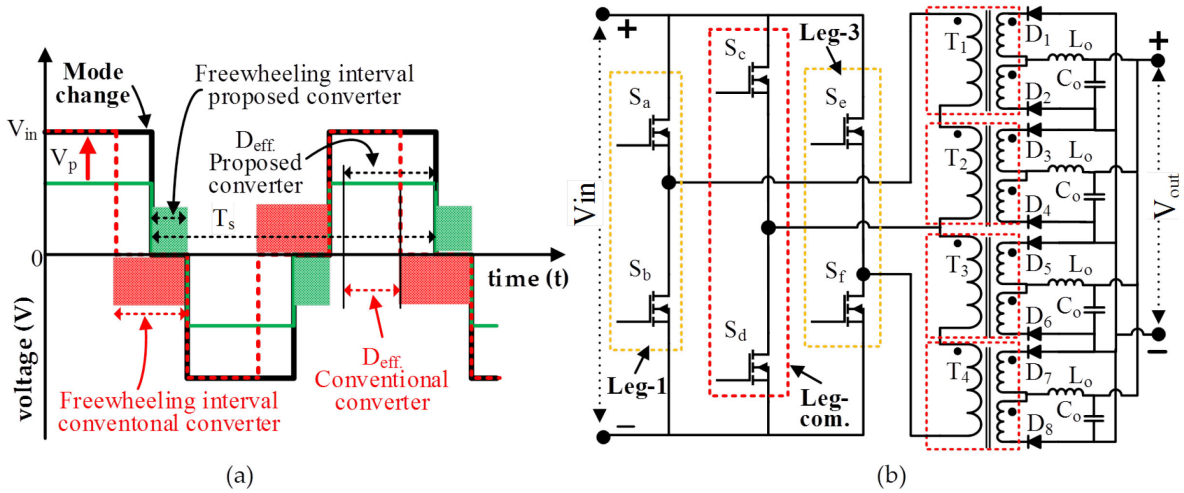

FIGURE 1. (a) Explanation of increase in the freewheeling interval, operation with low duty ratio against the operation with high duty ratio, (b) Simplified diagram of the proposed converter showing additional leg and transformers.

a boost capacitor in [14] reduces the conduction loss during the freewheeling interval; however, it narrows the range of ZVS.

The problem of circulation current can be minimized by keeping the duty cycle high and thus eliminating the freewheeling interval. This can be accomplished by adjusting the effective dc gain with the variation in input voltage. The authors [15], [16] varies the dc gain by adopting the tap-winding technique to reduce the size of link capacitors. However, the concepts have only been investigated for the hold-up interval of 20 ms, which limits its scope. This work presents a modified three-leg PSFB solution, which not only cuts the freewheeling period but can also be implemented in a broader range of applications.

Fig. 1(b), shows the schematic of the proposed converter. The proposed converter keeps the duty ratio high that allows the converter to operate for a wide range of input voltage while keeping the performance stable. In addition to the traditional leading and lagging leg, a common leg along with a configuration of four transformers have been introduced. This arrangement changes the effective dc gain as high or low. Depending on the operating condition, the effective gain can be configured either in high-gain mode or in low-gain mode. The proposed work has multiple advantages, e.g.,

1) The proposed converter keeps the operational duty high and shortens the freewheeling interval, the reduced circulation current improves conduction loss, overshoots/ringing resulting in better EMI.
2) Operation with high duty cycle reduces ripple current on the output filter inductor which cuts its size and cost.
3) The series configuration of transformers reduces the applied volt-second by the number of transformers; the total transformer loss will spread into four transformers. As a result, less heat management effort is required [17].
4) Since the domain wall motion in ferrite material is directly dependent on the rate of change of magnetic flux dB/dt, therefore, operation with a high duty cycle also reduces core loss [18].
5) The proposed converter works on the principle of traditional phase shifted full bridge converter, it simplifies the implementation for a range of applications.

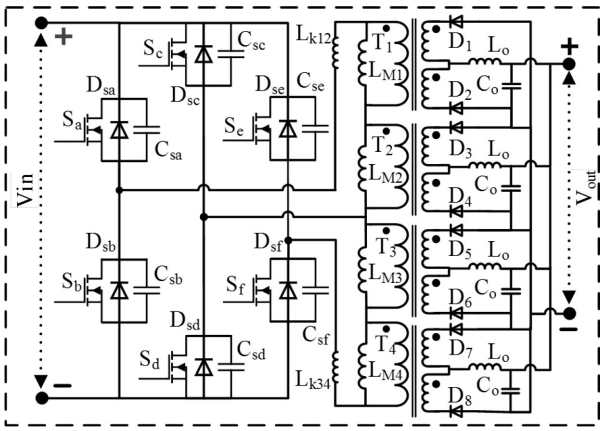

FIGURE 2. Block diagram of the converter showing key circuit elements of the circuit.

II. WORKING AND DESIGN CONSIDERATIONS OF THE PROPOSED CONVERTER

This section explains the working and design considerations of the proposed converter.

A. CIRCUIT DESCRIPTION

The simplified block diagram of the proposed converter along with the key circuit components is shown in Fig. 2. It consists of six primary switching devices $S_a - S_f$, which are arranged in a way to make it three-leg converter. Similar to the conventional PSFB converter, the devices S_a and S_b make the leading leg, and the devices S_e and S_f make the lagging

leg. In between them, there is a common leg consisting of devices S_c and S_d. The diodes $D_{sa} - D_{sf}$ represent the body diodes of the power devices $S_a - S_f$ respectively. Similarly, the capacitors $C_{sa} - C_{sf}$ are the drain to source output capacitance of devices $S_a - S_f$. As seen, the converter contains four center-tapped transformers shown as T_1-T_4. Each transformer consists of the same number of primary turn N_P and secondary turns N_S. The primary windings are connected in series, whereas, the secondary windings are connected in parallel. The series connection on the primary side ensures the equal flow of current through all four transformers. Similarly, the parallel connection on the secondary side equally shares the load current [17]. Although, the concept works with two transformers, however for the prototype evaluation four transformers are being utilized to reduce required current ratings for the secondary side elements such as winding, rectifiers, inductors and capacitors. The inductors L_{k12} and L_{k34} are the sums of the intrinsic leakage inductance of transformers T_1-T_2 and the transformers T_3-T_4 respectively. The diodes D_1-D_8 are the rectifiers connected with the center-tapped secondary windings of the transformers. The rectified voltage is filtered through a separate combination of inductor L_o and capacitor C_o for each transformer.

The proposed converter operates in two modes, the low-gain mode and the high-gain mode. In low-gain mode, the converter configures primary winding of all four transformers in series, while in high-gain mode, it configures a pair of two series transformers in parallel i.e., a series configuration of the transformers T_1-T_2 and T_3-T_4 become parallel. In low-gain mode, the common leg remains neutral; the phase shifted switching control is implemented only through the leading leg and the lagging leg. In high-gain mode, the second leg operates out of phase with both the first and the third leg. The common leg acts as the lagging leg while the other two as the leading legs. For verification of the concept, a simplified line sense/ voltage mode control strategy is adopted for the switchover between the operational modes and regulation of the output voltage.

B. TRANSFORMER CONSIDERATIONS

The proposed converter comprises of four transformers. The interconnection of transformers configures differently in both modes. The equivalent model of the transformer for the operation in each mode is shown in Fig. 3. The change in transformer interconnection affects only the primary section, secondary windings remain connected in parallel. The equivalent parameters of each transformer also act differently in each mode. In low-gain mode, the primary winding of all the transformers are configured in series, this equally divides the input voltage among the four transformers, therefore, the input voltage becomes $V_{in} = V_{t1} + V_{t2} + V_{t3} + V_{t4}$. The effective turn ratio n_L of the converter in low-gain mode can be defined as

$$n_L = \frac{V_{in}/4}{V_s} = \frac{N_p}{N_s} \tag{1}$$

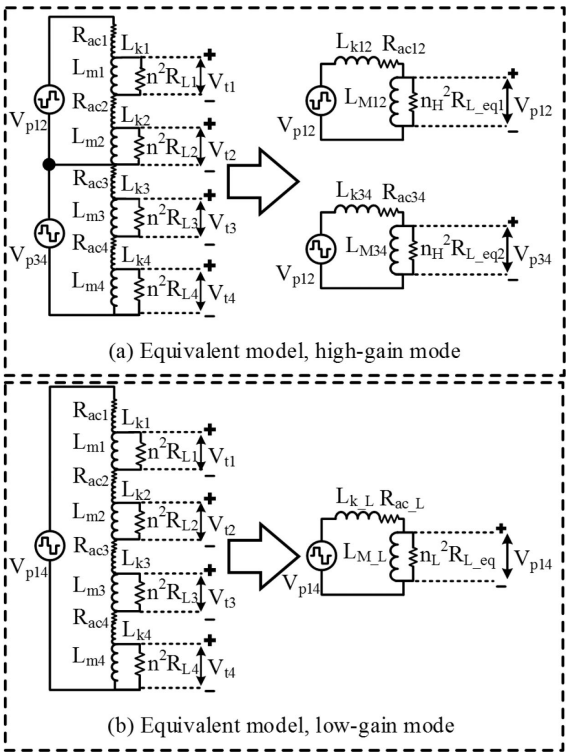

FIGURE 3. Equivalent model of key parameters of the proposed configuration of transformers: (a) high-gain mode, (b) low-gain mode.

Unlike the conventional converter, here the voltage stress on each transformer is $V_{in}/4$. This reduces the volt-sec per transformer, consequently the reduced core loss. Similarly, the total magnetizing and the leakage inductance are the sum of individual inductances, i.e., $L_{M\_L} = L_{m1} + L_{m2} + L_{m3} + L_{m4}$ and $L_{k\_L} = L_{k1} + L_{k2} + L_{k3} + L_{k4}$. The equivalent ac resistance R_{ac}, of the primary winding, is $R_{ac\_L} = R_{ac1} + R_{ac2} + R_{ac3} + R_{ac4}$.

When the converter is configured in high-gain mode, it connects the transformers as a combination of series/parallel voltage divider, and the input voltage is equivalent to $V_{in} = (V_{t1} + V_{t2}) \parallel (V_{t3} + V_{t4})$. The effective turn ratio n_H of the converter in high-gain mode can be written as

$$n_H = \frac{V_{in}/2}{V_s} = \frac{N_p}{N_s} \tag{2}$$

In this mode, primary current follows two opposite paths, one is $T_1 + T_2$ and the other is $T_3 + T_4$. The equivalent magnetizing inductance and the leakage inductance is the sum of the inductance seen by each path. The equivalent magnetizing inductance of the circuit becomes as $L_{M\_H} = (L_{m1} + L_{m2}) \parallel (L_{m3} + L_{m4})$. Similarly, the equivalent resonance inductance is $L_{k\_H} = L_{k12} \parallel L_{k34}$, and equivalent ac resistance is $R_{ac\_H} = (R_{ac1} + R_{ac2}) \parallel (R_{ac3} + R_{ac4})$.

C. WORKING PRINCIPLE OF THE CONVERTER

The proposed converter operates differently in each mode. The working principle of each mode will also be discussed

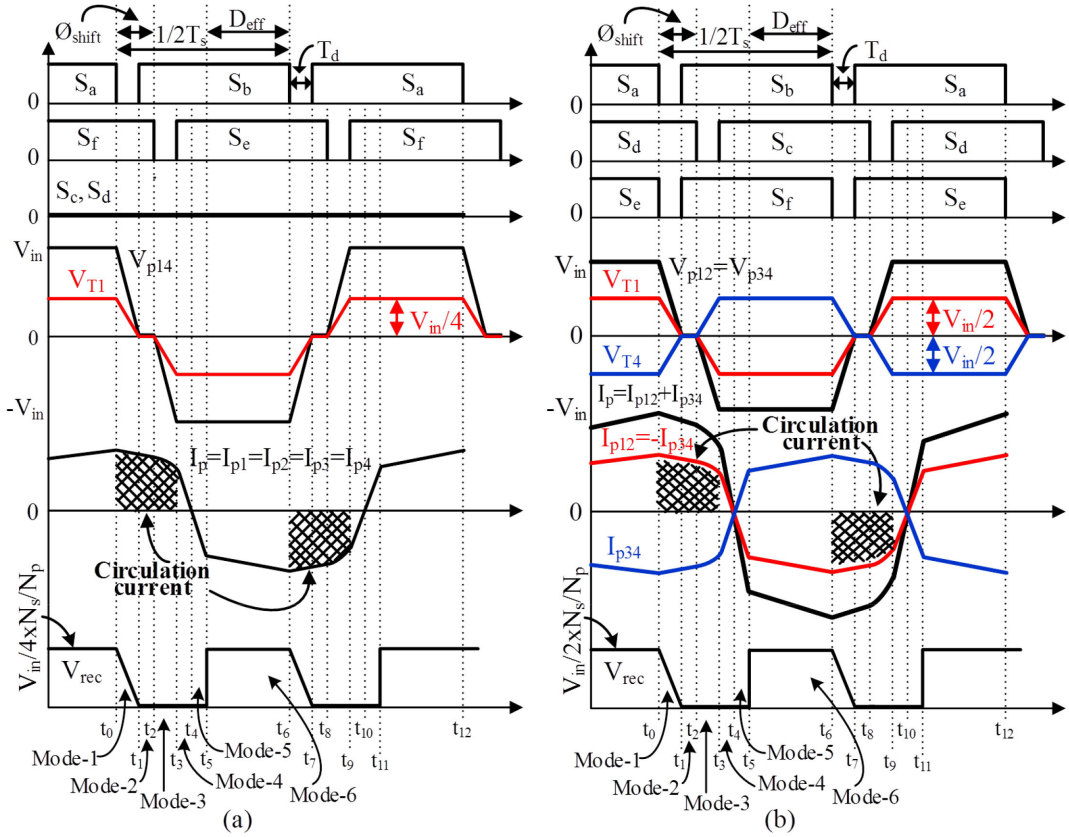

FIGURE 4. Control signal and key operational waveforms: (a) low-gain mode, (b) high-gain mode.

separately. In low-gain mode, the power devices $S_a - S_b$, and $S_e - S_f$ contribute to the transfer of power from the source to the load. The sum of the leakage inductance $L_{k12} + L_{k34}$ together with the output capacitance and the body diodes of the respective power devices arrange to achieve zero voltage switching of the devices. In high-gain mode, all primary devices $S_a - S_f$ take part in delivering the power from source to the load. In this mode, ZVS is achieved by using the leakage inductance L_{k12}, L_{k34}, together with the respective output capacitance and body diode. On the secondary side, all rectifiers D_1-D_8 and filtering components contribute to both modes. The timing diagram along with key operational waveforms of both the modes have been shown separately in Fig. 4. To make the working principle simple, and to estimate the gain of the converter, the following assumptions have been made [19]–[23].

1) All the power devices $S_a - S_f$ are ideal.
2) The drain-source output capacitance of all the power devices is equal, i.e., $C_{sa} = C_{sb} = C_{sc} = C_{sd} = C_{se} = C_{sf}$.
3) The body diodes have the same characteristics.
4) All the transformers are alike, i.e., all four transformers have the same number of primary/secondary N_p/N_s turns, the magnetizing inductances are equal, $L_{m1} = L_{m2} = L_{m3} = L_{m4}$, each transformer has the same amount of leakage inductance, $L_{k12} = L_{k34}$
5) The characteristics of all of the rectifiers D_1-D_8 are the same.
6) The filter elements L_{o_T}, and C_{o_T} are referred to as the total output filter inductor and capacitor and are sufficient to maintain the output voltage constant.

1) ZERO VOLTAGE SWITCHING—LOW-GAIN MODE

In low-gain mode, the converter configures the primary winding of all four transformers in series. As shown in the waveform Fig. 4(a), the devices on the common leg S_c and S_d remain OFF, and the phase shifted control is applied to the outer two legs. The power is transferred through a diagonal pair of devices $S_a - S_b$, and $S_e - S_f$ on the primary side and through rectifier D_1-D_8 on the secondary side. The bridge voltage V_{p14} is divided among four transformers. Therefore, the input voltage on the primary winding of each transformer is $V_{in}/4$, and the same amount of primary current I_p, flows through each transformer. To make the explanation more clear, a half-switching cycle is divided into six distinct states. The operational status of the key circuit components in each mode is shown in Fig. 5.

a) Mode 1: This mode starts when the power device S_a turns OFF at $t = t_o$. The primary current continues to flow through capacitor C_{sa}. The flow of primary current charges and discharges capacitors C_{sa} and C_{sb} respectively. Since the total

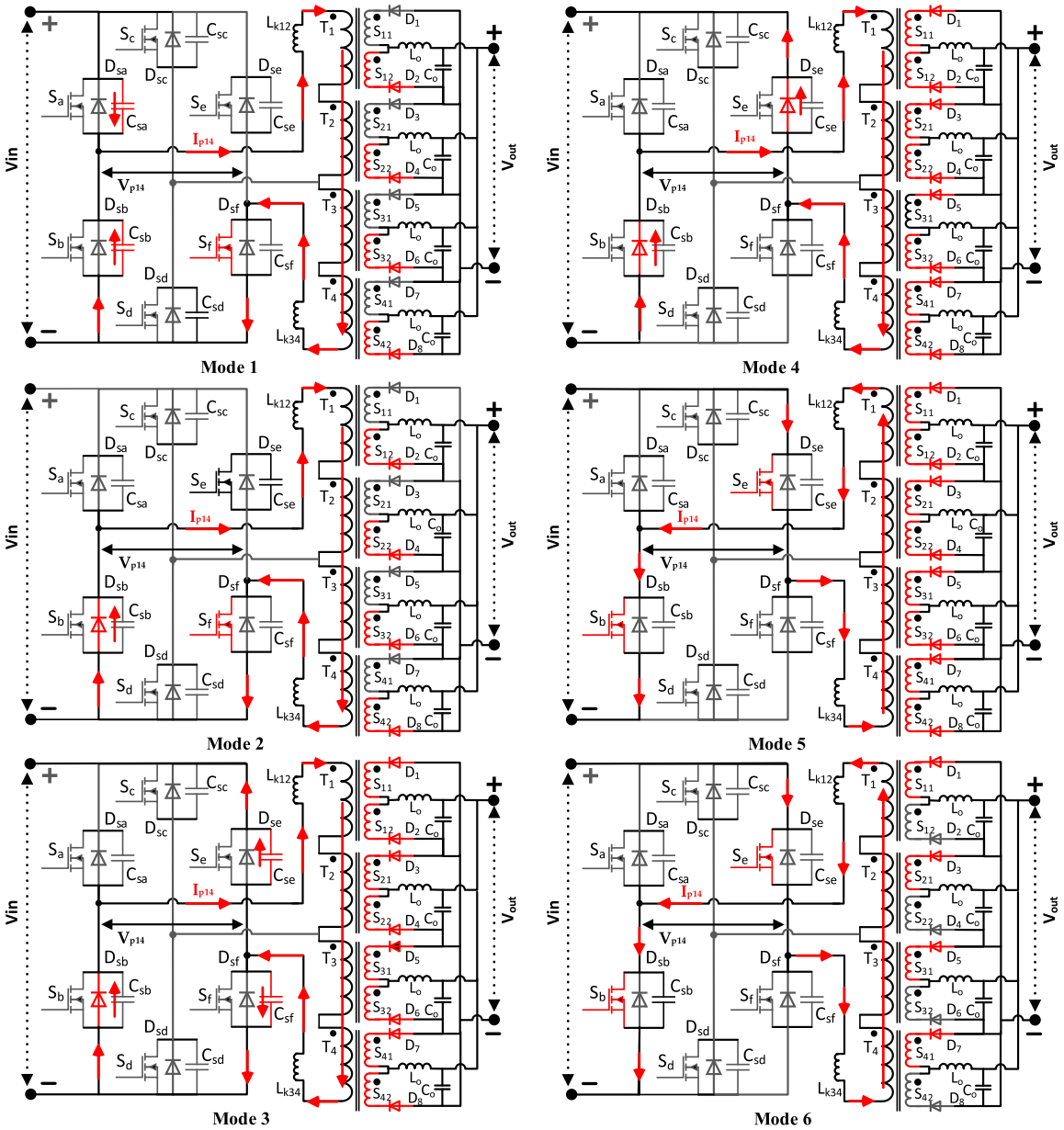

FIGURE 5. Low-gain mode, status of the key circuit elements during the operation in modes 1–6.

output filter inductance L_{o_T} reflects to the primary side and is in series with the equivalent leakage inductor L_{k_L}, the primary current I_{p14} continues to flow [22], [24]. The energy stored in the leakage inductors circulates in this mode, therefore, the primary current $I_p(t_1) = I_p(t_0)$ remains nearly the same during this interval. At the end of mode 1, the voltage across the capacitor C_{sa} rises to the input voltage V_{in}, and the voltage across C_{sb} decays to zero voltage, forcing the body diode D_{sb} to conduct.

b) Mode 2: The capacitor C_{sb} completely discharges at $t = t_1$, diode D_{sb} conduct and clamps the voltage across C_{sb} at zero and thus arrange zero voltage turn ON for the device S_b. The dead time between the devices of the leading leg S_a and S_b is of significant importance to ensure complete zero voltage switching. The dead time must be larger [25] than the time duration of mode 1 i.e.,

$$T_d\,(lead) > \frac{2C_{AB}}{I_{p14}\,(t_1)} V_{p14} \tag{3}$$

where T_d is the dead time between devices of the leading leg and C_{AB} is combined output capacitance of these devices. During charging and discharging of capacitors C_{sa} and C_{sb}, the primary current drops to $I_{p14}(t_1) = \frac{1}{n_L} I_{Lo\_T}$, where I_{Lo_T} is the total load current.

c) Mode 3: At time t_2, the bridge voltage V_{p14} drops to zero voltage. The primary device S_f turns OFF at zero voltage and the primary current starts charging and discharging capacitors C_{sf} and C_{se} respectively. As the bridge voltage reaches

$V_{p14} = -V_{Csf}$, the primary current I_{p14} starts to decay. As a result, the current flowing in secondary rectifiers D_2, D_4, D_6 and D_8 decays. To overcome this shortfall, the other secondary rectifiers D_1, D_3, D_5, and D_7 also start conducting, clamp all secondary windings to zero voltage. The full bridge voltage V_{p14} appears on the sum of leakage inductors L_{k_L}, which resonates along with C_{sf} and C_{se}. The primary current I_{p14} can be expressed as

$$I_{p14}\,(mode3) = I_{p14(t2)} \cos \frac{1}{\sqrt{2L_{k\_L}C_{EF}}}\,(t - t_2) \tag{4}$$

The capacitance C_{EF} is the sum of the output capacitance of both devices S_e and S_f. At the end of this mode, the voltage across capacitor C_{sf} reaches the input voltage V_{in} and the voltage across C_{se} drops to zero voltage, which turns the body diode D_{se} ON. The duration of this mode can be determined as

$$T\,(mode3) = \sqrt{2L_{k\_L}C_{EF}}\,\sin^{-1}\frac{V_{p14}}{\left(\sqrt{\frac{L_{k\_L}}{2C_{EF}}}\right) I_{p14(t2)}} \tag{5}$$

d) Mode 4: At time t_3, after capacitor C_{se} is completely discharged, body diode D_{se} clamps the voltage across the power device S_e at zero voltage and makes it ready to turn ON at zero voltage. To achieve zero voltage switching, the dead time between devices of the lagging leg S_e and S_f must be greater than the time interval of mode 3, i.e.,

$$T_d\ \ (lag) > T\,(mode3) \tag{6}$$

In this mode, the body diode of both the diagonal devices S_b and S_e start to conduct and the energy stored in the equivalent leakage inductor L_{k_L} is regenerated to the input source. On the secondary side, all rectifiers D_1-D_8 continue to conduct, and I_{p14} decays in equivalent leakage inductor. At time t_4, the primary current crosses the zero line, the decay in I_{p14} during this mode can be expressed as

$$I_{p14}\ \ (t) = I_{p14}\,(t_3) - \frac{V_{p14}}{L_{k\_L}}\,(t - t_3) \tag{7}$$

e) Mode 5: At the start of this mode, the primary current starts building up linearly in the reverse direction through devices S_b and S_e. As the primary current I_{p14} is not sufficient to power the load, all rectifiers D_1-D_8 remain ON. The full input voltage is impressed on the equivalent leakage inductor, which increases the input current in the reverse direction. As soon as the primary current reaches to the value equal to the reflected load current, the rectifies D_2, D_4, D_6, and D_8 turns OFF, while the rectifiers correspond to the second set of secondary windings i.e., D_1, D_3, D_5 , and D_7 continue to conduct. After this mode, the load is powered from the source.
f) Mode 6: This is the power delivery mode. The power is delivered from the input source to the load. On the primary side, the devices S_b and S_e conduct, and the equal amount of primary current flows through the primary winding of each transformer. Similarly, on the secondary side, the rectifiers D_1, D_3, D_5 and D_7 along with the corresponding secondary windings of transformers T_1-T_4 conduct to power the load and the output filter capacitor C_o. The primary current I_{p14} can be determined as

$$I_{p14}\,(t) = \left\{\left(\frac{V_{p14} - n_L V_{out}}{L_{m\_L} + L_{k\_L} + (n_L)^2 L_{o\_T}}\,(t - t_5)\right) + I_{Lo\_T}\,(t_5)\,/n_L\right\} \tag{8}$$

The output voltage V_{out} is determined as

$$V_{out\_L} = 2D_{eff}\frac{V_{p14}}{n_L} \tag{9}$$

The effective duty cycle D_{eff} is defined as $D_{eff} = D - (D_{loss} + \varphi_{shift})$, where D is a duty ratio. At the end of this mode, it completes one half-cycle. In the next half-cycle, the same principle applies to achieve ZVS of the other diagonal pair S_a and S_f.

The above discussion infers that PSFB converters deliver actual power to the load only in mode 6. It means that the primary current in the rest of the modes merely circulates within the circuit elements [26]. The only significant duration within this interval is the length of dead time between the devices of the same leg, which is required to ensure zero voltage switching of the devices. Equations (3) and (5) shows that the required dead time is independent of the operational duty cycle. Therefore, the operation with a low duty cycle merely increases the total losses.

2) ZERO VOLTAGE SWITCHING—HIGH-GAIN MODE

To keep the analysis consistent with the previous mode, the discussion follows the same methodology as discussed in the low-gain mode. As shown earlier in Fig. 4(b), the main difference in this mode is that the common leg becomes active, clamps voltage on the common point to V_{in_max} and zero in alternate half cycles. It means that the devices of this leg S_c and S_d turn ON/OFF alternately. This configures pair of series-connected transformers T_1-T_2 and T_3-T_4 in parallel. The voltage and current across each pair is represented as V_{p12}, V_{p34} and I_{p12}, I_{p34} respectively. As seen, the drive signals to the devices of both outer legs are in phase, whereas the common leg acts as out of phase with the others. The working of the converter in this mode is also divided into six distinct modes. Fig. 6 shows the status of key components in each mode. One device from each leg takes part to deliver power from source to the load. In the first half-cycle, a group of devices S_a, S_d, and S_e deliver power to the load, similarly, in the next half-cycle the other group S_b, S_c, and S_f deliver power to the load. On the secondary side, two groups of rectifiers D_1, D_3, D_6, D_8 and D_2, D_4, D_5, D_7 conduct in alternate half-cycles. The flow of primary current through each group of transformers follows the opposite direction. Because of this, alternate secondary windings conduct during the same half-cycle. Similar to the previous mode, all six devices achieve ZVS on the principle of phase shifted full bridge converter, however as discussed earlier, circuit elements act differently in both mode. The following is a brief analysis of each mode.

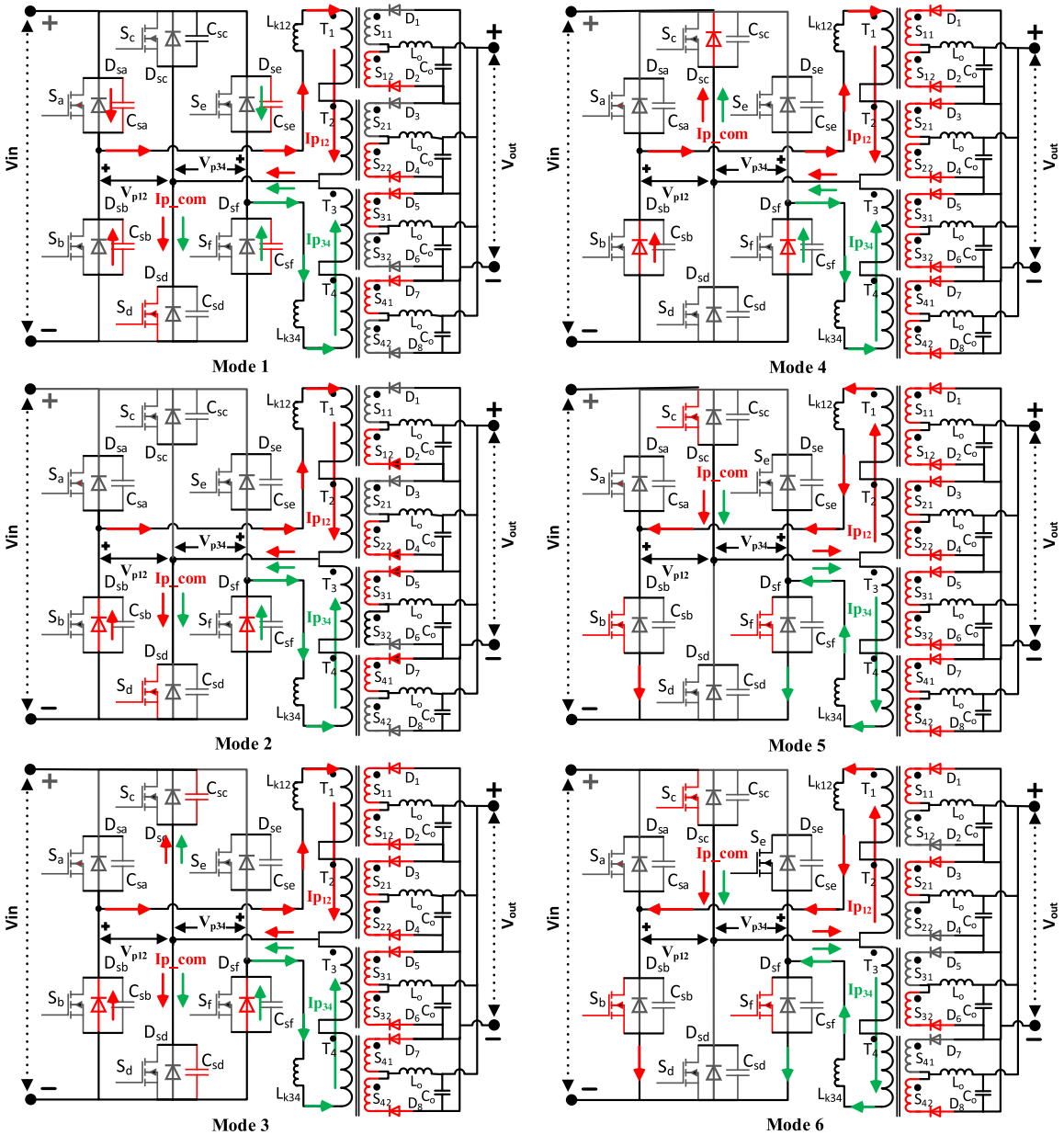

FIGURE 6. **High-gain mode, status of the key circuit elements during the operation in modes 1–6.**

a) Mode 1-2: Mode-1 starts when parallel devices S_a and S_e turn OFF at t = t_0. Both primary current I_{p12} and I_{p34} continue to flow through capacitors C_{sa} and C_{se} respectively. This charges capacitors C_{sa} and C_{se}, and discharges the opposite device capacitors C_{sb} and C_{sf}. The moment C_{sb} and C_{sf}, discharge completely, the anti-parallel body diodes D_{sb} and D_{sf} start to conduct and clamps the drain-source voltage of the respective device to zero, this prepares both devices to turn ON with zero voltage switching. To ensure zero voltage switching of both leading legs, the dead time between the switching of the opposite devices should be greater than the expressions given in (10) and (11)

$$T_d\,(lead1) \;>\; \frac{2C_{AB}}{I_{p12}\,(t_1)}V_{p12} \tag{10}$$

$$T_d\,(lead2) \;>\; \frac{2C_{EF}}{I_{p34}\,(t_1)}V_{p34} \tag{11}$$

The right-hand sides of (10) and (11) are the duration of mode 1. At the end of mode-2, I_{p12} and I_{p34} drops and are equal to the reflected load current.

b) Mode 3-4: The bridge voltage V_{p12} and V_{p34} across the primary windings is zero at time t_2. The device S_d turns OFF at zero voltage and the sum of both primary currents I_{p12} and I_{p34} contribute to charge and discharge the capacitors C_{sd} and C_{sc} respectively. As soon as the secondary current decays below output inductor current, there becomes shortfall of current on the secondary side, therefore the other non-conducting rectifiers start conducting, which in turn short-circuit all secondary windings. Thus the voltage V_{p12} and V_{p34} are applied on the

leakage inductor L_{k12} and L_{k34} respectively. The current I_{p_com} in the common leg is,

$$I_{p\_com} = I_{p\_com(t_2)} \cos \frac{1}{\sqrt{2L_{k\_H}C_{CD}}} (t - t_2) \tag{12}$$

At time t_3, the capacitor C_{sc} completely discharges, the body diode D_{sc} clamps drain-source voltage of the device S_c down to zero. Therefore, the device S_c is ready to turn ON observing ZVS. To achieve ZVS, the dead time between the devices of the lagging leg S_c and S_d should be

$$T_d\,(lagging) > \sqrt{2L_{k\_H}C_{CD}} \sin^{-1} \frac{V_{in}}{\left(\sqrt{\frac{L_{k\_H}}{2C_{CD}}}\right) I_{p(t2)}} \tag{13}$$

The right-hand side of (13) is the duration of mode 3. In mode-4, only the body diodes of S_c, S_b, and S_f conduct, whereas on the secondary side, all rectifiers D_1-D_8 continue to conduct, keeping the secondary windings shorted. The current in both primary and secondary windings continues to decay. At t_4, the current I_{p12} and I_{p34} start to decay below zero, the body diodes D_{sc}, D_{sb} and D_{sf} turn OFF naturally. Both primary currents in mode 4 can be expressed as

$$I_{p12}\,(t) = I_{p12}\,(t_3) - \frac{V_{p12}}{L_{k12}} (t - t_3) \tag{14}$$

$$I_{p34}\,(t) = I_{p34}\,(t_3) - \frac{V_{p34}}{L_{k34}} (t - t_3) \tag{15}$$

c) Mode 5-6: In mode 5, I_{p12} and I_{p34} continue to build up in reverse direction through leakage inductors L_{k12} and L_{k34} respectively. The slope of this rise is a function of input voltage and the respective leakage inductor. As the primary current I_{p12} and I_{p34} meet the reflected load current, the rectifiers D_2, D_4, D_5 and D_7 turn OFF, while rectifiers D_1, D_3, D_6, and D_8 remain ON. It starts mode 6, which delivers power to the load. The power device S_c in the common leg together with both the diagonal devices S_b and S_f conducts with phase shifted control. The dc output voltage V_{out} is

$$V_{out\_H} = 2D_{eff} \frac{V_{p12}}{n_H} \tag{16}$$

The primary current I_{p12} and I_{p34} is determined as

$$I_{p12}\,(t) = I_{p34}\,(t)$$

$$= \left\{ \left(\frac{V_{p12} - n_H V_{out}}{2L_{m\_H} + 2L_{k\_H} + (n_H)^2 L_{o\_T}} (t - t_5) \right) + I_{Lo\_T}\,(t_5)\,/n_H \right\} \tag{17}$$

The amount of primary current flowing through the device S_c of the common leg is the sum of the current flowing in the other two legs i.e.,

$$I_{p\_com}\,(t) = I_{p12}\,(t_5) + I_{p34}\,(t_5) \tag{18}$$

The ZVS characteristics of the lagging leg are better in high-gain mode. Because of the reduced magnetizing inductance, the primary current is higher as compared to other mode.

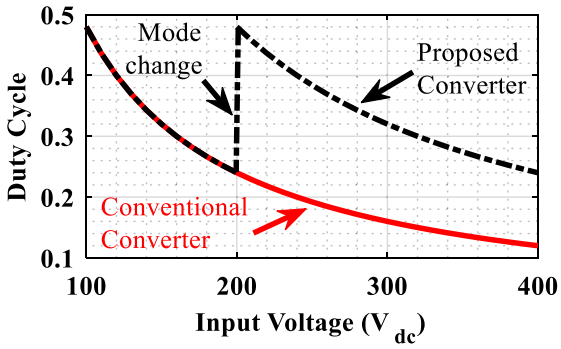

FIGURE 7. Comparison of duty cycle between the proposed and the conventional converter against the variation in the input voltage.

III. CHARACTERISTICS OF THE CONVERTER

A. DC GAIN OF THE CONVERTER

The effective dc voltage gain of the converter depends upon the number of transformers and the interconnection with supply voltage. Based on that, the effective gain differs in both modes. Rewriting (9) and (16), the output voltage of both modes is

$$V_{out\_L} = 2D_{eff} \frac{N_s}{N_p} \left(\frac{V_{in}}{4} \right) \tag{19}$$

$$V_{out\_H} = 2D_{eff} \frac{N_s}{N_p} \left(\frac{V_{in}}{2} \right) \tag{20}$$

The dc gain for each mode can be written as

$$G_{\_L} = \frac{V_{out}}{V_{in}} = \frac{1}{2} \frac{N_s}{N_p} D_{eff} \tag{21}$$

$$G_{\_H} = \frac{V_{out}}{V_{in}} = \frac{N_s}{N_p} D_{eff} \tag{22}$$

Equations (21) and (22) infer that for the same operating conditions, the gain of the converter in high-gain mode is double as much the gain in low-gain mode.

B. SETTING THE RANGE OF OPERATIONAL MODES

Since the gain of the proposed converter possesses different characteristics as compared to a conventional converter, the operational duty also varies differently against the input voltage. As the input voltage increases instead of reducing the duty cycle, the proposed converter can be configured to a low-gain mode where the duty cycle has to set high again to maintain the operating conditions. The operational range of each mode can be optimized depending upon the requirement of the chosen application. For example, the converter can be configured to operate in high-gain mode from V_{in_min} to $1/2V_{in\_max}$, then can be configured to the low-gain mode when the input voltage rises above $1/2V_{in\_max}$.

C. REDUCED CIRCULATION CURRENT

As said, the duty cycle varies differently in the proposed converter. A comparison plot is shown in Fig. 7, for the

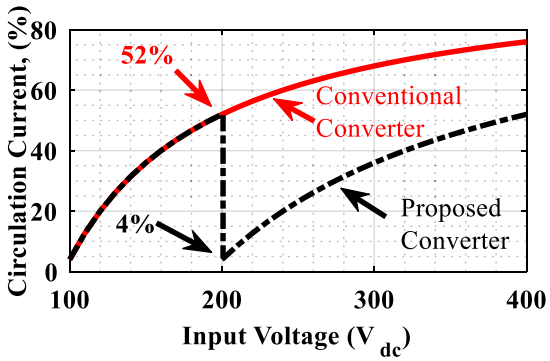

FIGURE 8. Comparison of the percentage length of the flow of circulation current in a half-cycle period for increasing input voltage and constant output voltage.

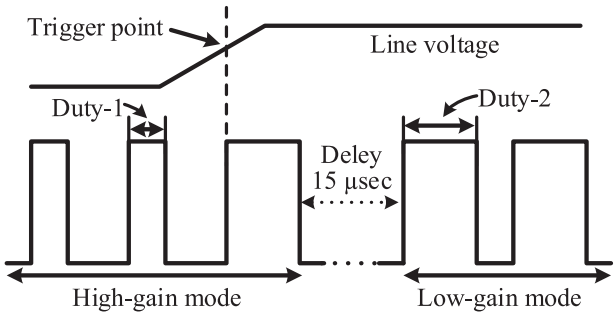

FIGURE 9. Control strategy implemented for the smooth transition of mode switchovers.

normalized operating condition, $N_p/N_s = 1$, and $V_o = 12$ V, and considering the duty cycle maximum at the minimum level of the input voltage. In conventional converters, the duty cycle drops linearly against the input voltage, whereas in the proposed converter it possesses different characteristics. By using the gain switchover characteristics, it operates in the high-gain mode for the input voltage 100–200 V, above 200 V it reconfigures to the low-gain mode and sets the duty cycle high again. As seen, for the increase in input voltage from 100 V to 400 V, the reduction in the duty cycle is 75% in the conventional converter, whereas it is 50% in the proposed converter. The reduced duty cycle extends the freewheeling interval which degrades performance.

As discussed earlier, during this interval, primary current circulates only through the primary devices. This contributes to the increase in conduction losses. Wider is the freewheeling interval the more will be the losses. The comparison of circulation current that flows during the period of one half-cycle is shown in Fig. 8. As seen for the same operating conditions, the circulation current flows for less period in the proposed converter. For example at $V_{in} = 200$ V, the current circulates for 52% of the time in the conventional converter, whereas it drops to 4% when the proposed converter reconfigures to another mode.

D. CONSIDERATION OF MODE SWITCHOVER

To ensure the intended operation of the converter, the switchover of modes requires careful considerations. There are two important aspects to be considered. One is the stability of the output voltage and the other is the switching of respective power devices. Both require a smooth transition to ensure proper operation. When the transition occurs, the converter resets effective gain from high to low or vice versa, which varies the operational duty of the converter. The strategy adopted for the evaluation of the concept is shown in Fig. 9, where the line voltage is sensed and the controller enters into a transition strategy. A delay of 15 μsec has been introduced between the switchovers to ensure demagnetization of transformers. To keep the output voltage stable the new duty cycle has been updated one cycle earlier the start of switchover command.

E. CURRENT STRESS

The parallel connection of secondary windings reduces the current stress on secondary elements such as windings, rectifiers and filtering components by a factor of four. This helps to reduce the volume and cost of the converter. The current stress on primary devices is different in both modes. This is because the transformers and devices are configured differently in each mode. In low-gain mode, the current stress on the devices of the leading leg $S_a - S_b$, and the lagging leg $S_e - S_f$, is given as the sum of the magnetizing current and the reflected load current, i.e.,

$$I_{p\_L} = I_{LM\_L} + I_{o\_T}/n_L \tag{23}$$

In high-gain mode, all three legs are active, the current flows through legs $S_a - S_b$, and $S_e - S_f$ is

$$I_{ab} = I_{ef} = I_{LM\_H} + I_{o\_T}/n_H \tag{24}$$

Since the current adds up in the common leg, therefore common leg bears twice as much stress as compared to the other two legs i.e., $I_{cd} = I_{ab} + I_{ef}$

F. REDUCED SIZE OF THE OUTPUT FILTER INDUCTOR

The operation with a high duty ratio also reduces the ripple current on the filtering components. The peak to peak current ripple in the output filter inductor depends upon the operational duty cycle and is estimated as [20]

$$\Delta I_{pk-pk} = \left\{ \left(\frac{N_s}{N_p} V_{in} - V_{out} \right) \left(1 - 2D_{eff}\right) T_s \right\} / L_o$$

The elimination of freewheeling interval and hence the operation with high duty cycle reduces the peak-peak ripple current in the output filter inductor. Besides, since the secondary windings of the transformers are connected in parallel, the amount of load current flowing through each winding is $I_{o\_T}/4$. This further cuts the size and cost of filtering components.

TABLE 1. Specification of the Example Application and Key Parameters of Key Circuit Components/a Single Transformer

Symbol	Quantity	Value
V_{in}	Input voltage	100-400 V_{dc}
V_{out}	Output voltage	12 V_{dc}
P_{out}	Load power	1.2 kW
f_s	Switching frequency	200 kHz
S_a-S_f	Power devices	GS66508B
D_1-D_8	Rectifiers	SBLF25L30
DSP	Microchip's dsPIC	Dspic33fj16gs
	Core shape/ size/ material	PQ 20/20/3C95
L_p/L_s	Primary/ secondary inductance	190/3 µH
L_{kp}/L_{ks}	Primary/secondary leakage inductance	2.8/0.05 µH
Rac	Primary/ secondary winding ac resistance	120/10 mΩ
N_p:N_s:N_s	Primary to secondary turn ratio	4:1:1
L_o	Output filter inductor	4.7 µH
C_0	Output filter capacitor	68 µF

TABLE 2. Table of Equations Used in the Loss Analysis

Part	Loss	Calculation	
		high-gain mode	low-gain mode
Power devices	Driver	$P_{dr} = (V_{gs}Q_g f) \times 6$	$P_{dr} = (V_{gs}Q_g f) \times 4$
	Conduction	$P_{cond} = (I_{rms}^2\ R_{ds}) \times 3$	$P_{cond} = (I_{rms}^2\ R_{ds}) \times 2$
	switching	$P_{sw} = (V_{in}I_{rms}f(t_{rise} + t_{fall})) \times 3$	$P_{sw} = (V_{in}I_{rms}f(t_{rise} + t_{fall})) \times 2$
Rectifiers	Conduction	$P_D = \left(\frac{1}{2}V_f I_o + I_{Srms}^2 R_D\right) \times 8$	$P_D = \left(\frac{1}{2}V_f I_o + I_{Srms}^2 R_D\right) \times 8$
Transformer	Copper	$P_{cu} = (I_{rms}^2\ R_{ac} + I_{Srms}^2\ R_{Sac}) \times 4$	$P_{cu} = (I_{rms}^2\ R_{ac} + I_{Srms}^2\ R_{Sac}) \times 4$
	Core	$P_c = (K_{fe}B^{\beta}V_e) \times 4$	$P_c = (K_{fe}B^{\beta}V_e) \times 4$

IV. LOSS CONSIDERATIONS

To investigate the performance of the proposed converter, the concept is applied to an example application, and the theoretical losses are first estimated for both the operational modes. The specifications of the example application along with the key circuit components/ transformer parameters are given in Table 1.

The component-specific parameters such as device switching characteristics, drain-source resistance, and forward voltage drop have been taken from the respective datasheet. The core parameters are taken from the manufacturer's datasheet and other key parameters of the transformers such as ac resistance R_{ac} of the windings, leakage inductance and the magnetizing inductance have been measured on Bode-100 impedance analyzer. The table of equations used to estimate the losses is given in Table 2 [27]. As seen the operation in high-gain mode adds one switching device and two gate drivers in loss contribution. For the operation in high-gain mode, the input voltage range is set as $V_{in} = 100$–200 V, whereas, it is set as $V_{in} = 200$–400 V for low gain mode. The losses are calculated for the complete range of input voltage and the load power. An example comparison is shown in Fig. 10, for the load power of 1.2 kW.

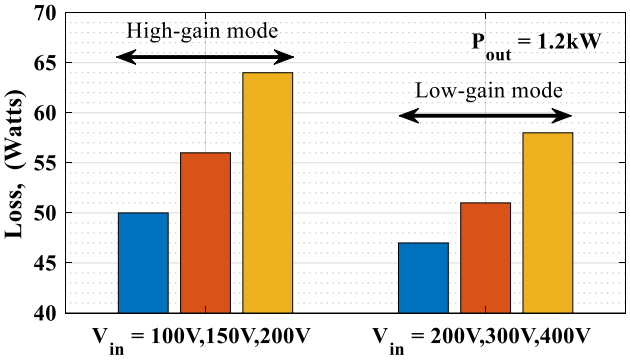

FIGURE 10. Comparison of the loss for both modes at 1.2 kW of the load power.

TABLE 3. Example Comparison of the Key Parameters between the Design With the Proposed and the Conventional Approach

Quantity	Conventional converter	Proposed converter
Circulation current at Vin (max.)	75%	50%
Switching/ conduction loss	100%	150%
Duty cycle at Vin (max.)	10%	25%
Stress on rectifiers	100%	25%
Stress on filtering elements	100%	25%
Thermal management	Complex	Simple
EMI	High	Low
Performance against input voltage	Degrading	Stable
Design complexity	Less	High

As seen, the losses are similar in both modes. Generally, power transformer mainly contributes towards the total loss in power converters, here as the input voltage increases above the specified limit, converter reconfigures to low-gain mode, which doubles the number of series-connected transformers, as a result, this keeps the volt-sec constant in both modes. As the input voltage increases, the loss goes up because of the reduced duty cycle. The loss distribution among different parts is also similar in both modes. Two additional switching devices and higher magnetizing current marginally increase the losses in high-gain mode.

V. COMPARISON OF THE PROPOSED AND A CONVENTIONAL CONVERTER

The design and performance comparison of key factors between the proposed converter and the conventional converter is listed in Table 3. The comparison is based on the analytical calculations made to the same specifications. As discussed, the operation with a high duty cycle keeps the performance stable. Moreover, higher operational duty results in reduced ringing and overshoot which improves EMI performance. The conduction and switching losses are slightly higher in the proposed due to the addition of two more devices. Although the

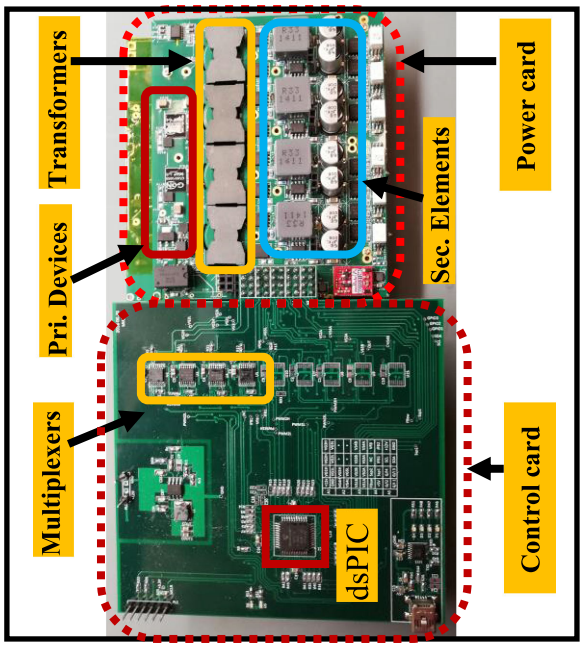

FIGURE 11. Picture of the prototype, showing both the control card and the power card.

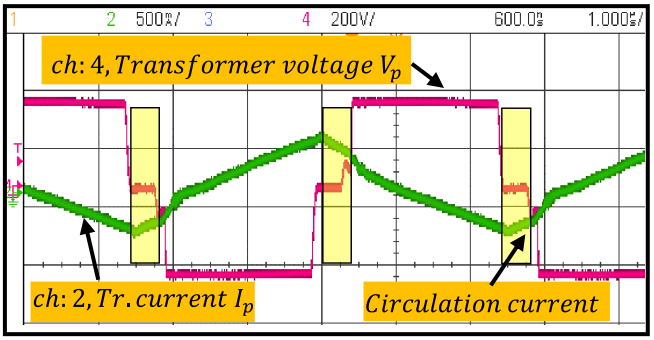

FIGURE 12. Demonstration of the flow circulation current in freewheeling interval. *Ch 2:-500 mA/div, Ch 4:-200 V/div, time base:-1μsec/div.*

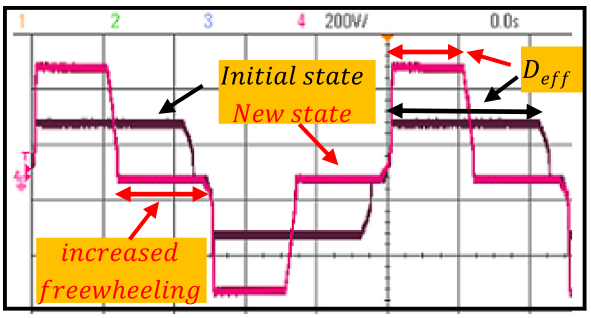

FIGURE 13. Working of a conventional converter, increased input voltage extends the freewheeling interval, Ch 4:-200V/div, time base:-1μsec/div.

component count in the proposed converter is higher which adds complexity, however the reduced stress on circuit components reduces the required power rating and volume of the components. The cost of components mainly depends upon the level of stress and in some cases, the only option available is the customized solution [28], [29]. For the example design, the required dc current rating of the filtering components is approximately 100 Amps if the design would have been made with the conventional approach. The availability of such high rating component is narrow and the solution is either the use of multiple components or the customized. However, on the economies of scale, the conventional design may be more cost-effective [28]. The presented approach of split transformers and parallel configuration of circuit elements simplifies heat management and improves system reliability.

VI. EXPERIMENTAL VERIFICATIONS

For the verification of the proposed concept, a prototype of an example application of the proposed converter is designed and investigated. The assembled converter along with the assembled control card is shown in Fig. 11. The control card contains Microchip's dsPIC, multiplexers and other necessary feedback and line sense circuitry. The switching control of power devices is routed via multiplexers. The power card consists of power devices, transformers, rectifiers and filters. The specifications of the prototype are the same as listed previously in Table 1. As given the physical turn ratio N_p/N_s , of a single center-tapped transformer is 4:1:1. By using (1) and (2) the effective dc conversion ratio becomes 8:1:1 in high-gain mode and it changes to 16:1:1 in low-gain mode. The performance of the converter is investigated for different operating conditions, for example, the variation in the line voltage and the load conditions. When the line voltage increases, in conventional PSFB converter, it requires to reduce the duty cycle to keep the output voltage constant, the proposed converter instead varies the effective turn ratio of the transformer to keep the output voltage constant. To verify that, the working range in the example investigations is set as V_{in} = 100–200 V_{dc} for high-gain mode, and above 200 V_{dc} up to 400 V_{dc} for low-gain mode. Each mode is characterized up to the load power of 1.2 kW.

Fig. 12, demonstrates the concept of circulation current. As seen current continues to flow during the freewheeling interval when the voltage at the primary winding of the transformer is zero. It means no power is transferred and circulation current merely flows through power devices adding more conduction losses. The more is the freewheeling interval, more is the loss.

Fig. 13 and 14 demonstrate the comparison of the freewheeling interval between the working of a conventional converter and the proposed converter. In both figures, channel 4 represents the differential voltage as an input to the primary windings i.e., V_{p14} in low-gain mode, and V_{p12} or V_{p34} in high-gain mode. In figure 13, suppose a conventional converter is working at V_{in}=200 V, at some point the input voltage increases to 400 V, to keep the output voltage constant, it is required, as shown, to reduce the duty cycle, which ends in the larger freewheeling interval. Instead of reducing the duty cycle, the proposed converter switches to another mode to reduce the effective turn ratio and keeps the duty cycle and the output voltage constant. Fig. 14, explains that the duty cycle

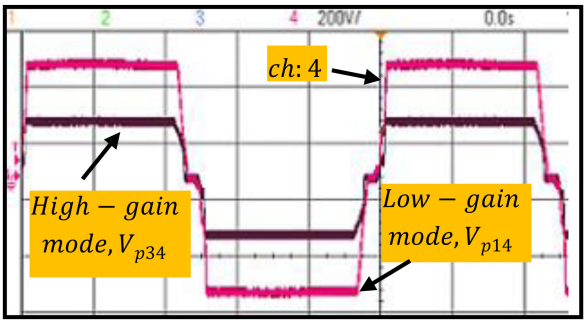

FIGURE 14. Working of the proposed converter, no change in the duty cycle despite 100% change in input voltage, *Ch 4:–200V/div, time base: –1μsec/div.*

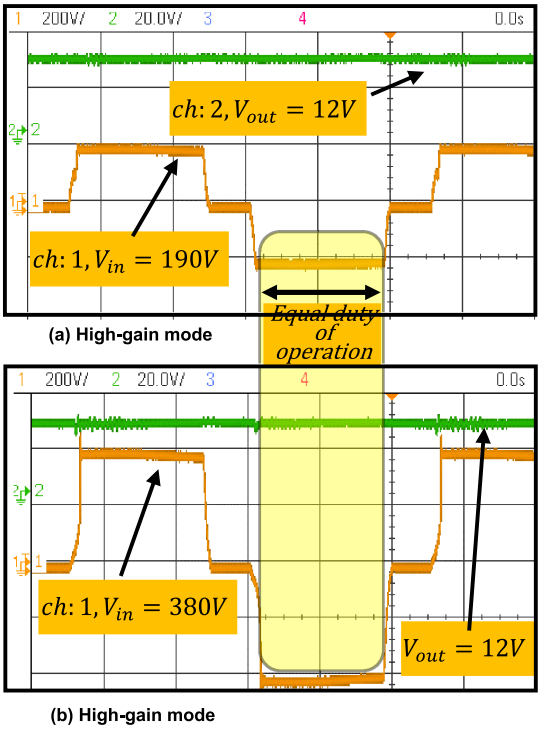

FIGURE 15. Demonstration of equal operational duty and maintained output voltage in both modes for the same load. *Ch 1:-200V/div, Ch 2:-20V/div, time base:-1μsec/div.*

remains unchanged in both modes even though the change in the input voltage is 100%. Since converter reconfigures the effective turn ratio N_p/N_s, it becomes half in the high-gain mode as compared to the low-gain mode, therefore, the input voltage also requires to reduce to half to maintain the operating conditions.

Fig. 15(a) and 15(b), again demonstrates how the switchover of effective gain keeps the operational duty constant. The operation in both modes has been captured for the same operating conditions but double the variation in the input voltage. The bridge voltage V_{p34} and V_{p14} for high-gain mode and low-gain mode have been captured respectively against the output voltage. As given in (19) and (20), the effective

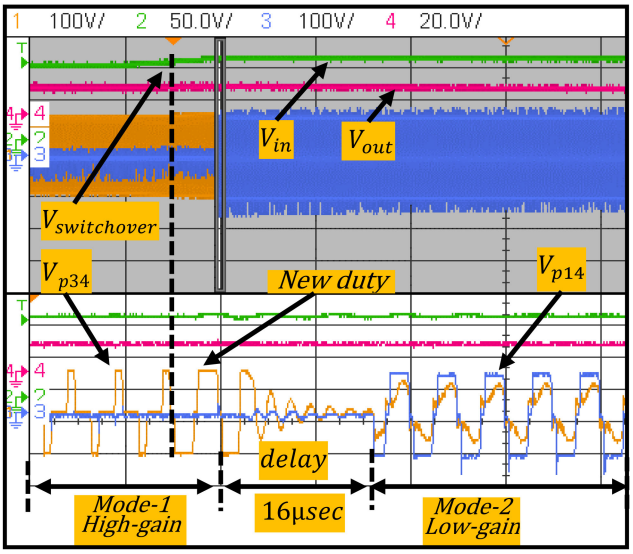

FIGURE 16. Dynamic transition of converter from high-gain mode to low-gain mode. *Ch 1:-100V/div, Ch 2:- 50V/div, Ch 3:- 100V/div, Ch 4:-20V/div.*

gain of the converter depends on the interconnection of transformers in each mode. Therefore, to keep the gain equal, operational duty cycle has to increase or decrease accordingly. As seen, the operational duty is same for both the modes although the change in the input voltage is 100%.

Fig. 16 shows the smooth dynamic switchover of modes when the input voltage crosses the set limit. The transformer bridge voltage V_{p34} and V_{p14} of both the operational modes have been simultaneously captured along with the input voltage and the output voltage of the converter. The figure shows both the actual waveforms captured at the trigger level of the oscilloscope and magnified view of the interval when mode switchover takes place. As the input voltage reaches the switchover voltage, the controller updates the operational duty and then adds the delay before switching to another mode. The output voltage remains almost constant.

In high-gain mode all three legs become active and the primary current is equally divided into two paths i.e., the primary current I_{p12} and I_{p34}. Fig. 17, shows the bridge voltage along with primary current (V_{p12}, I_{p12}, V_{p34}, I_{p34}) for both paths. As seen both paths bear the same level of voltage and current. Both of these currents add up in the common leg, which makes twice as much stress on the devices of this leg.

Fig.s 18–21 show the soft switching characteristics of the converter for different operating conditions. The ZVS is observed by capturing simultaneously the gate/drain waveforms of the respective devices. Fig. 18–19, compare the ZVS of leading legs for both modes of the operation. In high-gain mode, both outer legs act as the leading leg. In Fig. 18, the switching waveforms of both low side devices S_b and S_f have been captured. Channel 1 and channel 4 respectively show the gate-source voltage and the drain-source voltage of device S_b, whereas channel 2 and channel 3 are respectively the gate-source voltage and the drain-source voltage of device S_f.

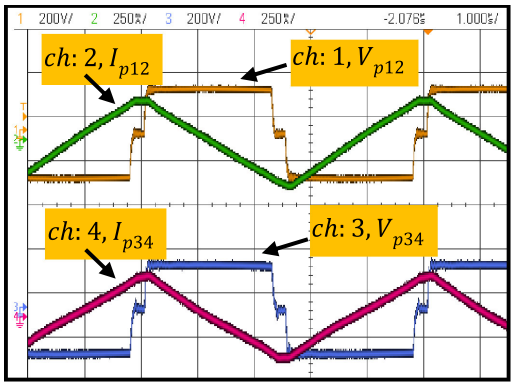

FIGURE 17. Demonstration of the equal amount of the flow of primary current in high-gain mode through two different paths. *Ch 1:-200V/div, Ch 2:-250mA/div, Ch 3:-200V/div, Ch 4:-250mA/div time base:-1μsec/div.*

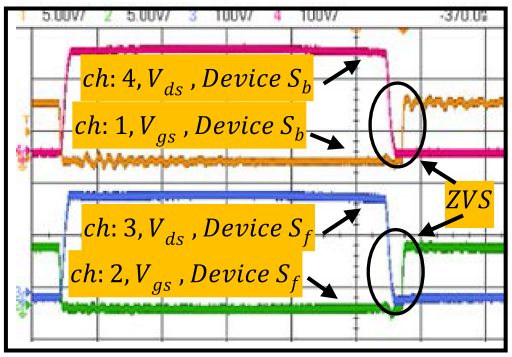

FIGURE 18. ZVS of leading leg—high-gain mode, 100% of the rated load. *Ch 1:-5V/div, Ch 2:-5V/div,Ch 3:-100V/div, Ch 4:-100V/div, time base:-0.5μsec/div.*

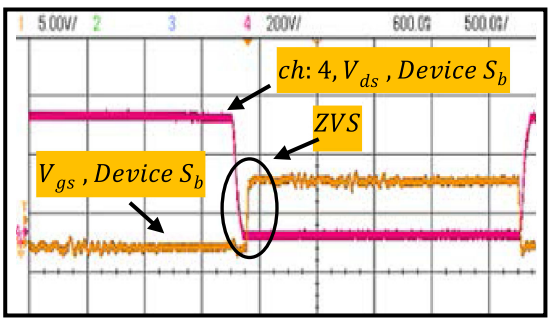

FIGURE 19. ZVS of the leading leg—low-gain mode, 100% of the rated load.*Ch 1:-5V/div, Ch 4:-200V/div, time base:-0.5μsec/div.*

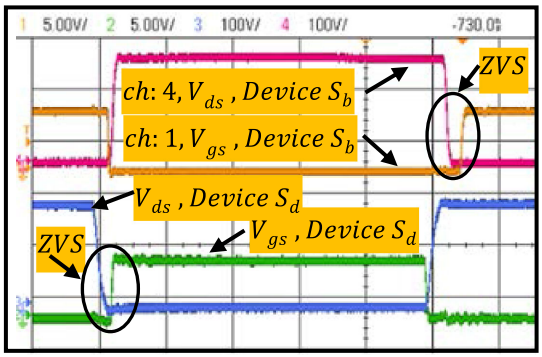

FIGURE 20. ZVS of the leading leg and the lagging leg, 10% load—high-gain mode, *Ch 1:-5V/div, Ch 2:-5V/div, Ch 3:-100V/div, Ch 4:-100V/div, time base:-0.5μsec/div.*

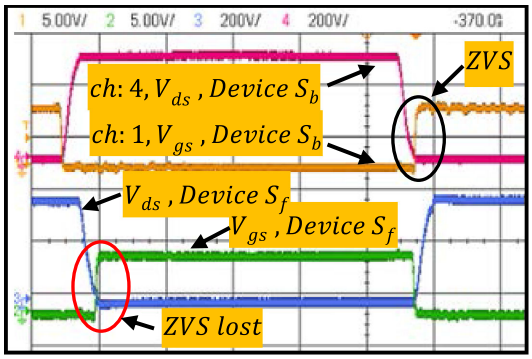

FIGURE 21. *ZVS of the leading leg and the lagging leg, 10% load—low-gain mode, Ch 1:-5V/div, Ch 2:-5V/div, Ch 3:-200V/div, Ch 4:-200V/div, time base:-0.5μsec/div.*

Similarly, Fig. 19, represents switching waveforms of the device S_b of the leading leg for the operation in low-gain mode. The operating condition for both figures is $V_{in} = 200\text{V}_{\text{dc}}/400\text{V}_{\text{dc}}$, $V_{out} = 12\text{V}_{\text{dc}}$, $P_{out} = 1.2$ kW. As seen, these devices possess the same switching characteristics in both modes. All devices turn ON observing complete zero voltage switching.

In phase shifted full bridge converter, it is difficult to achieve ZVS for the lagging leg at light load. The switching of devices of the lagging leg together with the devices of the leading leg has also been investigated at light load. For this, the load is reduced to 10% of the rated load i.e., $P_{out} = 100$W. Fig. 20, compares the ZVS characteristic of both legs together for the operation in high-gain mode, and Fig. 21, shows the characteristics for the operation in low-gain mode. In high-gain mode, since both leading legs have the same characteristics, the switching waveforms of only the device S_b have been compared. As seen in figures, the devices of the leading leg observe complete ZVS in both modes, while the devices of the lagging leg show better performance in the high-gain mode as compared to the series mode. It means the devices of lagging leg observe ZVS for a wide range of load power. This is because of the fact, that the operation of the converter in high-gain mode stores twice as much inductive energy as the operation in a low-gain mode that makes it possible for the lagging leg to observe ZVS for a wider range.

The performance of the converter for the full range of input voltage has also been characterized. Fig. 22, is the efficiency curve over the complete range of input voltage $V_{in} = 100\text{V} - 400\,\text{V}$. Similar to Fig. 10, shows that the proposed converter maintains the efficiency stable for a wide range of input voltage. For $V_{in} = 100$–200 V the converter operates in high-gain mode, as the input voltage increases the efficiency drops because of the reduced duty cycle. For $V_{in} > 200$V, converter reconfigures to low-gain mode resets the duty cycle

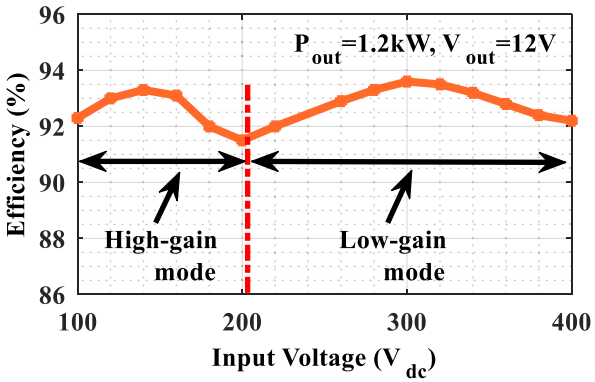

FIGURE 22. Performance curve of the proposed converter over the complete range of input voltage at the maximum of rated load.

high again, which results in improved efficiency. As a comparison with the theoretical loss shown in Fig. 10, the losses at $V_{in} = 150$ V and $V_{in} = 300$ V are approximately 55 W and 50 W respectively. The theoretical efficiency comes out above 95%. As seen, the measured efficiency for the same operating is approximately 94% which is comparable with the calculated efficiency.

VII. CONCLUSION

A modified phase shifted full bridge converter has been presented. As a comparison with the conventional converter, the proposed converter keeps the duty cycle high for a wide range of input voltage. The reduced freewheeling interval improves the performance of PSFB converters by minimizing downgrading factors such as duty cycle loss, excessive circulation current, noise in rectifiers and high EMI. The operation with a high operational duty keeps the converter in continuous conduction mode that reduces large ripple current and hence reduces the size of the output filter inductor. Also the reduced voltage stress on transformers, wider operational duty minimizes the rate of magnetic flux excursion, which serves to further reduce the losses in the cores. The performance can be maintained stable by reconfiguring the converter into an appropriate mode following the variation in the line voltage and/or the demand in the load. As a proof of concept, a smooth transition of modes switchover has been demonstrated. This makes the proposal more applicable. The prototype results show that the power devices observe soft switching for a wide range that helps to extend ZVS range. The design of a converter with multiple low profile cores and components reduces the weight and volume of the converter as compared to the design with a conventional single transformer. Therefore, the converter gets more attention for the applications where weight and volume are the main concerns. As a part of the future of work, a detailed analysis of the control strategy of the proposed concept will be presented as a separate work.

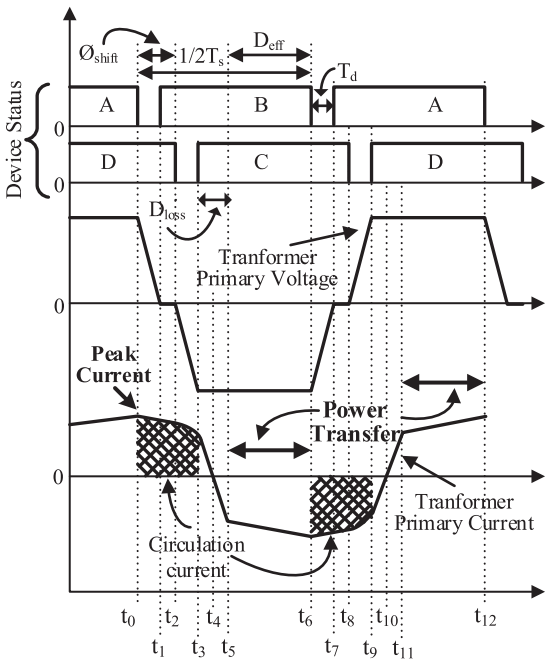

FIGURE 23. Explanation of circulation current in a typical phase shifted full bridge converter.

APPENDIX-A
CONCEPT OF CIRCULATION CURRENT

In switched-mode power converters, the regulation of the output voltage is generally maintained by adjusting the operational duty cycle in line with the operating conditions. As shown earlier in Fig. 1, to balance the volt-second on the primary side and the secondary side the duty cycle has to decrease when the line voltage increases. This extends the freewheeling interval where primary current circulates merely through the switching devices. The useful intervals in a complete switching cycle are the intervals where power is delivered from the input side to the output side. A typical timing diagram of a phase shifted full bridge converter along with transformer primary voltage and current is shown in Fig. 23, where A and B represent one leg and C and D represent the second leg. As shown during the freewheeling interval, the transformer primary winding voltage effectively remains zero and there is no transfer of power, primary current circulates only through the primary devices. This contributes to the increase in conduction losses. The wider is the freewheeling interval the more will be the loss. As seen the power is transferred alternately from t_5-t_6 and t_{11}-t_{12}. The rest of the time is referred to as the freewheeling interval. The only significant duration within this interval is the length of dead time between the devices of the same leg, which is required to ensure zero voltage switching of the devices. The loss due to the circulation current dominates during the freewheeling period. The primary current circulates at its peak through power devices results in more conduction loss.

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