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Multi-Winding Transformer for 18-Pulse AC–DC Converter Fed 7-Level CHB-Inverter With Fundamental Switching Based VCIMD

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(Invited Paper)

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ABSTRACT In this article, a new structure is used for induction motor drive (IMD). A Δ-polygon configuration based multi-winding transformer is designed in it to get an eighteen pulse AC-DC converter, which fulfill the DC-supply requirement of a 7-level cascaded H-bridge (CHB) inverter. This 7-level CHB-inverter is utilized at the drive end, to drive an induction motor (IM) and it requires less semiconductors switches and DC-supplies than the existing 7-level CHB-inverter. Therefore, a modified multi-winding transformer is designed to fulfil the need of a 7-level CHB-inverter, which also makes the input current closer to sinusoidal and reduces its THD to an acceptable value. A vector control is used to control an IM, which has good performance than v/f control. A new fundamental frequency switching technique (area equalization modulation strategy) is used in this work, to operate a 7-level CHB-inverter at fundamental frequency switching, which reduces the switching losses and increases efficiency of the system. The comparative study is also given to show the effectiveness of the system. Performance of the system is analyzed in MATLAB/Simulink under various operating conditions of IM. The simulated performances are validated from the experimental results captured from the developed laboratory prototype.

INDEX TERMS Multipulse ac–dc converter, multilevel inverter, induction motor drive and power quality.

I. INTRODUCTION

With technology advancements in semiconductor devices such as insulated gate bipolar transistors (IGBTs), modern high-power medium voltage (MV) drives are increasingly used in petrochemical, mining, steel and metals, transportation and other industries to conserve electric energy, increase productivity and to improve product quality. Although research and development of the medium voltage drive, are continuously growing, the literature dedicated to this technology seems to be very limited [1], [2]. Hence, the aim of this paper, is to propose a configuration of medium voltage induction motor drive (MVIMD) and their performances are proved by simulations and test results.

In [3]–[5], several MVIMDs are reported. These show the needs of multi-winding transformer (MWT) in case of MVIMD. Since, the IM voltage is in few kV and available grid rating is in 33/11 kV. Hence this MWT matches the nominal stator voltage and connects several diode bridge rectifier (DBR) in selected style, which cancel the harmonics produced among BDRs. By doing this, it has made the supply current similar to sinusoidal and decreased its THD to an adequate value [6], [7].

Three types of conventional multilevel inverters namely neutral point clamped (NPC), flying capacitor (FC) and cascaded topologies, are utilized in MVIMDs. A NPC-MLI has capacitor voltage equalization issue. Several strategies have been reported in the literature to maintain the required voltage across capacitor of NPC MLI [8], [9]. These modulation strategies are quite difficult, and the difficulty increases as the number of level increases. In FC-MLI, apart from

DC-link capacitor, it also has flying capacitors. These DC-link and flying capacitor voltages must be supervised very precisely for proper operation of flying capacitor inverter [10], [11]. A cascaded H-bridge (CHB) multilevel inverter (MLI) is one of the popular inverter topologies for MVIMDs. Unlike other multilevel inverters, where high-voltage insulated gate bipolar transistors (IGBTs) are utilized, the CHB inverter normally utilizes low-voltage IGBTs as a switching device in a H-bridge power module (PM). The PMs are connected in cascaded manner to achieve medium voltage operation. This CHB-inverter has easy structure and simple control. Moreover, the power rating in CHB-inverter, can be easily scaled to required value. Therefore, in this study, CHB-inverter is utilized. The CHB-inverter has been successfully implemented for MVIMD in [12]–[14].

In the literature [12]–[14], an eighteen pulse AC-DC converter fed 7-level CHB-inverter based IMD is reported. In [12]–[14], a symmetrical CHB-inverter is used, which need 36 power semiconductor switches and 9-isolated DC-supply. To get, these DC-supply using MWT a quite big MWT is needed. Therefore, in this work, a binary principle is used to choose the DC voltages. By this principle, a 7-level CHB-inverter needs 24 power semiconductor switches and 6-isolated DC-supplies only. Moreover, to get 6-isolated DC-supply from MWT, a small size MWT is needed compared to the MWT given in [12]–[14]. Apart from it, in [12]–[14], the MWTs have symmetrical voltage windings on both primary and secondary side. However, in the work, the MWT has asymmetrical voltage secondary windings. The complete design equation of this modified MWT is given in section III. From above discussion, it is realized that the configuration of MVIMD given in this work, needs less electrical components. Therefore, the size and cost of the proposed MVIMD are quite less than the existing MVIMD [12]–[14].

In [12]–[15], a 7-level CHB-inverter is controlled by sinusoidal pulse width modulation (SPWM). Therefore, the switching frequency of 7-level CHB-inverter is high and these MVIMD has considerable switching losses. Due to it, these existing MVIMDs have moderate efficiency. This problem can be solved by utilizing fundamental frequency switching (FFS) to control this 7-level CHB-inverter. A selective harmonic elimination (SHE) technique is most widely utilized in CHB-inverter to achieve FFS [16]–[18]. In SHE strategy, the switching angles are calculated from transcendental equations, which is a function of cosine terms and modulation index. Therefore, in most of the literature, switching angles are calculated off-line at different values of modulation index and performance of CHB-inverter corresponding to each set of switching angles, is analyzed. The calculation of the switching angles corresponding to each modulation index varying from 0 to 1, is not possible. It is because, quite complex and time taking methods are utilized to solve the transcendental equations. Therefore, for constant load voltage frequency application or known modulation index application, SHE is quite good. However, SHE strategy becomes very complex for applications, where load voltage frequency and modulation

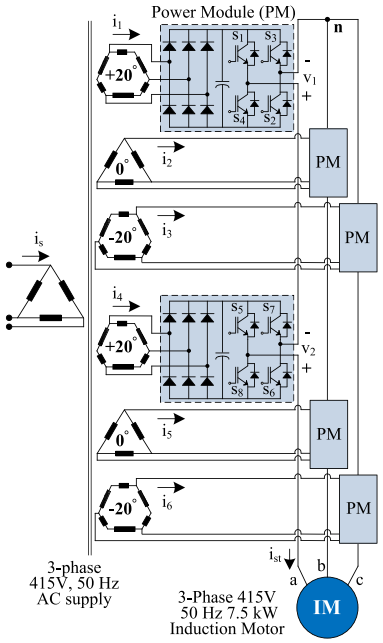

FIGURE 1. Schematic of proposed system.

index are varying in nature. It is because, the algorithms to solve transcendental equations are very stochastic and one cannot predict what going to happen, because it takes random steps and one cannot be sure for the correct solution within the limited time. Therefore, SHE is not utilized in this work. In the literature [19], a nearest level modulation technique (NLMT) is reported. By utilizing NLMT, one can easily get the FFS of CHB-inverter. Moreover, in the case of NLMT, switching angles calculation is not required as like SHE technique. However, this modulation strategy is more suitable for higher numbers of levels (more than 13-levels). It is because in this strategy, predefined levels are obtained from the quotient of ratio (m_{ref}/S_p), where, m_{ref} is the instantaneous value of references signal produced from indirect vector control (IVC). Due to this, if NLMT is utilized for 7-level CHB-inverter then the output phase voltage symmetry is not maintained over a wide speed range of IMD and the power quality of voltage and current at the motor terminals, is very poor. Therefore, a new area equalization modulation strategy (AEMS) is used here for binary based 7-level CHB-inverter, to operate this at FFS over a wide speed range operation of IMD. The complete theory and implementation of AEMS for IMD, are given in this study.

II. SYSTEM CONFIGURATION

The schematic diagram of MVIMD is depicted in Fig. 1. Here, it is seen that the MWT configured eighteen-pulse converter is used. This MWT has Δ-connected primary and its secondary has 6-windings and separated in two parts. First part has 2-isolated delta polygon windings for $+20°$ and $-20°$ phase-shift and one Δ-connected windings. These are the mandatory requirement for eighteen pulse converters. Second part has similar configuration as first part. Whereas the winding voltages of second part are two times the first part. These six

isolated windings give six-isolated AC-supply, which are converted into six-isolated DC-supply by mean of DBR. These six-isolated DC-supplies are the input for binary based 7-level CHB-inverter as depicted in Fig. 1. This inverter has 7-levels (0, $\pm v_{dc}$, $\pm 2v_{dc}$, $\pm 3v_{dc}$) in phase voltage and 13-levels in line voltage. The switching sequence for a-phase to get this 7-level is given as '$S_1S_3S_5S_7$' for "0", '$S_1S_2S_5S_7$' for "1", '$S_1S_3S_5S_6$' for "2", '$S_1S_2S_5S_6$' for "3", '$S_3S_4S_5S_7$' for "−1", '$S_1S_3S_7S_8$' for "−2", '$S_3S_4S_7S_8$' for "−3", in similar way sequences are found for 'b' and 'c' phases.

III. SYSTEM MODELLING

This system is depicted in Fig. 1. An eighteen-pulse converter is used as a front end and a 7-level CHB-inverter at drive end. Here, a 3-phase, 415 V, 50 Hz AC mains, is taken to operate a 3-phase, 415 V, 50 Hz, 7.5 kW IM. The complete design and selection of required parameters of proposed VCIMD, are given here in detail.

A. CALCULATION OF DC-LINK VOLTAGE

A 7-level CHB-inverter is depicted in Fig. 1. Here, it is seen that a 7-level CHB-inverter has two PMs in each leg. Typically, V_{dc}, and $2V_{dc}$ voltages are utilized to produce 7-levels in phase voltage. Here, the switching sequence is taken in such a manner that the transition from one to other switching sequence, has minimal changes in it. The DC-link capacitor voltage is obtained from,

$$m_a = \frac{\widehat{V}_{an1}}{B4V_{dc}/\pi}. \tag{1}$$

Where m_a, $\widehat{V}_{an1}$, B and V_{dc} represent the modulation index, peak of fundamental phase voltage, number of PMs and DC voltage, correspondingly. This equation is derived for symmetrical cascaded inverter-based configuration. However, it holds good for both symmetrical and asymmetrical configuration. Moreover, in case of symmetrical configuration, 'B' is the number of H-bridge cells and in case of asymmetrical configuration, 'B' is a number of positive steps.

From (1), $\widehat{V}_{an1}$ is calculated as,

$$\widehat{V}_{an1} = \frac{m_a B4V_{dc}}{\pi} = \frac{0.8 \times 3 \times 4V_{dc}}{\pi} = 3.056V_{dc}.$$

The rms of V_{an1} is obtained as,

$$V_{an1} = \frac{\widehat{V}_{an1}}{\sqrt{2}} = \frac{3.056V_{dc}}{\sqrt{2}} = 2.164V_{dc}.$$

To meet the active power requirement of IMD, the V_{an1} should be equivalent to stator phase voltage ($V_{st\,ph}$).

$$V_{an1} = 2.164V_{dc} = V_{st\,ph} = 239.6 \text{ V}.$$

Utilizing binary methodology, a 7-level CHB-inverter should have $V_{dc} = 110$ V and $2V_{dc} = 220$ V, to drive a 7.5 kW motor.

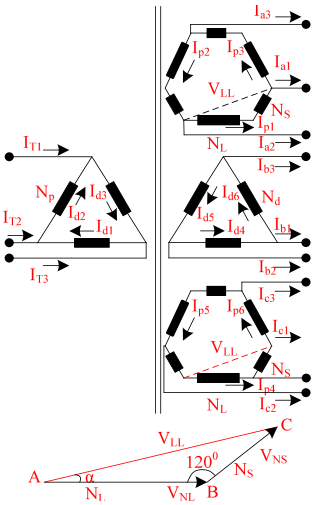

FIGURE 2. Configuration of delta-polygon transformer and its vector diagram.

B. EIGHTEEN-PULSE CONVERTER

The configuration of MWT is depicted in Fig. 1. The winding voltages are obtained from the vector diagram depicted in Fig. 2. The relation between output voltage (V_{dc}) and line input voltage (V_{LL}) of a 6-pulse AC-DC conversion, is expressed as,

$$V_{LL} = \frac{\pi V_{dc}}{3\sqrt{2}} = \frac{\pi \times 110}{3\sqrt{2}} = 81.453 \text{ V}.$$

The dependency among line voltages, small and large windings voltage of delta-polygon transformer, is obtained by utilizing ΔABC as depicted in Fig. 2, and given as,

$$\frac{V_{LL}}{\text{Sin}120} = \frac{V_{NS}}{\text{Sin}\alpha} = \frac{V_{NL}}{\text{Sin}(60-\alpha)}. \tag{2}$$

As mentioned earlier to get 18-pulse AC-DC conversion, α must be equivalent to 20°. The 'V_{NS}' and 'V_{NL}' winding voltages for delta-polygon configuration, are obtained here,

$$V_{NS} = \frac{\text{Sin}20}{\text{Sin}120}V_{LL} = 32.168 \text{ V}$$

and

$$V_{NL} = \frac{\text{Sin}(60-20)}{\text{Sin}120}V_{LL} = 60.457 \text{ V}.$$

Here, a 7.5 kW IMD is utilized. Each leg of 7-level CHB-inverter has two PMs and they are coupled in cascaded fashion as depicted in Fig. 1. The same amount of current flows through the both PMs of each leg and their value is equivalent to the phase current of an IM. From aforementioned section, the values of DC-link capacitor voltages, are obtained ($V_{dc} = 110$ V and $2V_{dc} = 220$ V). Here, it is assumed that the power of first PM of each leg, is P_1.

The mathematical equation of power is expressed as,

$$P_1 + P_2 = P_1 + 2P_1 = \frac{\text{RatingofInductionMotor}}{3} = \frac{7.5kW}{3}. \quad (3)$$

It is considered here that the losses are negligible. Therefore, input power = output power, and it is written as,

$$V_{dc}I_{dc} = P_1$$

Therefore, the DC-link current is as,

$$I_{dc} = \frac{P_1}{V_{dc}} = \frac{833.33}{110} = 7.576 \text{ A}$$

where V_{dc} and I_{dc} represent the DC-link voltage and current of a PM, respectively.

The value of 'I_{a1}' for 6-pulse AC-DC conversion, is expressed here,

$$I_{a1} = I_{b1} = I_{c1} = \sqrt{\frac{2}{3}}I_{dc} = 0.8165I_{dc} = 6.186 \text{ A}.$$

In Fig. 2, the transformer has 2-windings in each phase.

The direction of each winding current of this transformer, is also depicted in Fig. 2. The currents in these windings, are calculated from Fig. 2 and they are given as,

$$I_{p1} = \frac{I_{a1} - I_{a2}}{3}, I_{p2} = \frac{I_{a2} - I_{a3}}{3} \text{ and } I_{p3} = \frac{I_{a3} - I_{a1}}{3}$$

$$I_{p1} = \frac{6.186\angle 0^\circ - 6.186\angle -120^\circ}{3} = 3.571\angle 30^\circ \text{ A}. \quad (4)$$

In this work, a transformer is utilized on the grid side, which has Δ-configured input windings and its output has 6-windings. Its output has four delta-polygon configured and two simple Δ-configured windings as depicted in Fig. 1. The summation of ampere-turns at transformer core must be zero.

Therefore, the ampere-turns of this transformer, are expressed here,

$$I_{d1}N_p - I_{p1}N_{1L} + I_{p3}N_{1s} - I_{d4}N_{1d} - I_{p4}N_{1L} + I_{p6}N_{1s} - I_{p7}N_{2L} + I_{p9}N_{2s} - I_{d7}N_{2d} - I_{p10}N_{2L} + I_{p12}N_{2s} = 0. \quad (5)$$

It results in,

$$I_{d1} = I_{p1}\left(\frac{N_{1L}}{N_p}\right) - I_{p3}\left(\frac{N_{1s}}{N_p}\right) + I_{d4}\left(\frac{N_{1d}}{N_p}\right) + I_{p4}\left(\frac{N_{1L}}{N_p}\right) - I_{p6}\left(\frac{N_{1s}}{N_p}\right) + I_{p7}\left(\frac{N_{2L}}{N_p}\right) - I_{p9}\left(\frac{N_{2s}}{N_p}\right) + I_{d7}\left(\frac{N_{2d}}{N_p}\right) + I_{p10}\left(\frac{N_{2L}}{N_p}\right) - I_{p12}\left(\frac{N_{2s}}{N_p}\right)$$

$$I_{d1} = 6.2443\text{A}.$$

The kVA rating of this transformer, is obtained from [8] as,

$$\text{Transformer, kVA} = \frac{0.5\sum V_{rms}I_{rms}}{1000} \quad (6)$$

$$= 0.5 \times \frac{\begin{bmatrix} 3V_{ph}I_{d1} + 3V_{1NL1}I_{p1} + 3V_{1NS1}I_{p3} + 3V_{1NL2}I_{p4} \\ +3V_{1NS2}I_{p6} + 3V_{1dph}I_{d4} + 3V_{2NL1}I_{p7} + 3V_{2NS1}I_{p9} \\ +3V_{2NL2}I_{p10} + 3V_{2NS2}I_{p11} + 3V_{2dph}I_{d7} \end{bmatrix}}{1000}$$

$$= 8.1604 \text{ kVA}.$$

The kVA rating of proposed MWT must be greater than 8.1604 kVA to operate a 7.5 kW motor.

IV. CONTROL ALGORITHMS

An IVC is used to run IM and an AEMS is utilized to run a 7-level MLI. Here, an IVC is utilized to achieve independent control of flux and torque of IMD. This IVC produces three voltage signals (v_a, v_b and v_c). These are input of AEMS. Aforementioned controls are elaborated herein in detail.

A. IVC

The structure of IVC control is depicted in Fig. 3(a). In it, the speed error is obtained from reference and sensed speed, which is input to PI controller and then reference q-axis current is estimated from this PI output. The field weakening technique is employed to obtain the d-axis current. These d and q axes currents are compared with sensed d and q axes currents. The error signals from these comparators are given to PI controllers, which gives the d and q axes voltages and it converted into abc co-ordinates. These v_a, v_b and v_c are the input for AEMS [6], [7].

B. AREA EQUALIZATIONS MODULATION STRATEGY

To achieve fundamental frequency switching, an AEMS is used in this work. In this modulation strategy, the steps in the VSI output voltage, are independent of the time and hence its frequency is not predefined. The frequency of VSI output voltage, depends on modulating signals. The plots of reference signals and VSI output voltage, are depicted in Fig. 3(b). To obtained α_1, α_2 and α_3, one may consider x_1, x_2, x_3, x_4, x_5 and x_6, which have same value and their summation must be equal to the peak of $\widehat{V}_{an}$, which indicates that area A_1 is identical to area A_2. Now considering, $\widehat{V}_{an}$ is equal to 1 p.u. and from Fig. 3(b). These are calculated as,

$$\sin\alpha_1 = X_1$$

$$\alpha_1 = \sin^{-1}(X_1) = \sin^{-1}(1/6) = 9.594^\circ \quad (7)$$

$$\sin\alpha_2 = X_1 + X_2 + X_3$$

$$\alpha_2 = \sin^{-1}(X_1 + X_2 + X_3) = \sin^{-1}(3/6) = 30^\circ \quad (8)$$

$$\sin\alpha_3 = X_1 + X_2 + X_3 + X_4 + X_5$$

$$\alpha_3 = \sin^{-1}(X_1 + X_2 + X_3 + X_4 + X_5)$$

$$= \sin^{-1}(5/6) = 56.443^\circ. \quad (9)$$

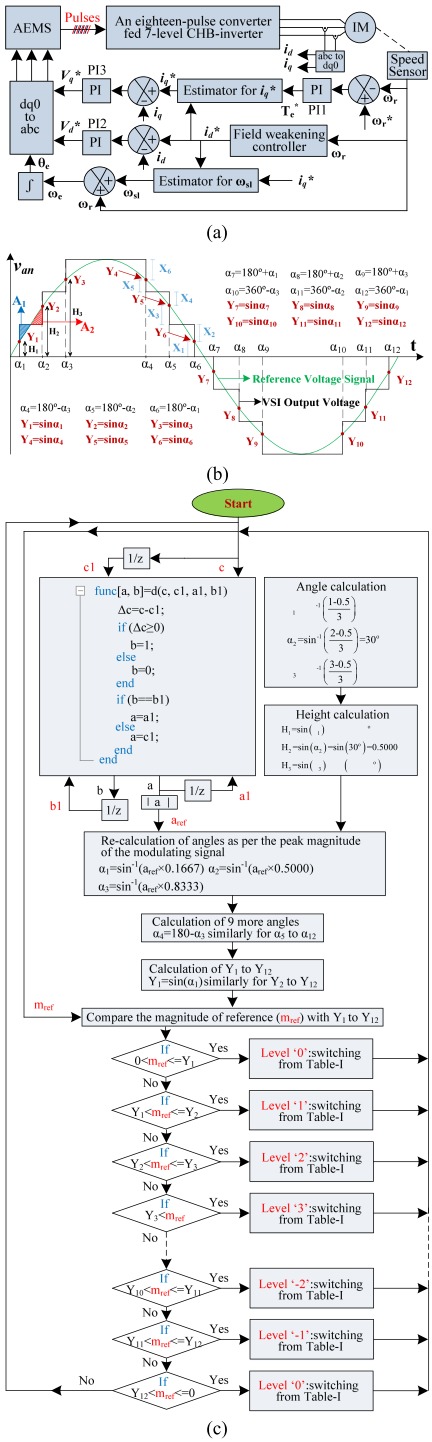

FIGURE 3. Control strategy of proposed system (a) block diagram of IVC, (b) reference and phase voltage waveforms for an AEMS and (c) flowchart for an implementation of AEMS.

From these expressions, one can generalize the angle calculation for N-level inverter as,

$$\alpha_i = \sin^{-1}\left((i-0.5)/N_p\right) \tag{10}$$

where $N_p = (N-1)/2$ and $i = 1, 2 \ldots\ldots N_p$. In case of a 7-level CHB $N_p = 3$ and $i = 1$, 2 and 3.

From (10), the switching angles are calculated for a 7-level CHB-inverter. In order to maintain the symmetry of inverter phase voltage, the height reference signal for every switching angle should be of same ratio. The heights (H_1, H_2 and H_3) are calculated for unity peak,

$$H_1 = \sin(\alpha_1) = \sin(9.594) = 0.1667$$
$$H_2 = \sin(\alpha_2) = \sin(30) = 0.5000$$
$$H_3 = \sin(\alpha_3) = \sin(56.443) = 0.8333.$$

Corresponding to peak magnitude (a_{ref}) of the reference signal, the angles are re-calculated as,

$$\left.\begin{aligned}\alpha_1 &= \sin^{-1}(a_{\text{ref}} \times H_1)\\ \alpha_2 &= \sin^{-1}(a_{\text{ref}} \times H_2)\\ \alpha_3 &= \sin^{-1}(a_{\text{ref}} \times H_3)\end{aligned}\right\}. \tag{11}$$

To get seven levels in phase voltage, the value of α_1, α_2 and α_3, is calculated using AEMS from (10). It is assumed that the modulating signal has sinusoidal waveform with peaks of $+1$ and -1. From these three angles, nine more angles ($\alpha_4 = 180°-\alpha_3$, $\alpha_5 = 180°-\alpha_2$, $\alpha_6 = 180°-\alpha_1$, $\alpha_7 = 180°+\alpha_1$, $\alpha_8 = 180°+\alpha_2$, $\alpha_9 = 180°+\alpha_3$, $\alpha_{10} = 360°-\alpha_3$, $\alpha_{11} = 360°-\alpha_2$ and $\alpha_{12} = 360°-\alpha_1$) are calculated to get the desired 7-levels in phase voltage. The magnitude of the sine waveform is calculated at different values of α (α_1 to α_{12}) and denoted by Y_1 to Y_{12} ($Y_1 = \sin(\alpha_1)$, similarly for Y_2 to Y_{12}), respectively. The modulating signals have also sinusoidal waveforms and their magnitude varies from $+1$ to -1. The instantaneous magnitude of the modulating signal is measured and denoted by 'm_{ref}'. There are two magnitude quantities, one (Y_1 to Y_{12}) is fixed to get predefined level and other one (m_{ref}) is varying between $+1$ and -1. From Fig. 3(b), it is observed that, if $0 < m_{ref} \leq Y_1$ then "0" level is required, to get it, switching sequence is carefully selected. In same fashion, the value of 'm_{ref}' is compared throughout the cycle with predefined values (Y_1 to Y_{12}) and according to the value of 'm_{ref}', one can know that which level is required at that instant. Then according to required level, switching pattern is carefully chosen and accordingly 7-level CHB-inverter is switched to get that level in phase voltage. From this, it is seen that the angle calculation in this AEMS is quite easy. The step by step procedure to implement AEMS, is given in Fig. 3(c).

V. SIMULATED RESULTS

This system is designed and developed in Simulink/ MATLAB platform and simulated results are depicted here. The parameters of IMD is listed in Appendix. A 7-level CHB-inverter has two PMs per phase, and their output voltages (v_1), (v_2) and phase voltage (v_{an}), are depicted in Fig. 4(a). The primary (i_s) and secondary (i_{s1}, i_{s2}, i_{s3}, i_{s4}, i_{s5} and i_{s6}) currents of the transformer, are depicted in Fig. 4(b). These secondary currents have similar waveforms however, time phase-shift is in them. The steady state performance of VCIMD is depicted

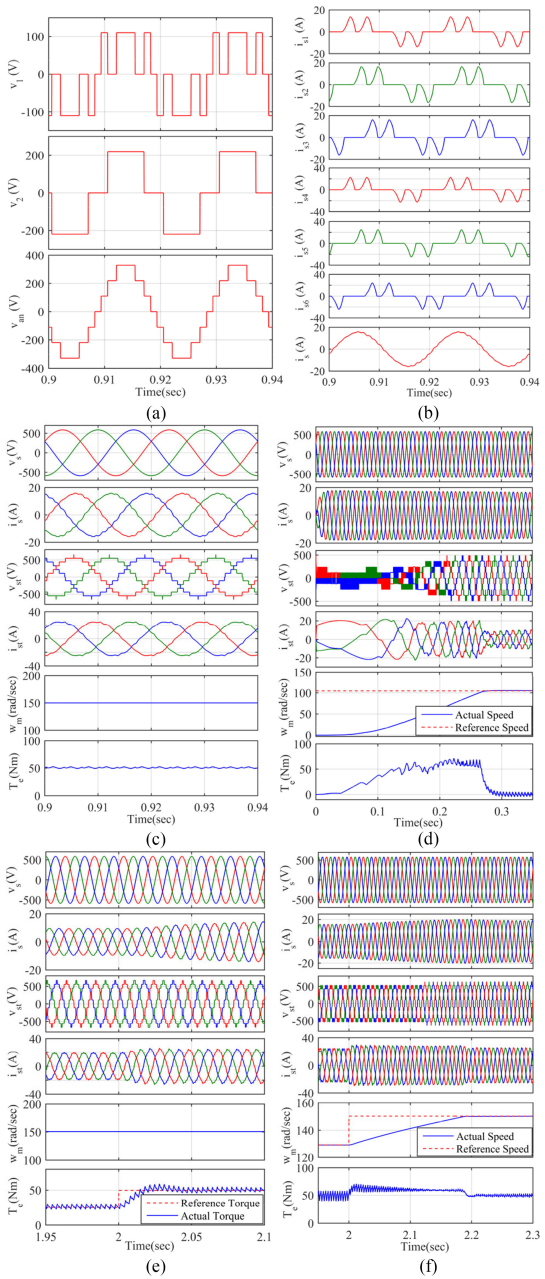

FIGURE 4. Simulated results (a) PM voltage and their sum, (b) transformer secondary and primary windings currents, (c) steady state results, (d) starting results, (e) load changed results and (f) speed control results.

in Fig. 4(c). Here, one can observe that the VCIMD demonstrates good steady state performance on front end and IM end.

The starting performance of VCIMD is depicted in Fig. 4(d). In this response, references speed is fixed at 1000 rpm (104.72 rad/s). The load perturbation performance is depicted in Fig. 4(e). In load perturbation, the drive is operated at half load. At t = 2 s, the reference torque is changed from half to rated value. The speed control results of the VCIMD, is depicted in Fig. 4(f). In this response, the drive is operating at 1240 rpm (129.85 rad/s). At t = 2 s, the speed is changed from 1240 rpm to 1440 rpm (150.8 rad/s).

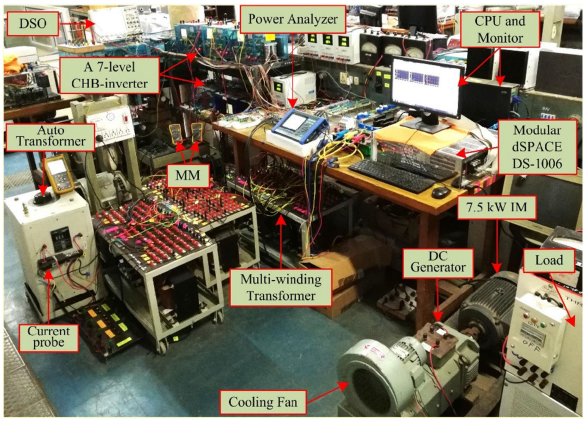

FIGURE 5. Photograph of experimental prototype.

VI. EXPERIMENTAL PERFORMANCES

A prototype of the system is developed with a DSP (dSPACE-DS1006). The parameters of IMD, which are used in the implementation, are given in Appendix. An indirect vector control is implemented by means of two Hall-Effect current sensors (LA-55p) and one speed sensor. Three reference voltages signals (v_a, v_b and v_c) produced from an IVC, are given to AEMS, which generates pulses to control a 7-level inverter as per the drive requirement. The characteristics of the drive are depicted here at varying operating conditions of IMD, to demonstrate input voltage (v_s), input current (i_s), stator line voltage (v_{st}), current (i_{st}), speed (ω_m), d-axis current (i_d), q-axis current (i_q) and torque (T_e). The photograph of prototype is depicted in Fig. 5.

A. STEADY STATE PERFORMANCES

The transformer secondary winding currents (i_{s1}, i_{s2}, i_{s3} and i_{s4}) waveforms are depicted in Fig. 6(a). First three plots of this figure, show the currents drawn by the first group. They show identical waveforms. However, there is a time phase shift in them. Since of phase shifts of $+20°$, $0°$ and $-20°$ among three sets of voltages, the last current waveform (i_{s4}) of this figure, represents the current of second group, which feeds the power to the second PM of each leg, with $2V_{dc}$ voltage. This current is plotted once more in Fig. 6(b) to study performance of all secondary winding currents of MWT. The behavior of second groups currents is plotted in Fig. 6(b).

The currents (i_{s4}, i_{s5} and i_{s6}) waveforms in Fig. 6(b), have similar patterns, though, there is a time shift in them. These currents (i_{s1}, i_{s2}, i_{s3}, i_{s4}, i_{s5} and i_{s6}) of the multi-winding transformer, are transferred to input side and the resulting current (i_s) waveform, is depicted in Fig. 6(b). This current represents an 18-pulse input current waveform. The transformer windings currents given in Fig. 4(b) and also given in Figs. 6(a)–6(b). From these two simulated and experimental results one

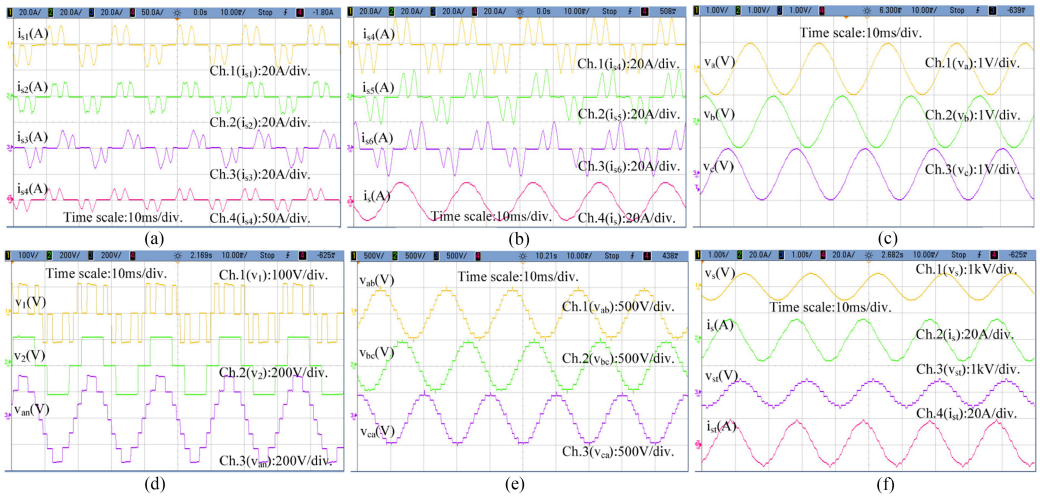

FIGURE 6. Experimental results (a) transformer currents (i_{s1}, i_{s2}, i_{s3}, i_{s4}), (b) transformer currents (i_{s4}, i_{s5}, i_{s6}, i_s), (c) modulating signals generated from IVC and input for AEMS, (d) PM voltage and their sum, (e) three phase motor line voltage and (f) steady state results of proposed system.

TABLE 1. Comparison of Proposed AEMS With SHE Technique

SL.	Speed (RPM)	Proposed AEMS				SHE Technique			
		V_{st} (rms)(V)	i_{st} (rms)(A)	V_{st} (THD%)	i_{st} (THD%)	V_{st} (rms)(V)	i_{st} (rms)(A)	V_{st} (THD%)	i_{st} (THD%)
1.	1440	361.09	13.151	8.62	4.15	361.36	14.226	8.52	3.93
2.	1385	351.93	11.992	8.45	4.70	344.73	13.52	9.63	6.70
3.	1242	328.50	10.890	9.09	5.39	297.20	12.863	14.83	13.02
4.	955	252.51	8.968	9.28	6.24	236.62	9.959	13.84	12.67
5.	764	205.36	7.912	9.36	8.55	175.75	9.000	21.49	25.60

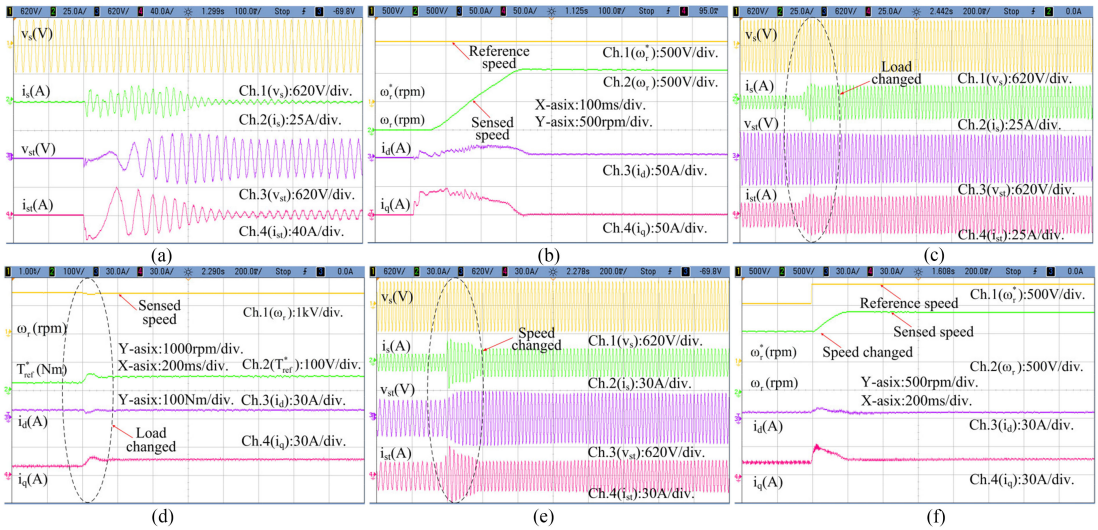

FIGURE 7. Dynamic results (a) starting result, (b) internal signals through starting, (c) load change results, (d) internal signals through load change, (e) speed change result, (f) internal signals through speed change.

can say that the simulated results are verified from experimental results. The three-phase voltage reference signals, which are the output of IVC are depicted in Fig. 6(c). The module output voltage and a-phase voltage waveforms are depicted in Fig. 6(d). The 'v_1' and 'v_2' of this figure, represent outputs of first and second PMs, respectively. The 'v_{an}' of this figure represents the sum of first two waveforms or the a-phase voltage of 7-level CHB-inverter. The power module output voltage and their sum are depicted in Fig. 4(a) and Fig. 6(d). From these two simulated and experimental results, one can say that the simulated results are confirmed from experimental results.

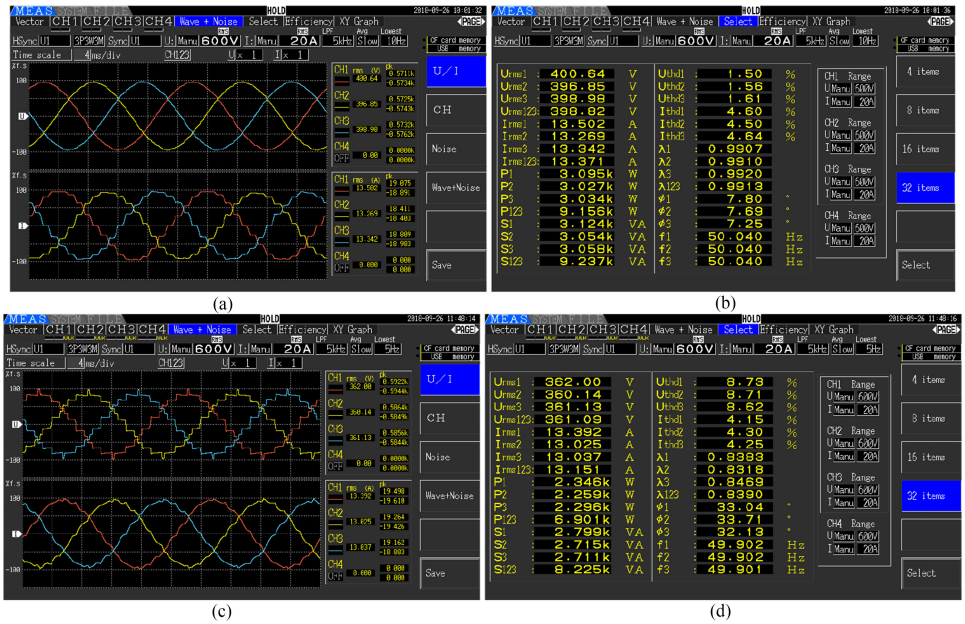

FIGURE 8. Recorded parameters at utility and motor end (a) 3-phase input voltage and currents waveforms at utility end, (b) recorded parameters at utility end, (c) three phase v_{st} and i_{st} waveforms, and (d) recorded parameters on motor terminals.

Three phase motor line voltages (v_{ab}, v_{bc} and v_{ca}) of IMD are depicted in Fig. 6(e). Fig. 6(f) demonstrates the test results of MVIMD. From this, it is realized that the system demonstrates good performance. The performance comparison of proposed AEMS with existing SHE technique are given in Table 1. For this comparison, the configuration of an 18-pulse AC-DC converter fed 7-level binary CHB-inverter is controlled by AEMS and SHE techniques and results are given in Table 1.

B. TRANSIENT RESPONSE

The starting behavior of the system is depicted in Figs. 7(a)–7(b). Here, the primarily speed is set to 1100 rpm. The motor speed (sensed speed) of the IMD, is depicted in Fig. 7(b), which is started from zero and moving to pre-set speed (1100 rpm). The behavior of MVIMD at change of the load, is depicted in Figs. 7(c)–7(d). In these waveforms, IMD is operating at 10% of nominal load. Then the load is raised to nominal value. The speed control of the drive is depicted in Figs. 7(e)–7(f). In it, the speed is increased from 1050 rpm to 1440 rpm.

C. RECORDED POWER QUALITY

The 3-phase waveforms of v_s, i_s, v_{st} and i_{st} are depicted in Fig. 8(a). The voltages (V_{rms1}, V_{rms2}, V_{rms3} and V_{rms123}), currents (I_{rms1}, I_{rms2}, I_{rms3} and I_{rms123}), per phase active power and total active power (P_1, P_2, P_3 and P_{123}), per phase and total power (S_1, S_2, S_3 and S_{123}), THD of line voltages (V_{thd1}, V_{thd2} and V_{thd3}) and currents (I_{thd1}, I_{thd2} and I_{thd3}), power factor (λ_1, λ_2, λ_3, λ_{123}), angles between voltage and current (ϕ_1, ϕ_2, ϕ_3), frequency (f_1, f_2 and f_3), are recorded and depicted in Fig. 8(b). In this, 9.237 kVA is the input power of MWT with 0.9913 PF. The THDs of v_s and i_s are 1.56% and 4.50%, correspondingly. The three-phase v_{st} and i_{st} waveforms are shown in Fig. 8(c). The above-mentioned parameters are also measured at IM terminals and depicted in Fig. 8(d). In this, the THDs of v_{st} and i_{st} are 8.71% and 4.30%, respectively.

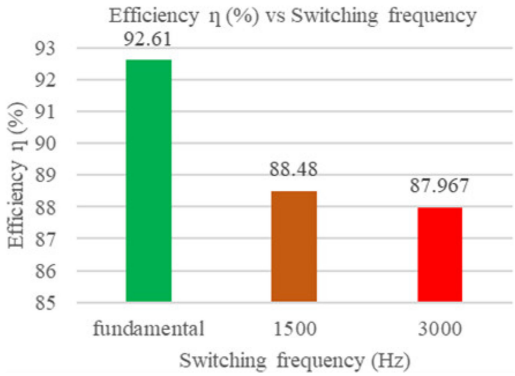

FIGURE 9. Bar-chart diagram of efficiency vs. switching frequency.

D. EFFICIENCY OF MVIMD

The bar-chart diagram of efficiency is depicted in Fig. 9, which represent the comparison of efficiency of an 18-pulse AC-DC converter fed 7-level binary CHB-inverter based IMD when it is controlled by proposed AEMS and existing phase disposition (PD) sinusoidal pulse width modulation (SPWM) technique with carrier frequency equal to 1500 and 3000 Hz.

VII. CONCLUSION

A delta-polygon eighteen-pulse AC-DC conversion fed 7-level CHB-inverter driven MVIMD has been used to enhance

the power quality at front end and motor end. An eighteen pulse AC-DC conversion has made 'i_s' almost sinusoidal with less THD within adequate limit according to the IEEE-519 standard. A 7-level MLI has been used in this work to reduce the numbers of power semiconductor switches and required less numbers of DC-supplies. Due to which, the MVIMD has less size and low cost than existing IMD. An IVC has been utilized to control an IM and to achieve better dynamic response of the IMD than scalar control. An AEMS has been proposed to operate 7-level CHB-inverter as per drive requirement. The inverter output voltage frequency is dependent on reference voltage signal generated from an IVC. A 7-level CHB-inverter fed IM has improved the performance of MVIMD. The AEMS operates a 7-level MLI at FFS, which decreases switching losses and enhances the efficiency of MVIMD. The performances of MVIMD have been experimentally achieved to confirm the decent operation of delta-polygon eighteen-pulse AC-DC converter-fed 7-level CHB-inverter based MVIMD with allowable THD of voltage and current on grid side.

APPENDIX

Parameters of a 7.5 kW (10 hp), 4 pole, 415 V, 50 Hz, $R_s = 0.044$ pu, $R_r = 0.0305$ pu, $L_{ls} = 0.0665$ pu, $L_{lr} = 0.0665$ pu, $L_m = 1.642$ pu and $J = 0.10$ kg-m^2.

REFERENCES

[1] K. Saito and H. Akagi, "A real-time real-power emulator of a medium-voltage high-speed induction motor loaded with a centrifugal compressor," *IEEE Trans. Ind. Appl.*, vol. 55, no. 5, pp. 4821–4833, Sep./Oct. 2019.

[2] N. A. Azeez, K. Gopakumar, J. Mathew, and C. Cecati, "A harmonic suppression scheme for open-end winding split-phase IM drive using capacitive filters for the full speed range," *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp. 5213–5221, Oct. 2014.

[3] P. Kant and B. Singh, "Multi-pulse AC–DC converter fed SVM controlled NPC inverter based VCIMD," *IET Power Electron.*, vol. 11, no. 14, pp. 2204–2214, 2018.

[4] S. C. Richu and P. P. Rajeevan, "A load commutated multilevel current source inverter fed open-end winding induction motor drive with regeneration capability," *IEEE Trans. Power Electron.*, vol. 35, pp. 816–825, 2020, Early Access.

[5] M. Ghosh Majumder, A. K. Yadav, K. Gopakumar, K. R. R, U. Loganathan, and L. G. Franquelo, "A five-level inverter scheme using single DC link with reduced number of floating capacitors and switches for open-end IM drives," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 960–968, Feb. 2020.

[6] B. Singh, V. Garg, and G. Bhuvaneswari, "Polygon-connected autotransformer-based 24-pulse AC–DC converter for vector-controlled induction-motor drives," *IEEE Trans. Ind. Electron.*, vol. 55, no. 1, pp. 197–208, Jan. 2008.

[7] B. Singh, V. Garg, and G. Bhuvaneswari, "A novel T-connected autotransformer-based 18-pulse AC–DC converter for harmonic mitigation in adjustable-speed induction-motor drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2500–2511, Oct. 2007.

[8] P. Liu, S. Duan, C. Yao, and C. Chen, "A double modulation wave CBPWM strategy providing neutral-point voltage oscillation elimination and CMV reduction for three-level NPC inverters," *IEEE Trans. Ind. Electron.*, vol. 65, no. 1, pp. 16–26, Jan. 2018.

[9] W. Wang, B. Zhang, and F. Xie, "A novel SVPWM for three-level NPC inverter based on m-mode controllability," *IEEE Trans. Ind. Electron.*, vol. 65, no. 8, pp. 6055–6065, Aug. 2018.

[10] A. M. Y. M. Ghias, J. Pou, V. G. Agelidis, and M. Ciobotaru, "Voltage balancing method for a flying capacitor multilevel converter using phase disposition PWM," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6538–6546, Dec. 2014.

[11] A. Abdelhakim, P. Mattavelli, and G. Spiazzi, "Three-phase three-level flying capacitors split-source inverters: Analysis and modulation," *IEEE Trans. Ind. Electron.*, vol. 64, no. 6, pp. 4571–4580, Jun. 2017.

[12] P. W. Hammond, "Enhancing the reliability of modular medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 948–954, Oct. 2002.

[13] H. Akagi, "Multilevel converters: Fundamental circuits and systems," *Proc. IEEE*, vol. 105, no. 11, pp. 2048–2065, Nov. 2017.

[14] X. Liang and J. He, "Load model for medium voltage cascaded H-bridge multi-level inverter drive systems," *IEEE Power Energy Technol. Syst. J.*, vol. 3, no. 1, pp. 13–23, Mar. 2016.

[15] X. Wu, C. Xiong, S. Yang, H. Yang, and X. Feng, "A simplified space vector pulse-width modulation scheme for three-phase cascaded H-bridge inverters," *IEEE Trans. Power Electron*, vol. 35, no. 4, pp. 4192–4204, Apr. 2020.

[16] H. Zhao, S. Wang, and A. Moeini, "Critical parameter design for a cascaded H-bridge with selective harmonic elimination/compensation based on harmonic envelope analysis for single-phase systems," *IEEE Trans. Ind. Electron.*, vol. 66, no. 4, pp. 2914–2925, Apr. 2019.

[17] C. Buccella, C. Cecati, M. G. Cimoroni, and K. Razi, "Analytical method for pattern generation in five-level cascaded H-Bridge inverter using selective harmonic elimination," *IEEE Trans. Ind. Electron.*, vol. 61, no. 11, pp. 5811–5819, Nov. 2014.

[18] F. L. Luo and H. Ye, *Advanced DC/AC Inverters Applications in Renewable Energy*," New York, NY, USA: CRC Press Taylor & Francis Group, 2013.

[19] P. Hu and D. Jiang, "A level-increased nearest level modulation method for modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 1836–1842, April 2015.

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