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A Novel Discontinuous PWM Method With Hybrid Three-Step Commutation to Reduce Common-Mode Voltage for Direct Matrix Converter

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ABSTRACT The conventional discontinuous pulsewidth modulation (PWM) can provide several advantages in a direct matrix converter (DMC), such as less switching number and less execution time for modulation signals' calculation. However, it suffers from high common-mode voltage (CMV), which may cause damage to the DMC-based system. This article proposes a novel discontinuous PWM (DPWM) method to not only mitigate CMV but also further improve the conversion efficiency. In this method, the switching sequence is obtained in a new way using two medium and two small input line voltages, increasing the conversion efficiency. Besides, the proposed DPWM employs a rotating vector instead of a zero vector, which causes the CMV to reduce by 50% compared with the conventional DPWM. Notably, the proposed DPWM provides the above advantages while maintaining low total harmonic distortion (THD). Simulations and experiments have been conducted to verify the proposed DPWM method's effectiveness. The results of these tests support the claims made in the paper regarding the reduction of CMV, improved efficiency, and low THD.

INDEX TERMS Common-mode voltage (CMV), commutation method, direct matrix converter (DMC), discontinuous pulsewidth modulation (DPWM), efficiency.

I. INTRODUCTION

Direct matrix converters (DMCs) can perform direct ac-to-ac (ac/ac) conversion without requiring energy storage components (dc-link capacitors). Since there is no dc link, the DMC is more compact and has higher power densities than back-to-back converter [1]. Additionally, DMC can control the input power factor and provide bidirectional power flow. In fact, this topology has the capability to achieve a power factor close to unity, irrespective of the load power factor.

Generally, DMC consists of nine groups of bidirectional power semiconductor switches, as illustrated in Fig. 1, resulting in 27 viable switching states [2]. These switching states are classified into three categories, as listed in Table 1. The first category consists of 18 active vectors, each with a predetermined angular position corresponding proportionally to the phase-to-phase voltage of a single input phase. The second category consists of three zero vectors, which enable

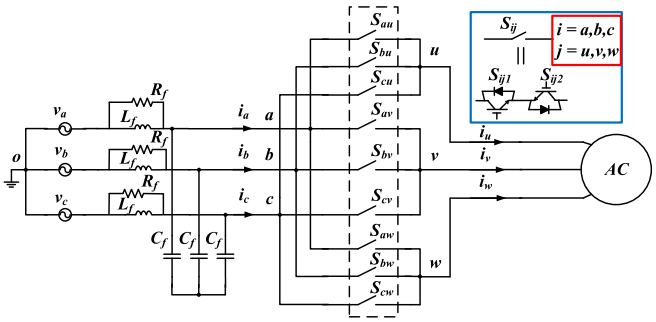


FIGURE 1. DMC topology.

TABLE 1 Switching States in Matrix Converter

	No.	u v w	V_o	α_o	i_i	β_i	CMV
Active Vector	+1	a b b	$2/3V_{ab}$	0	$2/\sqrt{3}\, i_u$	$-\pi/6$	$\frac{1}{3}v_{bc}$
	-1	b a a	$-2/3V_{ab}$	0	$-2/\sqrt{3}\, i_u$	$-\pi/6$	$\frac{1}{3}v_{ac}$
	+2	b c c	$2/3V_{bc}$	0	$2/\sqrt{3}\, i_u$	$\pi/2$	$\frac{1}{3}v_{ca}$
	-2	c b b	$-2/3V_{bc}$	0	$-2/\sqrt{3}\, i_u$	$\pi/2$	$\frac{1}{3}v_{ba}$
	+3	c a a	$2/3V_{ca}$	0	$2/\sqrt{3}\, i_u$	$7\pi/6$	$\frac{1}{3}v_{ab}$
	-3	a c c	$-2/3V_{ca}$	0	$-2/\sqrt{3}\, i_u$	$7\pi/6$	$\frac{1}{3}v_{cb}$
	+4	b a b	$2/3V_{ab}$	$2/3\pi$	$2/\sqrt{3}\, i_v$	$-\pi/6$	$\frac{1}{3}v_{bc}$
	-4	a b a	$-2/3V_{ab}$	$2/3\pi$	$-2/\sqrt{3}\, i_v$	$-\pi/6$	$\frac{1}{3}v_{ac}$
	+5	c b c	$2/3V_{bc}$	$2/3\pi$	$2/\sqrt{3}\, i_v$	$\pi/2$	$\frac{1}{3}v_{ca}$
	-5	b c b	$-2/3V_{bc}$	$2/3\pi$	$-2/\sqrt{3}\, i_v$	$\pi/2$	$\frac{1}{3}v_{ba}$
	+6	a c a	$2/3V_{ca}$	$2/3\pi$	$2/\sqrt{3}\, i_v$	$7\pi/6$	$\frac{1}{3}v_{ab}$
	-6	c a c	$-2/3V_{ca}$	$2/3\pi$	$-2/\sqrt{3}\, i_v$	$7\pi/6$	$\frac{1}{3}v_{cb}$
	+7	b b a	$2/3V_{ab}$	$4/3\pi$	$2/\sqrt{3}\, i_w$	$-\pi/6$	$\frac{1}{3}v_{bc}$
	-7	a a b	$-2/3V_{ab}$	$4/3\pi$	$-2/\sqrt{3}\, i_w$	$-\pi/6$	$\frac{1}{3}v_{ac}$
	+8	c c b	$2/3V_{bc}$	$4/3\pi$	$2/\sqrt{3}\, i_w$	$\pi/2$	$\frac{1}{3}v_{ca}$
	-8	b b c	$-2/3V_{bc}$	$4/3\pi$	$-2/\sqrt{3}\, i_w$	$\pi/2$	$\frac{1}{3}v_{ba}$
	+9	a a c	$2/3V_{ca}$	$4/3\pi$	$2/\sqrt{3}\, i_w$	$7\pi/6$	$\frac{1}{3}v_{ab}$
	-9	c c a	$-2/3V_{ca}$	$4/3\pi$	$-2/\sqrt{3}\, i_w$	$7\pi/6$	$\frac{1}{3}v_{cb}$
Zero Vector	0_a	a a a	0	-	0	-	v_a
	0_b	b b b	0	-	0	-	v_b
	0_c	c c c	0	-	0	-	v_c
Rotating Vector	r_1	a b c	V_i	α_i	I_o	β_o	0
	r_2	a c b	V_i	$-\alpha_i$	I_o	$-\beta_o$	0
	r_3	c a b	V_i	$2/3\pi + \alpha_i$	I_o	$-2/3\pi + \beta_o$	0
	r_4	b a c	V_i	$2/3\pi - \alpha_i$	I_o	$2/3\pi - \beta_o$	0
	r_5	b c a	V_i	$-2/3\pi + \alpha_i$	I_o	$2/3\pi + \beta_o$	0
	r_6	c b a	V_i	$-2/3\pi + \alpha_i$	I_o	$-2/3\pi - \beta_o$	0

freewheeling and lead to zero voltage on the load. The third category consists of six rotating vectors, where each input phase is connected to a distinct output phase. Many modulation methods described in the existing literature focus on using active and zero vectors to generate reference vectors, disregarding the rotating vectors.

Despite the advantages of DMCs, they still have specific concerns that need to be addressed, such as the need for commutation methods and common-mode voltage (CMV) reduction methods [3]. The CMV of the 27 switching states for DMC is shown in Table 1. Accordingly, the high-frequency change (dV_{cmv}/dt) of CMV is unavoidable in DMCs, considering the high switching frequency. The high-frequency CMV increases the effect of the parasitic capacitance between the wire and the ground and forms a leakage current. The flow of leakage current may cause the DMC-based system to be damaged, for example, damaging the motor bearing and shortening the service life of the motor. Therefore, CMV concern is of the highest importance, and exploring and implementing methods to reduce the CMV associated with DMC becomes crucial. There are several advanced modulation methods available to reduce the CMV of DMCs. These methods are categorized into space vector modulation (SVM) [4], [5], and pulsewidth modulation (PWM) [6]. SVM provides greater flexibility in designing switching sequences and a better understanding of the modulation process. However, it is more complex to implement. In contrast, PWM is easier to implement SVM in a popular method for reducing the CMV of DMC [7]. SVM methods can be categorized as indirect SVM (ISVM) and direct SVM (DSVM). In ISVM, the CMV peak is reduced to 34% by optimizing zero vectors [8] or using four active vectors for the desired output voltage [9]. DSVM, known for its direct power conversion and absence of third-harmonic components [10], is more appealing for CMV reduction in DMC. Several DSVM techniques have been developed to limit the CMV peak to 42% by replacing zero vectors with active vectors [11], rotating vectors [12], or lower input phase-to-phase voltages [13]. In [14], they used active vectors instead of zero vectors in DSVM methods due to having a smaller CMV of active vectors than zero vectors. Although the above methods effectively reduce the CMV, they often increase switching losses and negatively impact the efficiency of the DMC. Additionally, DSVM methods are usually limited in their voltage transfer ratio (q, the output voltage amplitude divided by the input voltage amplitude) or may increase total harmonic distortion (THD) [15].

On the other hand, some methods based on PWM can be used to reduce CMV. These PWM methods can be categorized into continuous PWM (CPWM) and discontinuous PWM (DPWM). CPWM has better THD but increases the switching number compared with DPWM. Accordingly, DPWM may be a better option in DMC applications, as it can reduce switching losses and lead to higher efficiency [16].

In [17], a CPWM method for mitigating CMV is proposed using deadtime compensation. Lei et al. [18] discuss a developed CPWM method with reduced CMV, limiting the number of switches during the modulation period. Other methods based on DPWM for mitigating CMV have also been proposed in [19] and [20]. However, these methods are only for IMC, not DMC.

In [21], a DPWM for DMC is proposed to achieve a unity input power factor and less calculation of modulation signals. Besides, this DPWM effectively lowers switching losses by reducing the number of switching events, resulting in improved efficiency. In [22], a high-efficiency DPWM method is proposed by rearranging the switching sequence presented in [21]. Although the above methods can make practical implementation easier and improve the DMC performance, they have not paid attention to CMV, which is a crucial reliability concern for DMC-based systems.

This article proposes a novel DPWM method to not only mitigate CMV but also further improve the conversion efficiency. The main contributions provided by this method can be counted as follows.

1) The proposed method obtained the switching sequence in a new way using two medium and two small input line voltages, which increases the conversion efficiency.
2) The proposed method employs a rotating vector instead of a zero vector, which causes the CMV to be reduced by 50% compared with the conventional DPWM.
3) While using rotating vectors to achieve lower CMV increases the proposed method's complexity relatively, it is developed through a carrier-based modulation technique, simplifying practical implementation. This possibility of carrier-based implementation indicates an acceptable tradeoff between the benefits of reduced CMV and the complexity involved in the proposed method.
4) The proposed method provides the above advantages while maintaining low THD.
5) The proposed method employs a new hybrid three-step commutation with the advantages of canceling output voltage error, making the change of the output current easy and decreasing the input current's THD.

The rest of this article is organized as follows. Section II provides a brief explanation of the principle of the conventional DPWM method and the conversion matrix. Section III presents the principle of the proposed DPWM method and the commutation strategy. Section IV focuses on the simulation and experimental verification of the proposed modulation method. Finally, Section V concludes this article.

II. DPWM METHODS' PRINCIPLES AND BACKGROUNDS

In this section, the fundamental principles of the DPWM method are introduced. Afterward, the two existing DPWM methods are investigated briefly, considering that the proposed method of this article will be compared with them.

A. DPWM METHODS' PRINCIPLES

To better explain the principle of the DPWM, this section presents the process of generating modulation signals to synthesize output voltages. Noteworthy that the comprehensive explanation can be found in [21] and [22], while the summary is presented in the following.

DMC must hold to the specified switching state outlined in (1) to prevent short circuits at the input and open circuits at the output

$$\begin{cases} S_{au} + S_{bu} + S_{cu} = 1 \\ S_{av} + S_{bv} + S_{cv} = 1 \\ S_{aw} + S_{bw} + S_{cw} = 1. \end{cases} \tag{1}$$

The DPWM method employs four active vectors to generate the switching sequence. The two largest input line voltages are used to determine the output line voltages, while a zero-voltage vector is connected to the output voltages during a switching cycle. DPWM only requires the calculation of four modulation signals. The conversion matrix $[M]$ is defined based on the input voltage and output voltage references, as explained in the Appendix. It comprises nine modulation signals, denoted as m_{xy}, as shown in the following equation:

$$[M] = \begin{bmatrix} m_{au} & m_{av} & m_{aw} \\ m_{bu} & m_{bv} & m_{bw} \\ m_{cu} & m_{cv} & m_{cw} \end{bmatrix}. \tag{2}$$

The DPWM method calculates the modulation signals to create a conversion matrix $[M]$. Each column of $[M]$ must have one modulation signal equal to 1 to prevent short circuits at the input terminal and open circuits at the output terminal in DMC. The modulation signal for the process of synthesizing output line voltage can be obtained from large, medium, and small input line voltages, and the maximum q for this method is 0.75. Assuming that the input three-phase voltage is balanced, the largest and second-largest input line voltages (v_{ab}, v_{bc}, v_{ac}) are used, and the minimum input line voltage is replaced by (3). Synthesizing output line voltage V_{uv}^* is shown in (4). The modulation signal is proportional to the input line voltage, with the coefficient represented by (5)–(7)

$$V_{bc} = -V_{ab} + V_{ac} \tag{3}$$

$$V_{uv}* = \alpha_1 V_{ab} + \alpha_2 V_{ac} + \alpha_0 V_0 \tag{4}$$

$$\alpha_1 = \frac{(V_{ab} - V_{bc})V_{uv}*}{({V_{ab}}^2 + {V_{bc}}^2 + {V_{ca}}^2)} \tag{5}$$

$$\alpha_2 = \frac{(V_{bc} - V_{ca})V_{uv}*}{({V_{ab}}^2 + {V_{bc}}^2 + {V_{ca}}^2)} \tag{6}$$

$$\alpha_0 = 1 - (\alpha_1 + \alpha_2) \tag{7}$$

where α_1, α_2, and α_0 are the coefficients proportional to the input line voltage, which must be between 0 and 1. The process of generating V_{uw}^* is shown in the following equations:

$$V_{uw}* = b_1 V_{ab} + b_2 V_{ac} + b_0 V_0 \tag{8}$$

$$b_1 = \frac{(V_{ab} - V_{bc})V_{uw}*}{({V_{ab}}^2 + {V_{bc}}^2 + {V_{ca}}^2)} \tag{9}$$

$$b_2 = \frac{(V_{bc} - V_{ca})V_{uw}*}{({V_{ab}}^2 + {V_{bc}}^2 + {V_{ca}}^2)} \tag{10}$$

$$b_0 = 1 - (b_1 + b_2). \tag{11}$$

DPWM needs to allocate intervals based on the input and output voltage phases. Additionally, to always use the two largest input line voltages and block (no switching) one output phase out of the three output phases in the DPWM method, it is necessary to have a permanent connection between the absolute greatest input voltage and the absolute greatest output voltage with the same sign as the input voltage. The input and output intervals need to be defined based on their respective values. First, the input voltage is divided into six intervals, and then the reference output voltage is assigned to each interval (positive and negative), as shown in Figs. 2 and 3, respectively. Nine ranges of combination input and output intervals can be defined: au, bu, cu, av, bv, cv, aw, bw, and cw. When the input interval is $a+$, and the output interval is $u+$, or when the input interval is $a-$, and the output interval

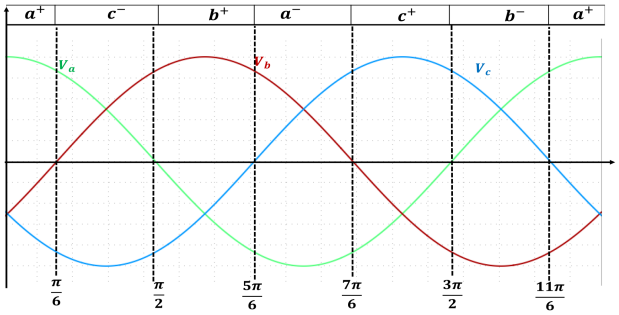


FIGURE 2. Input voltage range allocation.

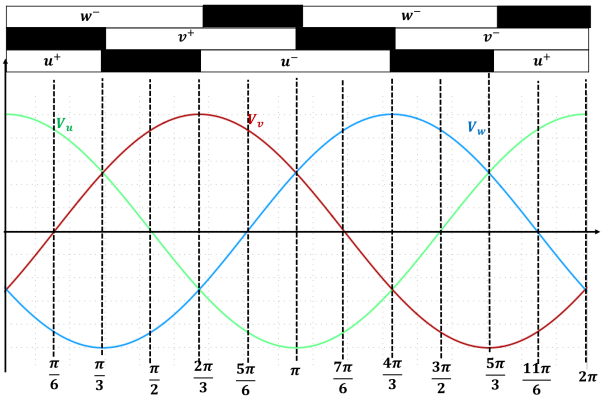


FIGURE 3. Reference output voltage range allocation.

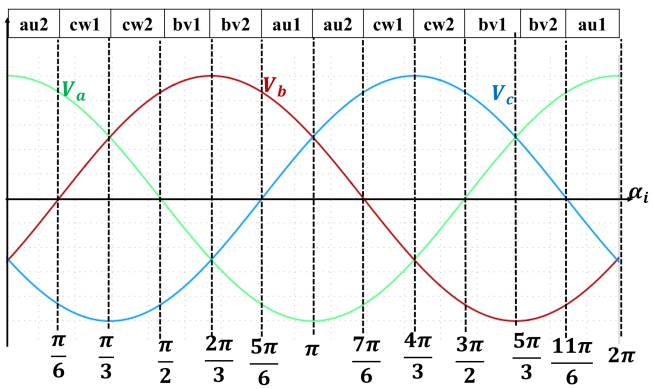


FIGURE 4. Schematic diagram of voltage range (final interval).

is $u-$, it is named interval au. Similarly, other combinations, such as bu, cu, av, bv, cv, aw, bw, and cw are named based on their corresponding input and output intervals. Based on the input and reference output intervals, the final interval for generating DPWM can be determined by combining the two ranges, as shown in Fig. 4. The final conversion matrices are constructed with lines and columns of modulation signals. After generating modulation signals, one of the output phases must be fixed to 1, and then the other two in the lines of $[M]$ are compared with carriers. This is because the control allocation changes over time based on the interval concept.

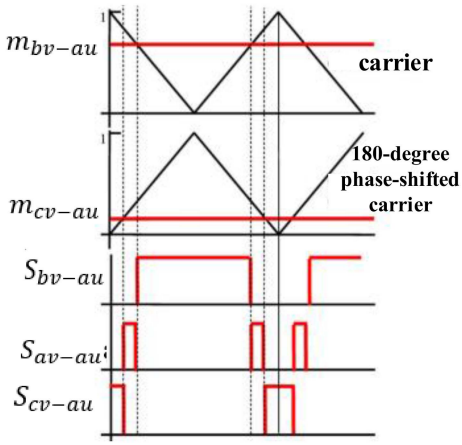


FIGURE 5. Generating switching state in DPWM.

The blocked output phases are chosen based on the greatest input and output voltages, which vary over time. For instance, when the interval is au, the value of m_{au} is set to 1, while m_{bu} and m_{cu} are set to 0, and the modulation signal au is calculated, as shown in (12). Likewise, the modulation signals for other intervals are derived according to the above process, as explained in [21] and represented in the Appendix

$$[M] = \begin{bmatrix} m_{au}=1 & m_{av}=1-m_{bv}-m_{cv} & m_{aw}=1-m_{bw}-m_{tw} \\ m_{bu}=0 & m_{bv}=\frac{(V_{ab}-V_{bc})V_{uv}*}{{V_{ab}}^2+{V_{ac}}^2+{V_{bc}}^2} & m_{bw}=\frac{(V_{ab}-V_{bc})V_{uw}*}{{V_{ab}}^2+{V_{ac}}^2+{V_{bc}}^2} \\ m_{cu}=0 & m_{cv}=\frac{(V_{bc}-V_{ca})V_{uv}*}{{V_{ab}}^2+{V_{ac}}^2+{V_{bc}}^2} & m_{cw}=\frac{(V_{bc}-V_{ca})V_{uw}*}{{V_{ab}}^2+{V_{ac}}^2+{V_{bc}}^2} \end{bmatrix} \tag{12}$$

where ${V_{ab}}^2+{V_{bc}}^2+{V_{ca}}^2$ is a constant and K represents a coefficient, which is shown as follows:

$$K = {V_{ab}}^2+{V_{bc}}^2+{V_{ca}}^2. \tag{13}$$

This DPWM method has the advantage of needing the calculation of only four modulation signals. The other two modulation signals can be computed based on the calculated modulation signals. Due to the similarity between the nine intervals, the interval au is explained as an example. When the interval is au, S_{au} is always on, S_{bu} and S_{cu} are always off. Comparing the modulation signals m_{bv-au} and m_{bw-au} with the carrier to generate switching signals S_{bv-au} and S_{bw-au}, and the modulation signals m_{cv-au} and m_{cw-au} with the 180° phase-shifted carrier, switching signals S_{cv-au} and S_{cw-au} are generated. The signals S_{av-au} and S_{aw-au} are obtained through logic gate (XNOR) operations. S_{bv-au} and S_{cv-au}, and S_{bw-au} and S_{cw-au} are used to get S_{av-au} and S_{aw-au}, respectively. Accordingly, Fig. 5 shows a comparison of the modulation signal with the fixed slope of the carrier and 180° phase-shifted carrier to obtain the switching states for controlling the switches in the DPWM method.

TABLE 2 Vector of Each Interval of DPWM Method

au	+1, -3, -4, +6, -7, +9	0_a	r_1, r_2
av	-1, +3, +4, -6, -7, +9	0_a	r_3, r_4
aw	-1, +3, +4, -6, -7, +9	0_a	r_5, r_6
bu	-1, +2, +4, -5, +7, -8	0_b	r_4, r_5
bv	+1, -2, -4, +5, +7, -8	0_b	r_1, r_6
bw	+1, -2, +4, -5, -7, +8	0_b	r_2, r_3
cu	-2, +3, +5, -6, +8, -9	0_c	r_3, r_6
cv	+2, -3, -5, +6, +8, -9	0_c	r_2, r_5
cw	+2, -3, +5, -6, -8, +9	0_c	r_1, r_4

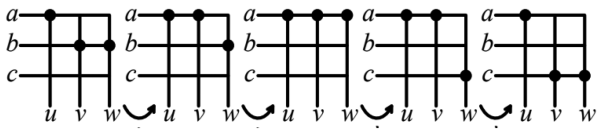


FIGURE 6. Vector sequences of the conventional DPWM in half switching (interval ***au*1**).

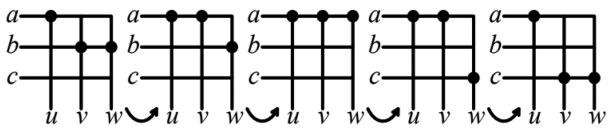


FIGURE 7. Vector sequences of the conventional DPWM in half switching (interval ***au*2**).

According to DPWM, nine types of vectors can be used in each interval. These vectors are selected based on the two greatest input line voltages and applied accordingly: six actives, two rotations, and one zero vector. The interval *au* is described as the output *u*-phase that is fixedly connected to the input *a*-phase. The vectors used in this interval are the active $(+1, -3, -4, +6, -7, +9)$, the zero vector (0_a), and the rotation (r_1 and r_2) vectors. The vectors used in all intervals are arranged in Table 2.

B. EXISTING METHODS OF DPWM

1) CONVENTIONAL DPWM

In [21], the DPWM utilizes the four active vectors and one zero vector to generate switching sequences by switching two large and two medium input line voltages within half a carrier cycle. The vector sequence of the DPWM for *au*1 and *au*2 intervals is displayed in Figs. 6 and 7, respectively, when half a switching period is considered. The DPWM method, developed based on the above switching DPWM, is called conventional DPWM in this article. Note that the vector sequences of conventional DPWM, determined based on the two greatest input line voltages, are the same in intervals *au*1 and *au*2 since the same line voltages are considered as the two greatest input line voltages in the aforementioned intervals.

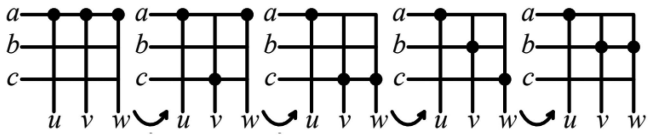


FIGURE 8. High-efficiency DPWM vector sequence for half a switching cycle (interval ***au*1**).

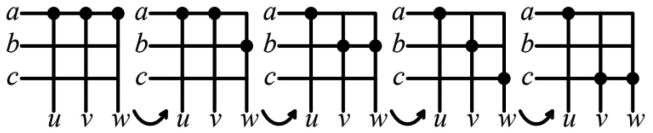


FIGURE 9. High-efficiency DPWM vector sequence for half a switching cycle (interval ***au*2**).

2) HIGH-EFFICIENCY DPWM

In [22], the DPWM uses a different switching sequence than the conventional DPWM in which the switching voltage changes to two medium and two small input line voltages to obtain the switching sequences in half a switching cycle. It employs three active vectors, one zero and one rotation vector, to achieve high efficiency. The vector sequences used to generate the switching signals in half a switching cycle for the intervals *au*1 and *au*2 are shown in Fig. 8 and Fig. 9, respectively. The DPWM method, developed based on the above switching DPWM, is called high-efficiency DPWM in this article.

III. PROPOSED METHOD

This section describes the proposed DPWM, which can reduce CMV while keeping the advantage of the conventional and high-efficiency DPWMs. Besides, it presents the hybrid three-step commutation strategy employed by the proposed method.

A. PROPOSED DPWM METHOD

The proposed method utilizes the DPWM principle to generate the modulation signals, as introduced in Section II. Besides, it employs the same switching sequence as high-efficiency DPWM (refer to Section II-B2) to achieve high efficiency and maximize the q. However, the proposed method employs rotation rather than zero vectors to reduce CMV. Accordingly, three active vectors and two rotation vectors are used in the proposed method. This method allows the extraction of output voltages and input currents proportional to input voltages, which makes the input power factor unity. The switching sequence of the proposed method for the half switching cycle of all intervals is shown in Figs. 10–13. When the interval is *au*1, $|v_{ab}|$ is the large line voltage, $|v_{ca}|$ is the medium line voltage, and $|v_{bc}|$ is the small line voltage. It can be seen from Fig. 10 that the switching voltage of half switching cycle changes into two medium and two small

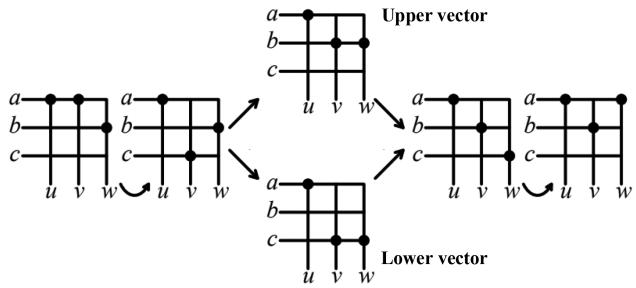


FIGURE 10. Vector sequence of the proposed DPWM in half switching cycle (interval *au*1).

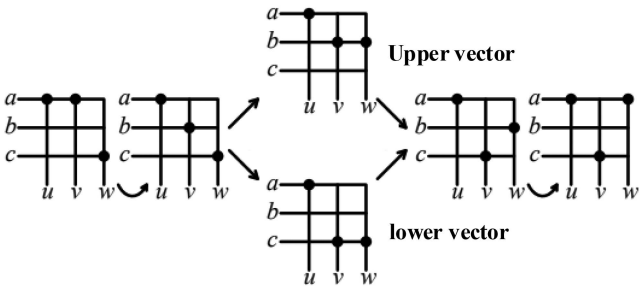


FIGURE 11. Vector sequence of the proposed DPWM in half switching cycle (interval *au*2).

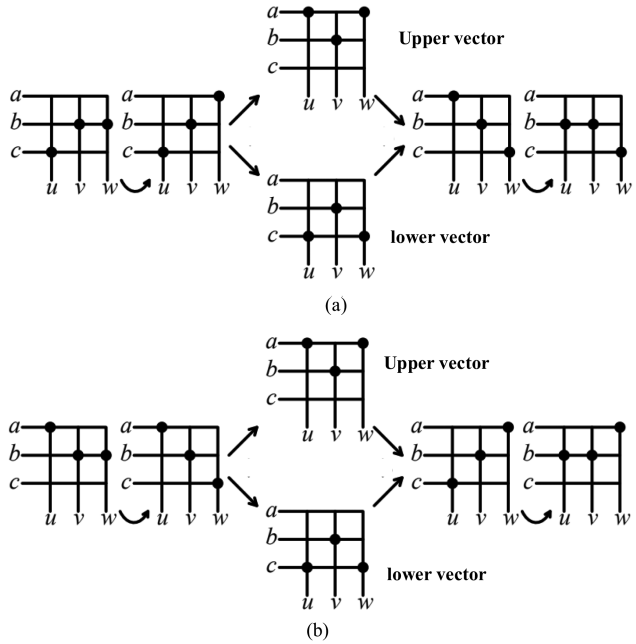


FIGURE 12. Vector sequence of the proposed DPWM in half switching cycle. (a) Interval *bv*1. (b) Interval *bv*2.

input line voltages. Among them, the maximum CMV peak generated by the active vector in this interval is $\frac{1}{2}V_i$, which reduces the peak value of the CMV by half.

When the interval is *au*2, $|v_{ca}|$ is the large line voltage, $|v_{ab}|$ is the medium line voltage, and $|v_{bc}|$ is the small line voltage.

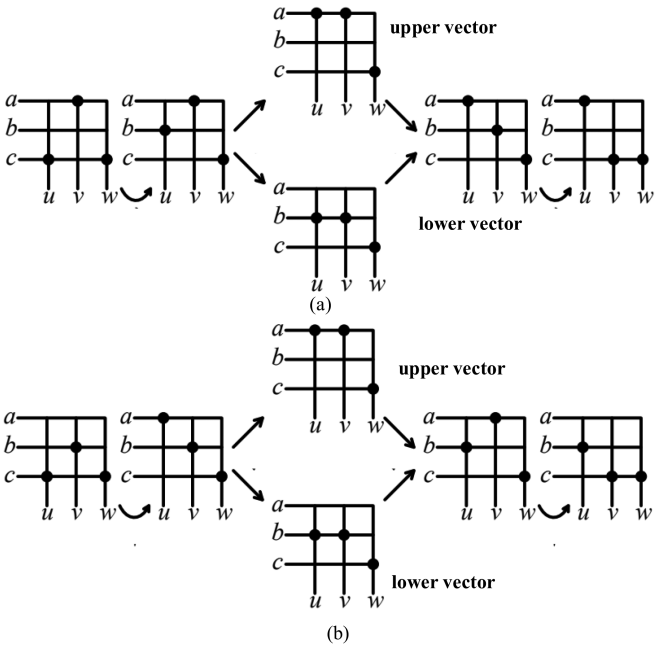


FIGURE 13. Vector sequence of the proposed DPWM in half switching cycle. (a) Interval *cw*1. (b) Interval *cw*2.

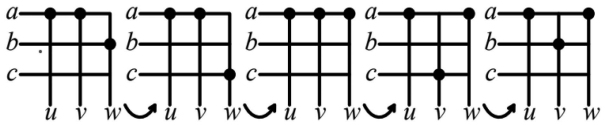


FIGURE 14. Vector sequence in half a switch cycle (interval *au*1).

As can be seen from Fig. 11, the switching voltage of half a switching cycle changes into two medium and two small input line voltages. Among them, the maximum CMV peak generated by the active vector in this interval is $\frac{1}{2}V_i$, which reduces the peak value of the CMV by half.

It can be seen that there are two viable third vectors in each figure. These two vectors can be obtained by comparing carrier waves and the modulation signals with different magnitudes. However, both the upper and lower vectors are consistent with high efficiency and low CMV. Figs. 12 and 13 show the switching sequence for *bv*1 and *bv*2, and *cw*1 and *cw*2, respectively.

Notable the maximum q of the proposed DPWM can reach $\frac{\sqrt{3}}{2}$, and the minimum q is $\frac{1}{2}$. When the q is less than $\frac{1}{2}$, the DPWM must have a zero vector. Consequently, although the proposed method has high efficiency, it cannot achieve low CMV when $q<\frac{1}{2}$. As the interval *au*1 is illustrated as an example, the zero vectors S_{au}, S_{av}, and S_{aw} are turned on at the same time; at this time, the output u-phase is fixedly connected to the input a-phase, and S_{au} is always turned on. To synthesize a lower output voltage, the modulation signal is compared with the carrier, and S_{av} and S_{aw} require a longer on-time. When the sum of the conduction time of S_{av} and the conduction time of S_{aw} exceeds the switching period, there be

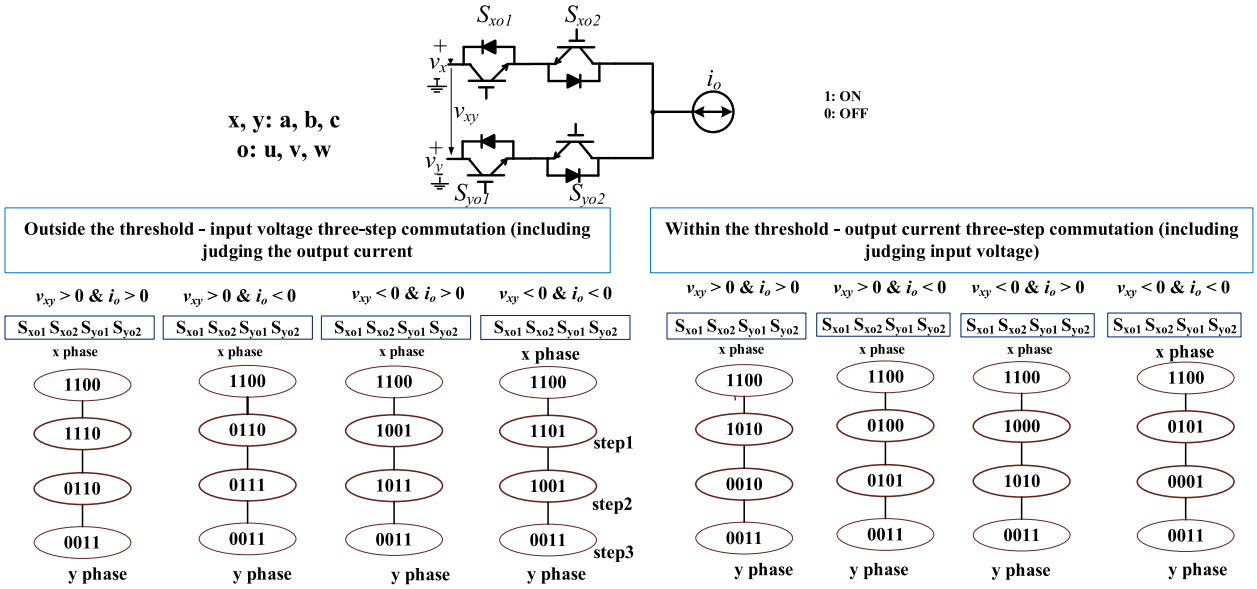


FIGURE 15. Proposed hybrid three-step commutation.

a situation, where S_{au}, S_{av}, and S_{aw} are turned on at the same time, in which a zero vector must be generated, as shown in Fig. 14.

B. PROPOSED HYBRID THREE-STEP COMMUTATION

The commutation of the DMC is categorized into output current, input voltage, and hybrid [23]. Generally, these types of commutation methods can be implemented in four, two, or three steps. The input voltage commutation is introduced based on determining whether the input line voltage is greater or less than zero. If the voltage sensor cannot accurately judge, it results in an error that causes a short circuit at the input end and generates a surge current. Therefore, the threshold is set near the zero-crossing point of the input line voltage, and the setting of the threshold value is according to the accuracy of the voltage sensor.

On the other hand, the output current commutation is introduced based on judging whether the output current is greater or less than zero. If the current sensor cannot accurately judge, it causes an open circuit at the output and surge voltage. Therefore, the threshold is set near the zero-crossing point of the output current [24]. The conventional hybrid commutation uses the output current commutation outside the threshold value, and the input voltage commutation whitens the threshold value. Therefore, there is no commutation within the output current threshold, which causes a problem with surge voltage. There is also no commutation within the input voltage threshold, which causes the issue of adding additional switching losses or results in modulation results that are different from expected [24].

Generally, when output current commutation and input voltage commutation are used, commutation within their threshold should be specifically assessed. Besides, the proposed DPWM method, which minimizes the switching voltage change in input voltage commutation, must employ vector switching of adjacent phase voltages. Therefore, a threshold must be considered near the zero-crossing point of the input line voltage. It is noteworthy that adding additional switching states for commutation increases the number of switching times within the input voltage threshold, resulting in increased switching losses and reduced efficiency. On the other hand, the switching state rearranging in commutation also increases the switching voltage variation and the switching loss within the input voltage threshold, causing the modulation to have a zero vector and making it impossible to achieve a low CMV. Considering the above challenges in employing the commutation method, an appropriate one should be selected to keep the proposed method's primary advantages. Therefore, this article uses a three-step commutation of output current and a three-step commutation of input voltage based on [25] and [26] to form a hybrid three-step commutation that can overcome the above challenges. This proposed commutation method uses input voltage commutation outside the threshold and the output current commutation within the threshold, as illustrated in Fig. 15. Notably, the proposed hybrid commutation can provide additional advantages as follows. First, the output load is easy to change, and as long as the output load and the output current change, the output current threshold is changed accordingly. Second, it also makes the output current smoother or more regular, resulting in a lower THD of the input current.

IV. SIMULATION AND EXPERIMENTAL RESULTS

This section validates the feasibility of the newly proposed method and explains the physical prototype of the DMC. Besides, it analyzes the simulation and experimental results

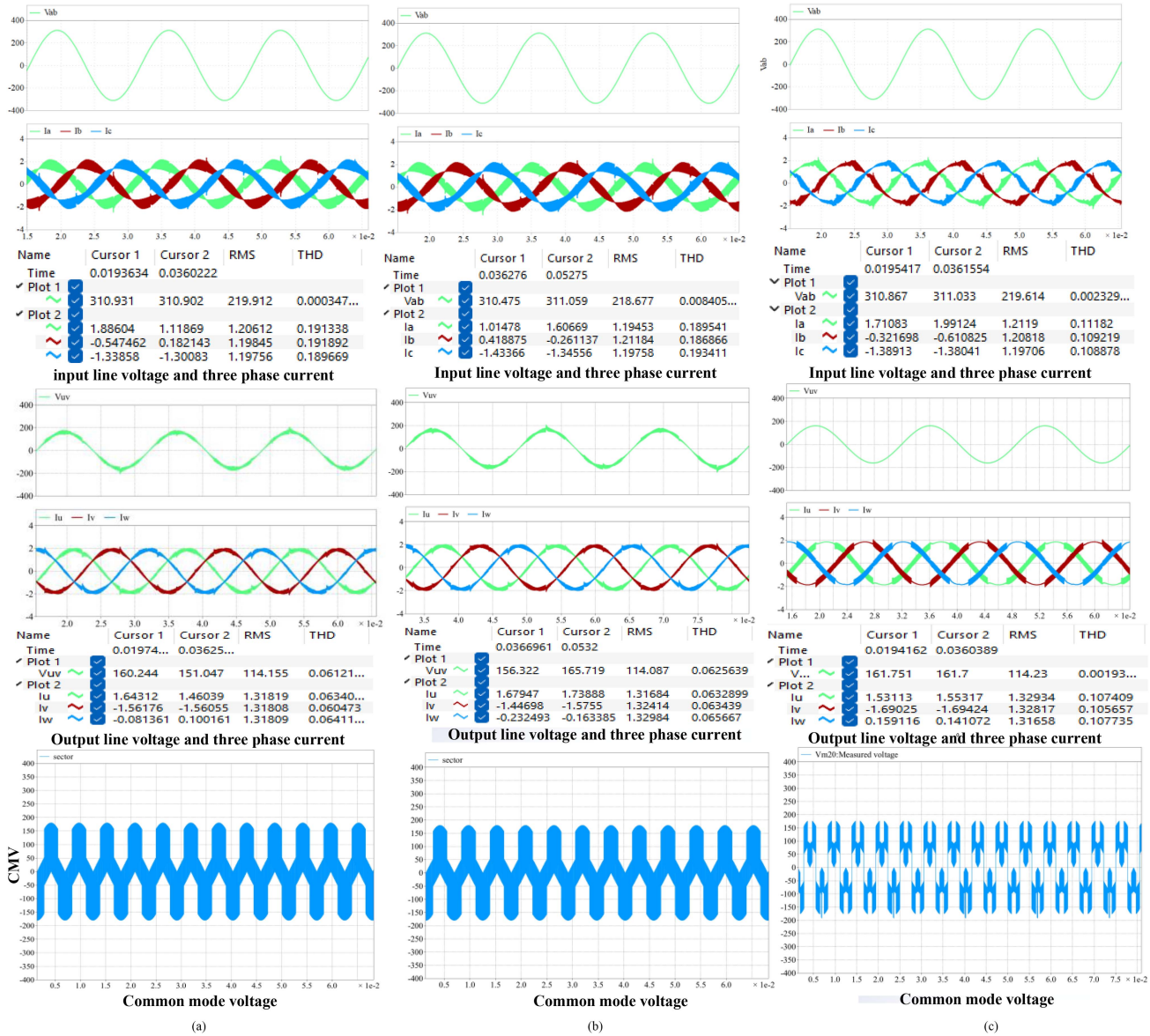


FIGURE 16. Simulation results at $q = 0.5$. (a) Conventional DPWM. (b) High-efficiency DPWM. (c) Proposed DPWM.

to assess the performance of the proposed method. Various parameters of the test system are listed in Table 3. These parameters are considered for both the simulation studies and the experimental setup. t_{step} is commutation time per step, which is used in a commutation strategy to prevent commutation failure [25]. The simulation study is done through the PLECS simulation.

A. SIMULATION RESULTS

Figs. 16 and 17 show the waveforms of input and output voltages, three-phase currents, and CMV of the conventional, high-efficiency, and proposed methods when q is equal to 0.5 and 0.866, respectively. It is verified that a sinusoidal input and output waveform can be generated by the proposed DPWM. Furthermore, it can be seen from Fig. 17(c) that the peak value of CMV for the proposed DPWM method at $q = 0.866$ is reduced by 50% compared with the conventional and high-efficiency DPWM methods. As shown in Fig. 16(c), the proposed method cannot achieve low CMV at $q = 0.5$, although it has high efficiency. Based on the analysis of the simulation results, it is observed that the THD of both the input and output waveforms is reduced using the proposed method. It can be seen from Fig. 16 that the distortion of the input phase current waveform is large when $q = 0.5$. This behavior is mainly attributed to the presence of low-order harmonics in the input voltage. In contrast, when analyzing the input phase current waveform indicated in Fig. 17, it can be seen that it is relatively sinusoidal and has a slight distortion. In addition, it can be seen from Figs. 16 and 17 that all methods have canceled the output voltage error.

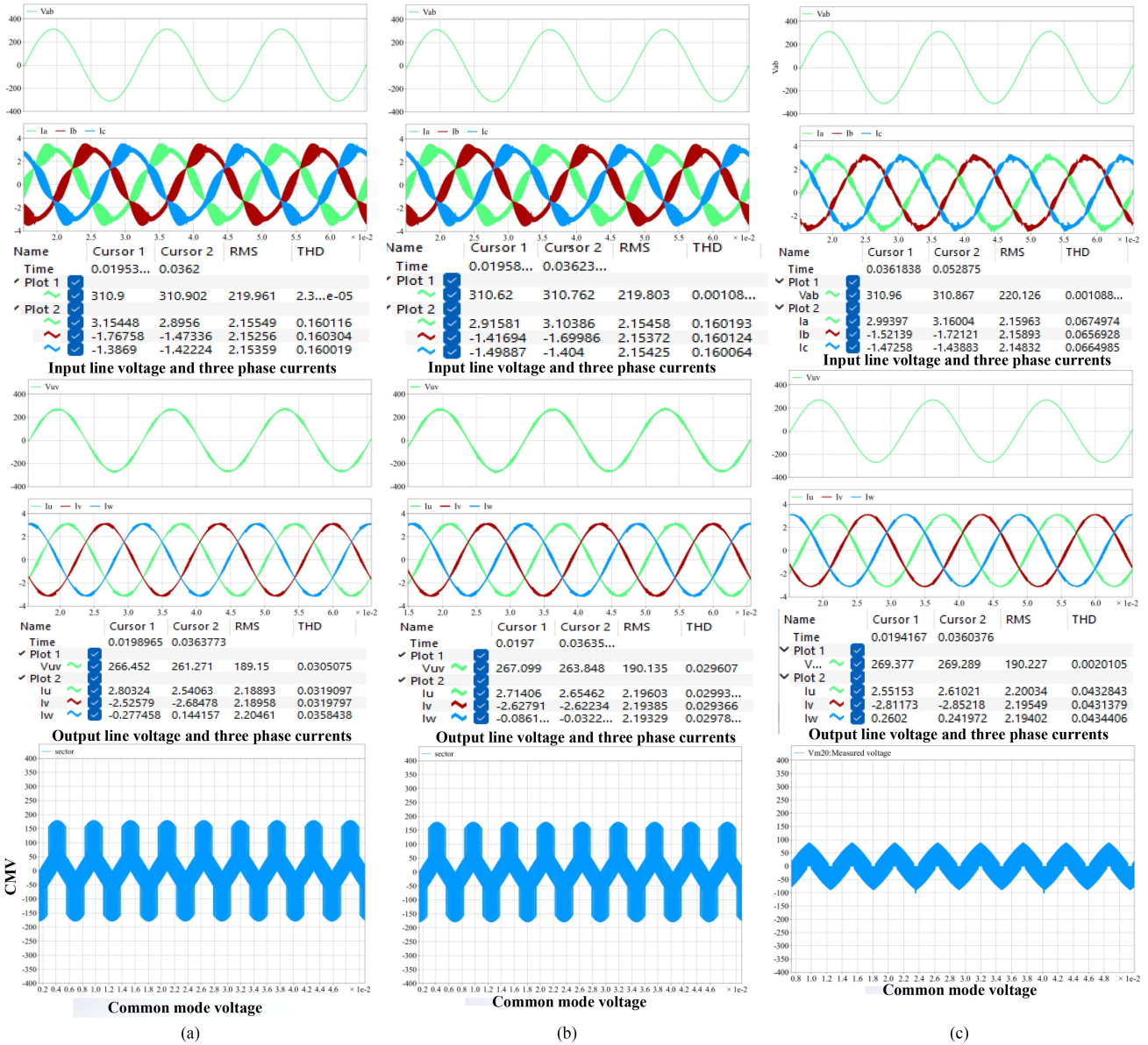


FIGURE 17. Simulation results at $q = 0.866$. (a) Conventional DPWM. (b) High-efficiency DPWM. (c) Proposed DPWM.

B. EXPERIMENTAL VERIFICATIONS

In this part, the practical implementation of the proposed method is proposed. Additionally, to verify the proposed method's efficiency improvement and CMV reduction capabilities, comparisons between the experimental results of the proposed, conventional, and high-efficiency DPWM methods are made. Since the proposed method cannot achieve low CMV at small q values (according to the simulation study), it is only experimented for $q = 0.866$.

1) PROPOSED METHOD IMPLEMENTATION

The prototype of the DMC is shown in Fig. 18(a). The DMC board has been developed using the IGBT switches of the IKW40N120T2 model. To measure the input voltage and current, output voltage and current, and CMV waveforms, the Teledyne LeCroy Wavesurfer 4024HD oscilloscope was used. Additionally, to measure the efficiency and THD of input current and output current, the HIOKI 3390 power analyzer was used. Modulation methods were implemented employing the Texas Instruments DSP of the TMS320F28379D model and the lattice complex programmable logic device (CPLD) of the LCMXO2-7000HE-4TG144C model. Fig. 18(b) shows the experimental diagram of the DMC, which consists of a three-phase ac power supply (Chroma 61703), input filter, primary circuit, output filter, three-phase resistive load, clamping circuit, and peripherals circuit composition. The input filter is composed of inductors, capacitors, and damping resistors. Due to the existing resources in the laboratory, the input filter is a circuit in which damping resistors and inductors are connected in parallel. The DMC is composed of 18 IGBT

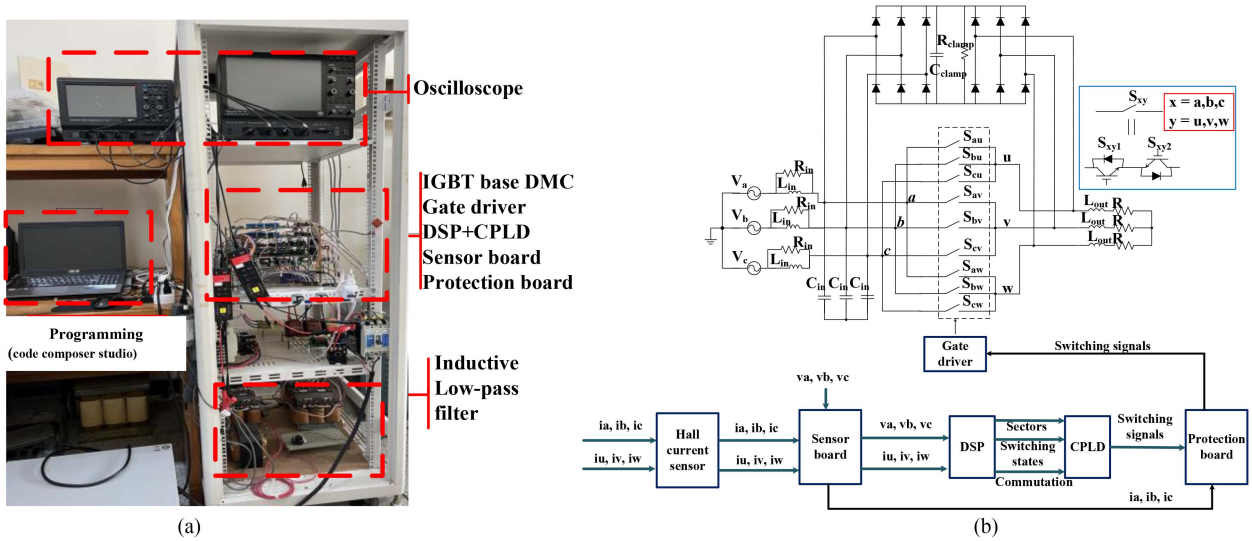


FIGURE 18. Laboratory setup. (a) Laboratory prototype of the DMC. (b) Experimental platform for DMC.

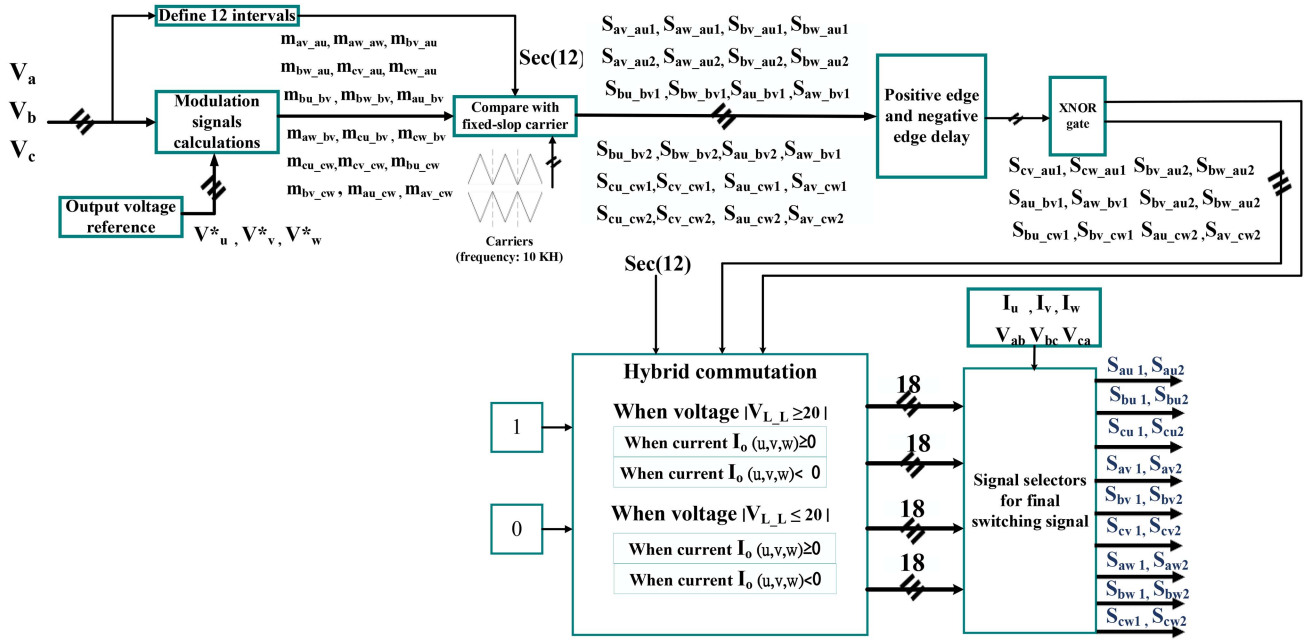
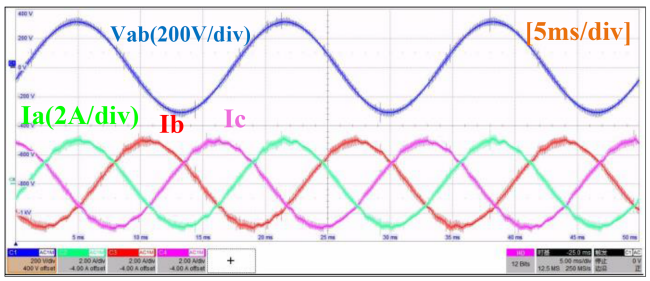


FIGURE 19. Control block diagram of the proposed DPWM.

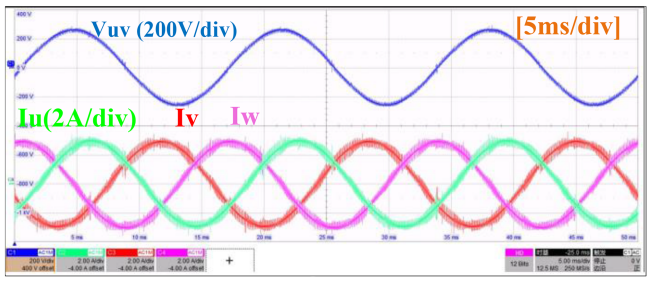
and *RC* snubber circuits. The output filter consists of inductors. The clamping circuit consists of two sets of three-phase diode bridge rectifiers, capacitors, and resistors. The peripheral circuit includes a hall current sensor, a sensor board, a Texas Instruments digital signal processor (DSP), a lattice semiconductor CPLD, a protection board, and a gate driver. First, the input and output voltage and current are transmitted to the sensing board to convert into an acceptable value for the DSP. Then, the values are transformed through a DSP built-in analog-to-digital converter. The DSP internal calculation scales the digital value proportionally and is restored to its actual size. Then, the partition is performed according to the selected modulation, and the switching state is calculated. The modulation signals and the commutation interval signal are sent to the CPLD through the general-purpose input/output pins. Besides, the switching states from enhanced pulsewidth modulation (EPWM) are sent to the CPLD. The CPLD triggers the switching states from the DSP using positive and negative edges. It combines various modulation signals and commutation methods to generate the final switching signal. Once generated, the switching signal is forwarded to the protection board. The protection board receives input current

TABLE 3 Simulation and Experimental Parameters

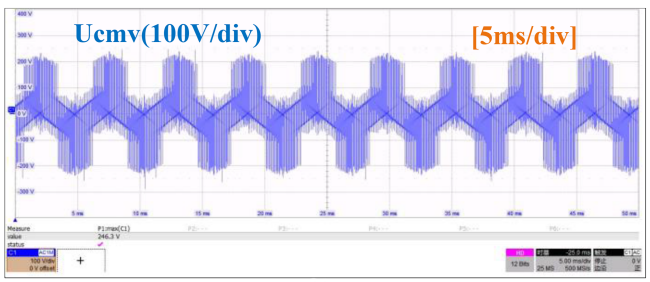
symbol	name	value	symbol	name	value
	Input voltage	220	load	Output load	50Ω
	Input frequency	60Hz		Carrier frequency	10KHz
	Output voltage	190		Commutation time (per step)	1μs
	Output frequency	60Hz		Input voltage threshold	20 V
	Input filter inductor	0.65mH		Clamp capacitor	5μF
	Input filter capacitor	20μF		Clamp resistor	11kΩ
	Passive damping resistor	20Ω		Snubber capacitor	1nF
	output filter inductor	10mH		Snubber resistor	22Ω



(a)



(b)



(c)

FIGURE 20. Experimental results of the conventional DPWM method. (a) Input line voltage and three-phase current. (b) Output line voltage and three-phase current. (c) CMV.

TABLE 4 Analysis of the Experimental Results for the Proposed, High-Efficiency, and Conventional DPWM

	Conventional DPWM	High-efficiency DPWM	Proposed DPWM
Efficiency	91.37%	92.50%	92.98%
THD of input current	2.89%	2.03%	2.89%
THD of output current	0.75%	0.83%	1.09%
CMV (Peak value)	246.3V	233.6V	120.9V
$V_O(rms)$	182.09v	182.49v	183.94 v

values from the sensing board and analyses them to determine the appropriate action. The protection board decides whether to transmit the switching signal to the gate driver based on the analysis. The gate driver converts the voltage level of the switching signal received from the protection board into the level that can drive the IGBT to turn on and off. Finally, it transmits the switching signal to the 18 switches. The control block diagram for the proposed DPWM and the hybrid three-step commutation is shown in Fig. 19. Using the control block diagram, it can be realized how to generate the final switching signals. The input voltage (v_a, v_b, v_c) and the reference output voltage (v_u^*, v_v^*, v_w^*) are divided into sectors to obtain final intervals. Then, modulation signals are calculated using (12) to generate the conversion matrix [M]. The modulation signals in each interval are compared with the carrier and 180° phase-shifted carrier, both of which have a 10 kHz frequency, to generate the switching states (EPWM). The switches are triggered by positive and negative edges to obtain the switching states that include deadtime. Then, the switching states are selected according to each interval signal, and all switching states are grouped for commutation. Commutation judgment is performed based on the input voltages (v_a, v_b, v_c) and the output currents (i_u, i_v, i_w). Finally, the switching state is switched according to the proposed commutation to generate the final switching signals.

2) EXPERIMENTAL RESULTS

Figs. 20, 21, and 22 illustrate the experimental waveforms of input and output line voltage, input and output three-phase current waveforms, and CMV of the conventional, high-efficiency, and proposed DPWM, respectively, when $q = 0.866$. The summary of experimental results is organized in Table 4. The results can be investigated in the following parts.

a) Input and output waveform analysis: It is verified that both the input and output terminals can produce sinusoidal voltage and current waveforms at 60 Hz.

It is worth noting that the introduction of the proposed DPWM method leads to an increase in the THD of the output

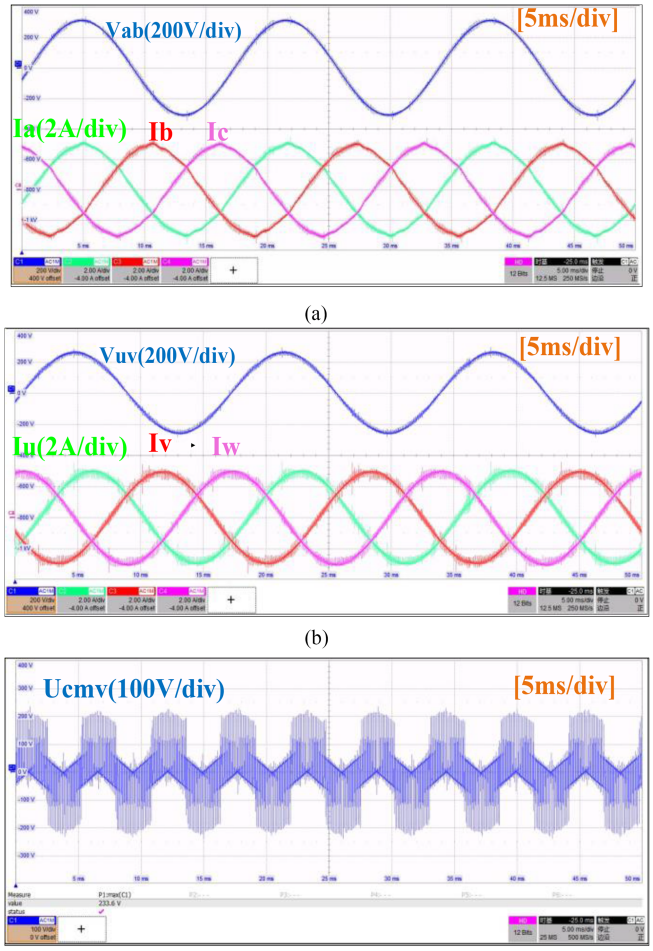


FIGURE 21. Experimental results of high-efficiency DPWM method. (a) Input line voltage and three-phase current. (b) output line voltage and three-phase current. (c) CMV.

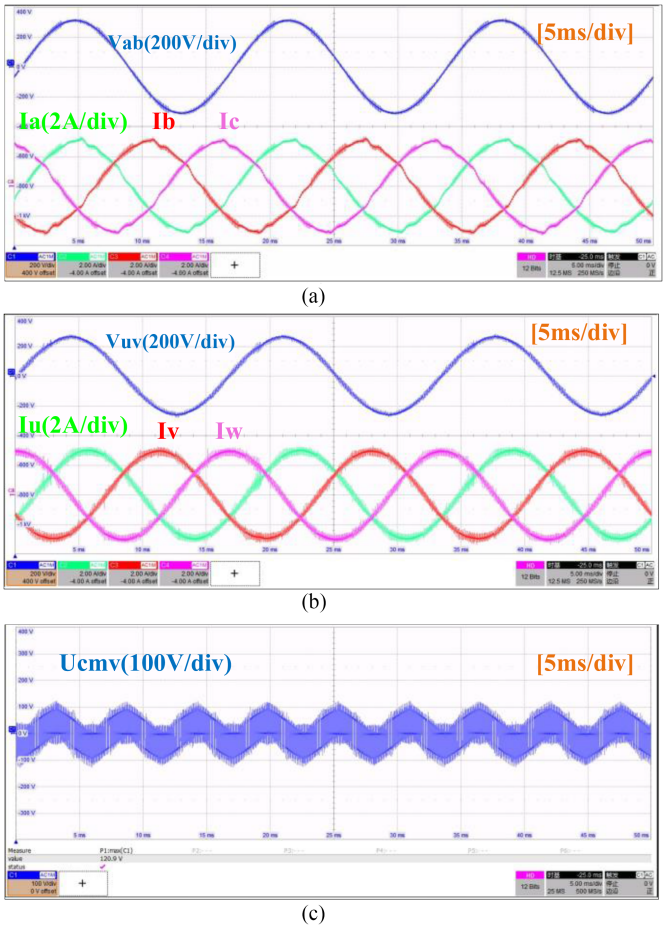


FIGURE 22. Experimental results of the proposed DPWM method. (a) Input line voltage and three-phase current. (b) Output line voltage and three-phase current. (c) CMV.

current compared with the conventional and high-efficiency DPWM methods. The proposed DPWM method employs rotating and active vectors to synthesize reference output voltage. However, the high-efficiency DPWM method also utilizes zero vectors in addition to the above types of vectors. Accordingly, although the proposed DPWM delivers the CMV mitigation advantage by avoiding zero vectors, it increases the differential-mode voltage, causing higher THD than the high-efficiency DPWM. Generally, there is a tradeoff between the CMV and differential-mode voltage, so the lower the CMV, the higher the differential-mode voltage [27]. However, it verified that the THD of both input and output current meets the IEEE standards, which proves that harmonic content specification has a low amount.

Although the proposed method maximizes the actual output voltage (V_O) compared with other methods, the actual output voltage is still lower than the expected output voltage ($190v_{\text{rms}}$). The main reason is the voltage drop across the input and output filters. Notably, the input power factor was not precisely unity because of the input filter capacitor.

b) CMV analysis: It can be seen from Figs. 20(c) and 21(c) that the peak value of CMV for conventional and high-efficiency DPWM methods is 246.3 V and 233.6 V, respectively. The peak value of CMV for the proposed DPWM method is 120.9 V, as shown in Fig. 22(c), which is decreased by half compared with the conventional and high-efficiency DPWM methods. Noteworthy that the CMV peaks of the conventional, high-frequency, and proposed DPWMs are higher than the expected peak value of the CMV. This is primarily due to surge voltages caused by switching actions. In fact, the nonideal characteristics of switches in a circuit cause to generating voltage spikes during the on-and-off periods. Several factors, including switch parameters and parasitic inductance, influence the amplitude of these voltage spikes. Furthermore, CMV spikes are generated due to the effect of switching deadtime. The experimental results indicate voltage spike amplitudes ranging from approximately 20 to 30 V. However, disregarding these voltage spikes, the observed peak CMV magnitude in the experimental results reasonably aligns with the theoretical predictions.

c) Efficiency analysis: The efficiency of the proposed DPWM is 92.98%, which is higher than that of the conventional DPWM (91.37%) and high-efficiency DPWM (92.50%). Therefore, the proposed DPWM not only effectively suppresses the peak magnitude of CMV but also increases efficiency by replacing the rotating vector with the zero vector.

V. CONCLUSION

In this article, a novel DPWM method, which is based on a carrier-based principle, is proposed. The objective of this proposed method is to reduce the CMV while preserving the advantages of the conventional DPWM, such as high efficiency, unity input power factor, and a large voltage transfer ratio. Using the proposed method, the CMV value is reduced by 50% compared with the conventional methods. Besides, the proposed DPWM method improves efficiency compared with the conventional DPWM due to its switching sequence. Although the proposed method slightly increases the output current THD, it is a small amount, and the THD is within acceptable IEEE limits. Notably, the proposed method employs a hybrid three-step commutation, which cancels output voltage error to maximize the actual output voltage and reduces switching losses by minimizing the number of hard switches and decreasing the input current's THD.

APPENDIX

This part presents the conversion matrix $[M]$ calculation method used in the DPWM. Proportional power distribution can be achieved by ensuring that the input currents are in phase with their respective input voltages, as shown in (14). It is important to note that the input reactive power must be zero to achieve maximum efficiency

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = N \begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} = \begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} \frac{p}{v_{an}^2 + v_{bn}^2 + v_{cn}^2}. \tag{14}$$

The matrix converter formulation can be summarized using two general relationships, (15) and (16). The connection matrix $[S]$ consists of the connection functions (expressed as 1 or 0) S_{ij}, which describe the ideal switch states (on or off) of the converter. The conversion matrix $[M]$ is defined based on the input and output voltage references and comprises nine switch modulation signals m_{ij}. The general matrix is determined using Kirchhoff's laws as follows:

$$\begin{bmatrix} v_{un} \\ v_{vn} \\ v_{wn} \end{bmatrix} = [S] \begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} \text{ and } \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = [S]^T \begin{bmatrix} i_u \\ i_v \\ i_w \end{bmatrix}$$
$$\text{with } [S] = \begin{bmatrix} S_{au} & S_{av} & S_{aw} \\ S_{bu} & S_{bv} & S_{bw} \\ S_{cu} & S_{cv} & S_{cw} \end{bmatrix}. \tag{15}$$

When the PWM operates with a modulation period T much lower than the input and output periods (i.e., PWM frequency is much higher than input and output frequency), the average values of the connection functions S_{ij} are equal to the modulation signals of the conversion matrix $[M]$. In other words, $<S_{ij}>T = m_{ij}$

$$\begin{bmatrix} v_{un} \\ v_{vn} \\ v_{wn} \end{bmatrix} = [M] \begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} \text{ and } \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = [M]^T \begin{bmatrix} i_u \\ i_v \\ i_w \end{bmatrix}$$
$$\text{with } [M] = \begin{bmatrix} m_{au} & m_{av} & m_{aw} \\ m_{bu} & m_{bv} & m_{bw} \\ m_{cu} & m_{cv} & m_{cw} \end{bmatrix}. \tag{16}$$

After obtaining the conversion matrix, the modulation signals of $[M]$ can be calculated in each interval using the following procedure.

When the interval is *bu* and the modulation signal m_{bu} is 1, the modulation signal of the DMC is shown as follows:

$$\begin{bmatrix} m_{au}=0 & m_{av}=\frac{(v_{ca}-v_{ab})v_{uv}*}{{v_{ab}}^2+{v_{bc}}^2+{v_{ca}}^2} & m_{aw}=\frac{(v_{ca}-v_{ab})v_{uw}*}{{v_{ab}}^2+{v_{bc}}^2+v_{ca}} \\ m_{bu}=1 & m_{bv}=1-m_{cv}-m_{av} & m_{bw}=1-m_{cw}-m_{aw} \\ m_{cu}=0 & m_{cv}=\frac{(v_{bc}-v_{ca})v_{uv}*}{{v_{ab}}^2+{v_{bc}}^2+v_{ca}} & m_{cw}=\frac{(v_{bc}-v_{ca})v_{uw}*}{{v_{ab}}^2+{v_{bc}}^2+v_{ca}} \end{bmatrix}. \tag{17}$$

When the interval is *cu* and the modulation signal m_{cu} is 1, the modulation signal of the DMC is shown as follows:

$$\begin{bmatrix} m_{au}=0 & m_{av}=\frac{(v_{ca}-v_{ab})v_{uv}*}{K} & m_{aw}=\frac{(v_{ca}-v_{ab})v_{uw}*}{K} \\ m_{bu}=0 & m_{bv}=\frac{(v_{ab}-v_{bc})v_{uv}*}{K} & m_{bw}=\frac{(v_{ab}-v_{bc})v_{uw}*}{K} \\ m_{cu}=1 & m_{cv}=1-m_{av}-m_{bv} & m_{cw}=1-m_{aw}-m_{bw} \end{bmatrix}. \tag{18}$$

When the interval is *av* and the modulation signal m_{av} is 1, the modulation signal of the DMC is shown as follows:

$$\begin{bmatrix} m_{au}=1-m_{bu}-m_{cu} & m_{av}=1 & m_{aw}=1-m_{bw}-m_{cw} \\ m_{bu}=\frac{(v_{ab}-v_{bc})v_{uv}*}{k} & m_{bv}=0 & m_{bw}=\frac{(v_{ab}-v_{bc})v_{uw}*}{k} \\ m_{cu}=\frac{(v_{bc}-v_{ca})v_{uv}*}{K} & m_{cv}=0 & m_{cw}=\frac{(v_{bc}-v_{ca})v_{uw}*}{K} \end{bmatrix}. \tag{19}$$

When the interval is *bv* and the modulation signal m_{bv} is 1, the modulation signal of the DMC is shown as follows:

$$\begin{bmatrix} m_{au}=\frac{(v_{ca}-v_{ab})v_{uv}*}{k} & m_{av}=0 & m_{aw}=\frac{(v_{ca}-v_{ab})v_{uw}*}{k} \\ m_{bu}=1-m_{bu}-m_{cu} & m_{bv}=1 & m_{bw}=1-m_{bw}-m_{cw} \\ m_{cu}=\frac{(v_{bc}-v_{ca})v_{uv}*}{K} & m_{cv}=0 & m_{cw}=\frac{(v_{bc}-v_{ca})v_{uw}*}{K} \end{bmatrix}. \tag{20}$$

When the interval is *cv* and the modulation signal m_{cv} is 1, the modulation signal of the DMC is shown as follows:

$$\begin{bmatrix} m_{au}=\frac{(v_{ca}-v_{ab})v_{uv}*}{k} & m_{av}=0 & m_{aw}=\frac{(v_{ca}-v_{ab})v_{uw}*}{k} \\ m_{bu}=\frac{(v_{ab}-v_{bc})v_{uv}*}{K} & m_{bv}=0 & m_{bw}=\frac{(v_{ab}-v_{bc})v_{uw}*}{K} \\ m_{cu}=1-m_{au}-m_{bu} & m_{cv}=1 & m_{cw}=1-m_{aw}-m_{bw} \end{bmatrix}. \tag{21}$$

When the interval is *aw* and the modulation signal m_{aw} is 1, the modulation signal of the DMC is shown as follows:

$$\begin{bmatrix} m_{au}=1-m_{bu}-m_{cu} & m_{av}=1-m_{bv}-m_{cv} & m_{aw}=1 \\ m_{bu}=\frac{(v_{ab}-v_{bc})v_{uv}*}{k} & m_{bv}=\frac{(v_{ab}-v_{bc})v_{uw}*}{k} & m_{bw}=0 \\ m_{cu}=\frac{(v_{bc}-v_{ca})v_{uv}*}{K} & m_{cv}=\frac{(v_{bc}-v_{ca})v_{uw}*}{K} & m_{cw}=0 \end{bmatrix}. \tag{22}$$

When the interval is *bw* and the modulation signal m_{bw} is 1, the modulation signal of the DMC is shown as follows:

$$\begin{bmatrix} m_{au}=\frac{(v_{ca}-v_{ab})v_{uv}*}{k} & m_{av}=\frac{(v_{ca}-v_{ab})v_{uw}*}{k} & m_{aw}=0 \\ m_{bu}=1-m_{au}-m_{cu} & m_{bv}=1-m_{av}-m_{cv} & m_{bw}=1 \\ m_{cu}=\frac{(v_{bc}-v_{ca})v_{uv}*}{K} & m_{cv}=\frac{(v_{bc}-v_{ca})v_{uw}*}{K} & m_{cw}=0 \end{bmatrix}. \tag{23}$$

When the interval is *cw* and the modulation signal m_{cw} is 1, the modulation signal of the DMC is shown as follows:

$$\begin{bmatrix} m_{au}=\frac{(v_{ca}-v_{ab})v_{uv}*}{k} & m_{av}=\frac{(v_{ca}-v_{ab})v_{uw}*}{k} & m_{aw}=0 \\ m_{bu}=\frac{(v_{ab}-v_{bc})v_{uv}*}{K} & m_{bv}=\frac{(v_{ab}-v_{bc})v_{uw}*}{K} & m_{bw}=0 \\ m_{cu}=1-m_{au}-m_{bu} & m_{cv}=1-m_{av}-m_{bv} & m_{cw}=1 \end{bmatrix}. \tag{24}$$

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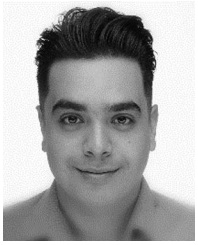

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