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Submodule Capacitor Voltage Balancing Through High-Frequency-Side Control for Multiport MMC-Based Solid-State Transformers

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ABSTRACT This article proposes a novel submodule capacitor voltage balancing control for multiport modular multilevel converter (MMC)-based solid-state transformers. To balance each submodule capacitor voltage, the balancing control is usually applied to the MMC. However, the low switching frequency operation and bulky arm inductance of the MMC limit the controller bandwidth and stability margin. These issues are addressed by moving the balancing control to the back-end dc/dc converter, which is operated at high switching frequency. The controller gains are designed based on the small-signal model. The superiority of the proposed controller over the conventional one has been verified through Bode plot, pole-zero map, and Nyquist path analyses. Experimental results for a 2.4-kW prototype system have also verified the accuracy of the model and effectiveness of the proposed balancing control for step load changes.

INDEX TERMS Balancing control, modeling, modular multilevel converters (MMCs), solid-state transformer (SST).

I. INTRODUCTION

Multiport converters have been extensively studied due to their benefits of flexibility and high efficiency, especially in systems involving multiple energy sources, storage, and loads [1]. When connecting multiple systems, isolation through transformers is usually required for safety, grounding, and noise reduction. The conventional low-frequency transformers are bulky, so they are being replaced by solid-state transformers (SSTs). The SSTs can provide isolation in medium/high-frequency ranges, which can reduce the transformer size and increase the system power density. A multiport converter including medium/high-frequency isolation is often called a multiport SST, whose basic structure and application are shown in Fig. 1. This structure integrates medium-voltage ac (MVAC), medium-voltage dc (MVDC), and several low-voltage dc (LVDC) ports. The MVDC port can be connected to loads, transmissions, or renewable energy (RE) sources. On the LVDC sides, they can be considered as microgrids, energy storage systems (ESSs), RE sources, or EV chargers.

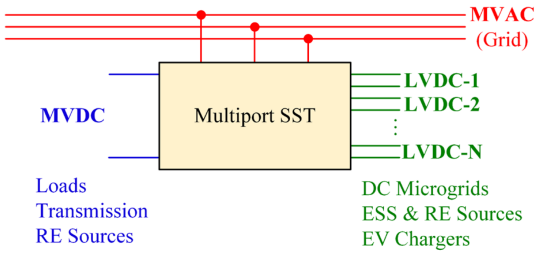

FIGURE 1. Basic structure and application of a multiport SST.

The number of LVDC ports can be adjusted depending on the system complexity and requirements.

For high-power applications, a multiport SST with a modular structure is preferable due to the ease of adjusting the power level, maintenance, and fault-tolerant capability. Several topologies of modular SST are shown in Fig. 2. Fig. 2(a) shows an SST with a multilevel converter as the ac/dc converter and dc/dc converters connected to the dc-bus with input

TABLE 1. Comparisons of Several SST Structures

References	Modularity of ac/dc stage	Modularity of dc/dc stage	Common dc-link	Ability to provide MVDC and LVDC	MFT power compared with the system power
[2]	No	Yes	Yes	Yes	Medium
[3], [4], [5]	Yes	Yes	No	No	Medium
[6], [7], [8], [9]	Yes	Yes	Yes	Yes	Smallest
[10]	Yes	No dc/dc stage	No	No	Largest
[11]	Yes	No dc/dc stage	Yes	Yes	Largest

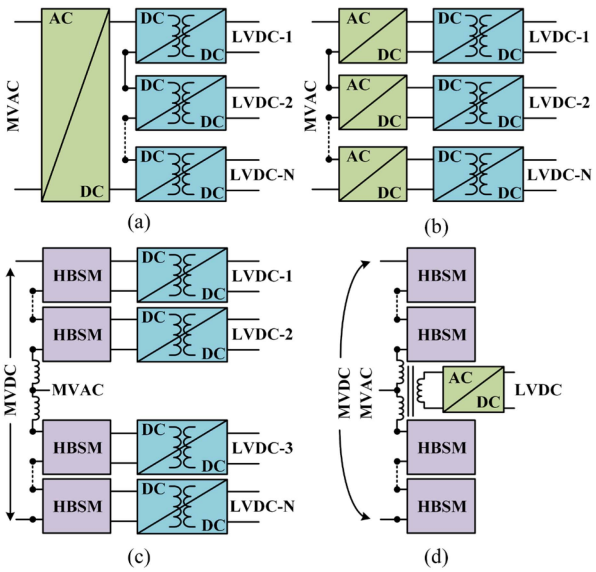

FIGURE 2. Several structures of SST based on (a) multilevel converter, (b) CHB, (c) MMC, and (d) MMC with magnetic integration.

series configuration [2]. This structure has MVAC, MVDC, and LVDC ports. In this structure, only the dc/dc converters are modular. If a full modularity in which both the ac/dc and dc/dc converters are modular is required, a cascaded H-bridge structure in Fig. 2(b) can be used [3], [4], [5]. However, this structure does not have a common dc-link for the system, resulting in the loss of the MVDC port. The structure in Fig. 2(c) has the full modularity aspect and a common dc-link for the system [6], [7], [8], [9]. This structure consists of a modular multilevel converter (MMC) as the ac/dc conversion between the MVAC and MVDC as well as dc/dc converters connected to each MMC submodule capacitor to construct the LVDC port. Any MMC submodule topologies can be applied to this structure. To simplify the illustration, only the half-bridge submodule (HBSM) is drawn. Note that in this topology, the SST plays a role of converting power from the MVAC to the LVDC. Compared with the previous two structures, bulky arm inductors are required here. To overcome this issue, they can be integrated to a medium frequency transformer (MFT), as shown by the structure in Fig. 2(d) [10], [11]. Unlike the other referred topologies, there is only one MFT in the system, which may deteriorate reliability and require the same power rating as that of the overall system. The advantages and disadvantages of the aforementioned topologies are summarized in Table 1.

In multiport systems, the output voltage of each port should be controlled by individual controller. Furthermore, for modular converter structures, a voltage balancing algorithm needs to be applied, especially to balance the submodule capacitor voltages. An easy solution to address this is to add average and/or individual voltage control in the ac/dc stage [12], [13]. Each capacitor voltage is measured and regulated by a proportional (P) or proportional–integral (PI) controller. However, the number of controllers increases as the number of submodules increases. A balancing method based on sorting algorithm can be applied to the modulation stage to overcome this issue [14], [15]. This algorithm requires current sensors to identify the direction of current flowing to the circuit. A sensorless balancing algorithm was proposed in [16]. However, it becomes more complex and its performance depends on the parameter accuracy. Furthermore, the ac/dc converter is usually operated at lower switching frequency, which further limits the bandwidth of the controllers [17], [18]. Consequently, the system tends to be slower and less stable. Table 2 provides a qualitative comparison of several submodule capacitor voltage balancing schemes for MMC systems.

The analysis of system controllers requires an appropriate modeling technique. So, the small-signal model is usually derived at first. In the case of the large number of submodules, the modeling of SST is challenging, especially in the ac/dc stage. The number of state variables is proportional to the number of capacitors and inductors in the system. Thus, it is preferred to replace all MMC submodules in the upper arm with a dependent voltage source, as well as those in the lower arm [19], [20], [21], [22], [23]. However, this technique cannot be applied to MMC-based SST systems since the dc/dc converters are connected to each of the submodule capacitors. The submodule capacitors should be modeled and investigated individually, which has never been considered in other literature as per this literature review. Furthermore, both dc and ac state variables exist in the dc/dc converter, so that a simple average model cannot be applied [24], [25], [26].

According to the aforementioned discussions, modeling and control require greater attention to constructing a robust SST system. This article extends the application of the MMC-based SST topology in Fig. 2(c). The main contributions are summarized as follows.

1) A simple and accurate modeling of the MMC-based SSTs is derived. The submodule capacitor voltage dynamics are considered individually, which has never been done in other literature. On the dc/dc stage, the

TABLE 2. Qualitative Comparison of Several Submodule Capacitor Voltage Balancing Schemes

References	Balancing scheme	Applied to	Current sensor	Dynamic response	Brief description
[12]	Voltage sorting	MMC-side	Yes	Slow	
[13]	PI control	MMC-side	Yes	Slow	The submodule is charged based on the direction of arm current
[14]	Improved voltage sorting	MMC-side	Yes	Slow	
[15]	Minimum DMV or CMV	MMC-side	Yes	Not mentioned	
[16]	Voltage and current sensorless sorting	MMC-side	No	Not mentioned	Estimation algorithm is required
[17]	Nearest level control	MMC-side	No	Not mentioned	The submodule is charged based on the phase-shift angle
Proposed	High-frequency-side control	DC/DC converter-side	No	Fast	The balancing control is applied to the dc/dc converter

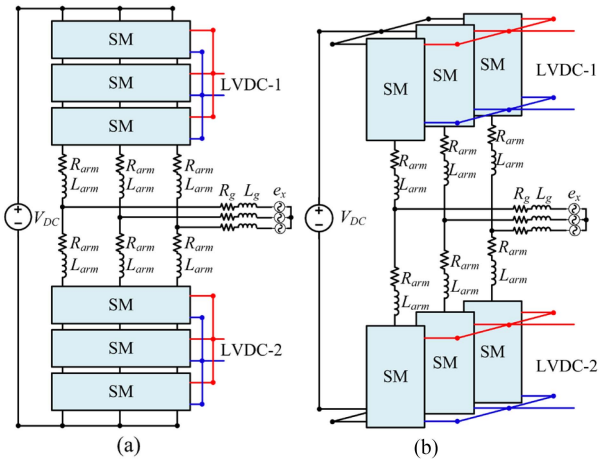

FIGURE 3. Four-port MMC-based SST with different submodule connections. (a) Horizontal connection. (b) Vertical connection.

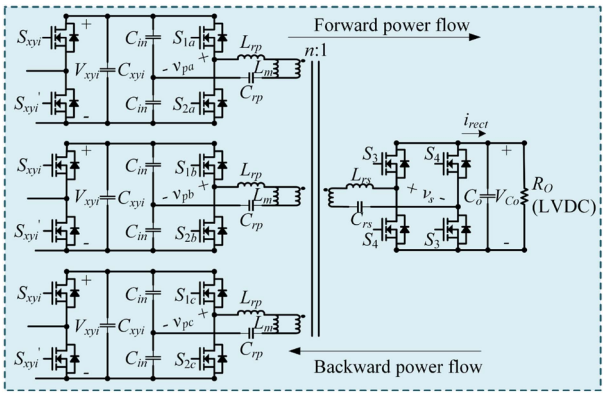

FIGURE 4. Submodule of the MMC-based SST using HBSM and Q-CLLC converter.

number of state variables can be reduced significantly without deteriorating the accuracy.

2) A fast and robust submodule capacitor voltage balancing algorithm is developed and realized from the dc/dc stage. Once the small-signal model is obtained, the controller performance can be analyzed thoroughly from its Bode plot, pole-zero location, and Nyquist path. Moreover, the conventional and proposed control schemes are designed to have a particular value of phase margin, while the bandwidth can be a parameter to compare. This comparison shows that applying the balancing algorithm to the dc/dc stage offers faster and more stable operations for the SST when stepwise load changes exist.

II. FOUR-PORT MMC-BASED SST

The well-known four-port MMC-based SST shown in Fig. 3 is analyzed further. The MMC converts MVAC to MVDC, where it can be connected to loads or dc transmission system. Isolated dc/dc converters are connected to each MMC HBSM to construct one or more LVDC ports. Furthermore, two separated LVDC ports are considered, where they can carry different amounts of power. Thus, a proper balancing technique is required when transferring unbalanced power. The LVDC port can be connected to loads, ESSs, or another dc transmission system. For the entire discussion, the combination of MMC HBSM and dc/dc converters is called submodule.

There are two alternatives to connect the submodules [27]. The submodules can be connected in a horizontal way, where they are connected to each phase of the MMC arm, as shown in Fig. 3(a). On the other hand, vertical connection is also possible, where they are connected to the same arm of the MMC, as shown in Fig. 3(b).

A. MODULAR MULTILEVEL CONVERTER

The power conversion from MVAC to MVDC (and vice versa) through MMC is not the SST part since it does not go through isolation stage. It consists of several submodules, which can reduce the switch voltage stresses, offer scalability, modularity, and fault-tolerant capability. The HBSM is considered and shown in Fig. 4. S_{xyi} and S_{xyi}' represent the half-bridge switches that operate in a complementary way, where $x = \{a, b, c\}$, $y = \{u, l\}$, and $i = \{1, 2, 3, \ldots, N\}$ denote the corresponding phase, arm, and submodule number. Phase-shift pulsewidth modulation (PSPWM) is applied to modulate the switches [28]. The basic operation of the MMC can be found in [29].

The submodule capacitors and their voltages are represented as C_{xyi} and V_{xyi}, respectively. The dc-link is assumed to be connected to RE sources with a constant voltage (V_{dc}). Arm inductor (L_{arm}) is connected to each MMC arm to reduce the

TABLE 3. Qualitative Comparison of DC/DC Converters

Parameters for comparison	Nonresonant converters	Resonant converters		
	Dual- and multiple -active bridge	LC	LLC	CLLC
Most used modulation technique	Phase-shift modulation	Frequency modulation	Frequency modulation	Frequency modulation
Complexity of modulation technique at low load	Complex	Simple	Simple	Simple
Soft switching in all ranges of output power	Yes (only at unity voltage gain)	No	Yes	Yes
Variation of switching frequency	Small	Large	Medium	Small
Symmetric bidirectional operation	Yes	Yes	No	Yes

circulating current and R_{arm} is its equivalent series resistance (ESR). On the other hand, the LVDC ports are assumed to be connected to two separate dc microgrids shown in Fig. 3, where power imbalance may occur between the upper and lower arms.

B. DC/DC CONVERTER

In SST systems, the isolation is performed in medium/high-frequency regions through isolated bidirectional dc/dc converters. Operation of high-power dc/dc converters has been extensively studied up to 500 kHz of switching frequency [30], [31], [32]. However, operation at high switching frequency limits the maximum power transfer capability, and may not increase the power density of the SST. This is due to the challenging isolation technique and partial discharge at high voltage and high power. Overall, the dc/dc converters can be categorized as nonresonant and resonant types. Their performances are summarized in Table 3.

Considering the performances in Table 3, the CLLC resonant converter offers significant advantages over the other topologies. It has a symmetric bidirectional power flow characteristic and less variation of switching frequency, which make the analysis of bidirectional power flow simple and the converter efficiency higher at low load, respectively. The asymmetric structure with three-input and single-output is adopted since it is the most beneficial in terms of cost and efficiency [33], [34]. Considering these features, the dc/dc converter topology adopted in this work is a quadruple CLLC (Q-CLLC) converter, as shown in Fig. 4.

In the Q-CLLC converter, the three input ports are connected to the submodule capacitors of the MMC, whereas the LVDC terminal is the output port. The LVDC load is denoted as R_O. A half-bridge structure is adopted to the input side with C_{in} as input capacitor, whereas the output side has a full-bridge structure with C_o as output capacitor. S_{1x} and S_{2x} represent the complementary switches on the primary side, whereas S_3 and S_4 correspond to the secondary side. A four-winding transformer provides the isolation between the MMC side and LVDC port, where n and L_m denote the transformer turn ratio and its magnetizing inductance, respectively. A CLLC resonant tank is adopted, where L_{rp}, L_{rs}, C_{rp}, and C_{rs} represent the resonant inductances and capacitances of the primary and secondary windings, respectively. Note that due to the three-input feature, the vertical connection in Fig. 3(b) can only be implemented where the number of submodules per arm is a multiple of three.

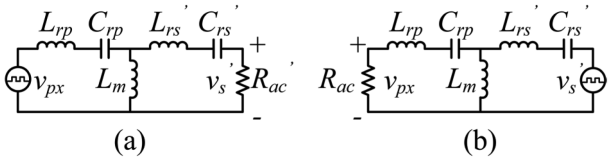

FIGURE 5. FHA model for CLLC converter. (a) Forward power flow. (b) Backward power flow.

The first harmonic approximation (FHA) model in Fig. 5 can be used to evaluate the performance of the Q-CLLC converter. The model for forward power flow, when transferring power to the LVDC port, is shown in Fig. 5(a), whereas that for backward power flow in Fig. 5(b), where a balanced resonant tank for each input port is assumed. Thus, each port carries the same amount of power and no circulating current flows between each port. The input–output relations can be expressed as follows:

$$G_{mf}(s) = \frac{v_s'}{v_{px}} = \frac{Z_m R_{ac}'}{Z_{rp}(R_{ac}' + Z_{rs}') + Z_m(R_{ac}' + Z_{rp} + Z_{rs}')} \tag{1}$$

$$G_{mb}(s) = \frac{v_{px}}{v_s'} = \frac{Z_m R_{ac}}{Z_{rs}'(R_{ac} + Z_{rp}) + Z_m(R_{ac} + Z_{rp} + Z_{rs}')} \tag{2}$$

where G_{mf} and G_{mb} are the gains for forward and backward power flows, $v_s' = nv_s$ is the secondary-side voltage referred to the primary side, v_{px} is the primary-side voltage, $Z_m = sL_m$, $Z_{rp} = sL_{rp} + 1/sC_{rp}$, $Z_{rs}' = n^2(sL_{rs} + 1/sC_{rs})$, and $R_{ac}' = 8n^2R_L/\pi^2$ is the ac equivalent resistance that is derived from [35].

The gain equations of (1) and (2) derived for the CLLC converter can be applied to LC and LLC converters. For LC converter, Z_m can be regarded as infinite and Z_{rs}' is zero. For the LLC converter, it is considered that Z_m is finite and Z_{rs}' is zero. The CLLC converter has a higher magnitude of denominators in (1) and (2), which makes the switching frequency lower than LC and LLC converters to transfer the same amount of power. Moreover, when $Z_{rp} = Z_{rs}'$, the forward and backward gains for the CLLC are identical, leading to a symmetric bidirectional power flow. The input–output gains

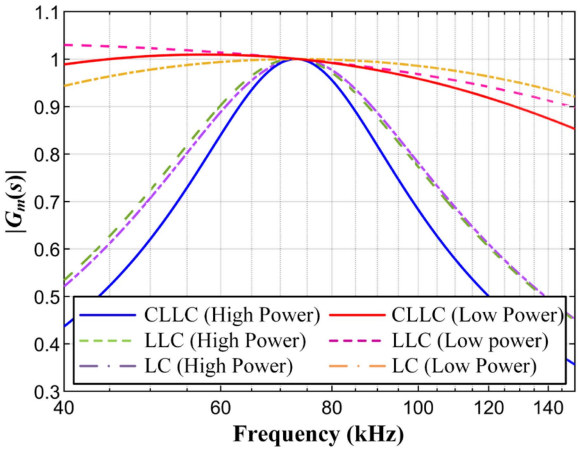

FIGURE 6. Input–output gains of LC, LLC, and CLLC converters as a function of switching frequency (f_{res} = 75 kHz).

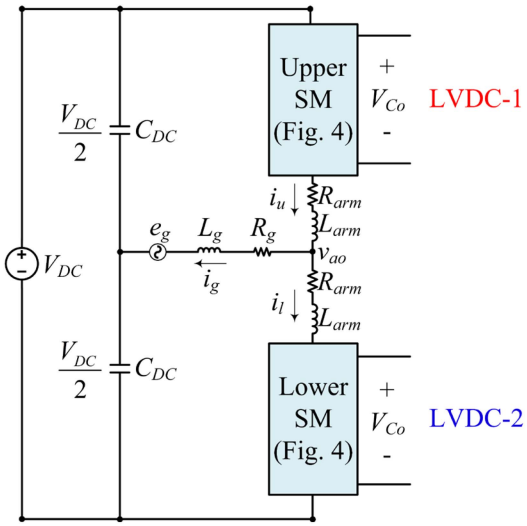

FIGURE 7. Single-phase MMC-based SST considered in the model derivation processes.

for these converters are illustrated in Fig. 6 when operating at high and low power conditions. A unity gain is obtained for all converters at the resonance frequency, which is expressed as follows:

$$f_{res} = \frac{1}{2\pi\sqrt{L_{rp}C_{rp}}}. \tag{3}$$

III. SMALL-SIGNAL MODELING

A small-signal model is used for a linearized representation of a system operating around a specific operating point. It is often applied to design the closed-loop controller of the converter. In this section, a small-signal model for a single-phase converter system with three submodules per arm, as shown in Fig. 7, is derived. Without loss of generality, this modeling procedure can be applied to a three-phase system with higher number of submodules.

A. MODELING OF MMC

In most of the literature, the submodules on the upper/lower arms are modeled as dependent voltage sources [19], [20], [21], [22], [23]. However, it is not valid for the MMC-based SST systems since dc/dc converters are connected to the HBSM as mentioned in Section I. Therefore, it is necessary to model the submodule capacitors independently. The submodule voltages and currents are denoted as v_{yi} and i_{Cyi}, respectively, which can be expressed as follows:

$$v_{yi}(t) = m_{yi}(t)V_{Cyi} \tag{4}$$

$$i_{Cyi}(t) = m_{yi}(t)i_y \tag{5}$$

where $m_{yi}(t) = M_{yi}\sin(\omega_g t)$ is the modulation signal of each MMC submodule, with M_{yi} and ω_g as the amplitude and grid angular frequency, respectively.

If the submodule capacitor voltages and upper/lower arm currents are chosen as the state variables of the MMC, the state equations can be expressed as follows:

$$\frac{d}{dt}v_{Cyi} = \frac{m_{yi}(t)}{C_{yi}}i_y - \frac{i_{CLLC,yi}}{C_{yi}} \tag{6}$$

$$\frac{d}{dt}i_u(t) = \frac{V_{DC}}{2L_{arm}} - R_{arm}i_u - \frac{\sum m_{ui}(t)V_{Cui}}{L_{arm}} - m_{ui}(t)\frac{V_{DC}}{2} \tag{7}$$

$$\frac{d}{dt}i_l(t) = \frac{V_{DC}}{2L_{arm}} - R_{arm}i_l - \frac{\sum m_{li}(t)V_{Cli}}{L_{arm}} + m_{li}(t)\frac{V_{DC}}{2} \tag{8}$$

where C_{yi} and v_{Cyi} are the submodule capacitance and its voltage, respectively, $i_{CLLC,yi}$ is the input current of Q-CLLC converter, and i_y is the upper/lower arm current.

During one cycle of switching period, the modulation signal can be regarded constant. By applying the averaging technique to (6)–(8)

$$\frac{d}{dt}v_{Cyi} = \frac{M_i}{C_{yi}}i_y - \frac{i_{CLLC,yi}}{C_{yi}} \tag{9}$$

$$\frac{d}{dt}i_y = \frac{V_{DC}}{2L_{arm}} - R_{arm}i_y - \frac{\sum M_i v_{Cyi}}{L_{arm}} \mp \frac{M_i V_{DC}}{2L_{arm}}. \tag{10}$$

From (9), it is intuitively known that the submodule capacitor current can be controlled by input current of QLLC converter, $i_{CLLC,yi}$.

The state equations in (9) and (10) should be linearized near the rated operating point. Assuming the balanced submodule capacitor voltages, the small-signal model in the Laplace domain can be derived as follows:

$$\tilde{v}_{Cyi} = \frac{\bar{I}_y\tilde{m}_i + \bar{M}_i\tilde{i}_y - \tilde{i}_{CLLC,yi}}{sC_{yi}} \tag{11}$$

$$\tilde{i}_y(s) = G_1(s)\left\{-K_1\tilde{m}_i - \bar{M}_i\tilde{v}_{Cy1} - \bar{M}_i\tilde{v}_{Cy2} - \bar{M}_i\tilde{v}_{Cy3}\right\} \tag{12}$$

$$K_1 = N\bar{V}_{cy} \mp \frac{V_{DC}}{2} \tag{13}$$

$$G_1(s) = \frac{1}{sL_{arm} + R_{arm}} \tag{14}$$

where symbols of "–" and "∼" above the variables represent the dc value and ac perturbation, respectively. The dc value of each variable can be obtained by using simulation or experimental results.

B. MODELING OF Q-CLLC CONVERTER

The Q-CLLC converter shown in Fig. 4 has a total of 15 state variables. This will lead to a large dimension of matrix, resulting in complex modeling procedure. For easy analysis, the modeling can be simplified without reducing the accuracy. Here, a model for the forward power flow is derived, but the same approach can be applied to the backward power flow.

The Q-CLLC converter cannot be operated at unity voltage gain where the switching frequency is equal to the resonance, which will be explained in detail later. Considering this issue, the converter is always operated above the resonant frequency. Thus, only this region of operation is considered for modeling. Furthermore, in forward power flow, the primary-side switches are controlled by the same gating signals, whereas on the secondary side, the body diodes conduct the current. To proceed with the analysis, several assumptions are made as follows.

1) The resonant tanks in each input port are balanced.
2) The MMC submodule capacitor voltages are balanced.
3) The three-input sides of the Q-CLLC converter are balanced.
4) The ESRs are neglected.

Under the aforementioned assumptions, the analysis of the Q-CLLC converter can be performed for any one input port, by which the total number of state equations is reduced. Several equations can be derived from Fig. 4 as follows:

$$L_{rp1} = L_{rp2} = L_{rp3} \tag{15}$$

$$C_{rp1} = C_{rp2} = C_{rp3} \tag{16}$$

$$v_{p,y1} = v_{p,y2} = v_{p,y3} = v_p = s_1 V_{Cu1}/2 \tag{17}$$

$$v_{su}{}' = v_{sl}{}' = v_s{}' = s_2 V_{Co}{}' = n s_2 V_{Co} \tag{18}$$

$$i_{Lrs}{}' = 3 i_{Lrp} - i_m \tag{19}$$

where V_{Co} is the LVDC port voltage, s_1 and s_2 are the switching functions of the primary and secondary sides, respectively, and i_{Lrp} and i_{Lrs} are the current flowing to the resonant inductors in primary and secondary sides, respectively, i_m is the magnetizing current, and superscript ' indicates that the variable is referred to the primary side. The switching functions can be expressed as follows:

$$s_1 = \text{sgn}[\sin(\omega_{sw} t)],\ s_2 = \text{sgn}[\sin(\omega_{sw} t + d)] \tag{20}$$

where ω_{sw} is the angular switching frequency, and d is the phase-shift angle between the primary and secondary sides.

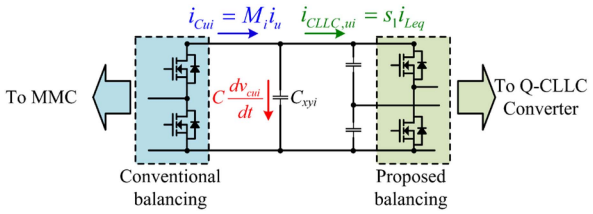

FIGURE 8. Conventional and proposed submodule voltage capacitor balancing methods.

Based on Fig. 4, the state equations can be written as follows:

$$\frac{d}{dt} v_{Cu1} = \frac{M_i}{C_{u1}} i_u - \frac{s_1 i_{Lrp}}{C_{u1}} \tag{21}$$

$$\frac{d}{dt} v_{Crp} = \frac{i_{Lrp}}{C_{rp}} \tag{22}$$

$$\frac{d}{dt} v_{Crs}{}' = \frac{i_{Lrs}{}'}{C_{rs}{}'} \tag{23}$$

$$\frac{d}{dt} i_{Lrp} = \frac{s_1 V_{cu1}}{2L_{rp}} - \frac{v_{Crp}}{L_{rp}} - \frac{L_m}{L_{rp}} \frac{di_m}{dt} \tag{24}$$

$$\frac{d}{dt} i_{Lrs}{}' = \frac{L_m}{L_{rs}{}'} \frac{di_m}{dt} - \frac{v_{Crs}{}'}{L_{rs}{}'} - \frac{s_2 V_{Co}{}'}{L_{rs}{}'} \tag{25}$$

$$\frac{d}{dt} v_{Co}{}' = \frac{s_2 i_{Lrs}{}'}{C_o{}'} - \frac{V_{Co}{}'}{R_o{}' C_o{}'} \tag{26}$$

where v_{Crp} and v_{Crs} are the voltages across C_{rp} and C_{rs}, respectively.

Equation (21) is the same equation as (9) viewed from the MMC side. It is seen that M_i can be controlled to balance the submodule capacitor voltage, which has been performed extensively in the conventional MMC control. On the other hand, s_1 also influences the submodule capacitor balancing, which is the fundamental idea of the proposed balancing scheme. The comparison of both methods is illustrated briefly in Fig. 8. However, the Q-CLLC converter cannot be operated as a dc transformer with a constant switching frequency at the resonance condition [36].

The model in (21)–(26) cannot produce accurate results since the inductor currents and capacitor voltages are ac variables. Therefore, a generalized average model (GAM) considering the fundamental component is preferred to model this converter, which has the similar concept with the extended describing function model [37], [38]. Using this model, all variables are represented as Fourier series in the complex form

$$\begin{aligned} x(t) &= \langle x \rangle_0(t) + \langle x \rangle_1(t) e^{j\omega_{sw} t} + \langle x \rangle_{-1}(t) e^{-j\omega_{sw} t} \\ &= \langle x \rangle_0 + 2\langle x \rangle_{1R} \cos(\omega_{sw} t) - 2\langle x \rangle_{1I} \sin(\omega_{sw} t) \end{aligned} \tag{27}$$

where $x(t)$ is the variable to be transformed, $\langle x \rangle_0$, $\langle x \rangle_{1R}$, and $\langle x \rangle_{1I}$ are dc, real, and imaginary components of the variable, respectively. The switching functions are taken as an example to derive the real and imaginary parts for GAM analysis. First,

the switching functions s_1 and s_2 can be expressed as follows:

$$s_1 = \begin{cases} 1, & 0 \le t < \frac{T_{sw}}{2} \\ -1, & \frac{T_{sw}}{2} \le t < T_{sw} \end{cases} \tag{28}$$

$$s_2 = \begin{cases} 1, & \frac{dT_{sw}}{2\pi} \le t < \frac{T_{sw}}{2} + \frac{dT_{sw}}{2\pi} \\ -1, & 0 \le t < \frac{dT_{sw}}{2\pi} \text{or} \frac{T_{sw}}{2} + \frac{dT_{sw}}{2\pi} \le t < T_{sw} \end{cases} \tag{29}$$

where t is the instantaneous time.

Both s_1 and s_2 are square waves with zero average values, which yields their zero-order components to zero, $\langle s_1\rangle_0$, $\langle s_2\rangle_0 = 0$. Their Fourier series representations can be expressed, respectively, as follows:

$$\langle s_1\rangle_{1R} = 0, \langle s_1\rangle_{1I} = -2/\pi \tag{30}$$

$$\langle s_2\rangle_{1R} = -2\sin(d)/\pi, \langle s_2\rangle_{1I} = -2\cos(d)/\pi. \tag{31}$$

The same concept is applied to the rest of the variables. Variables such as submodule capacitor voltage (v_{Cyi}) and LVDC port voltage (v_{Co}) are considered to be pure dc, thus the ac components are zero. On the other hand, s_1, s_2, i_{Lrp}, v_{Crp}, and $v_{Crs}{}'$ have zero average value, thus only the first-order harmonic is considered.

There are two important properties to derive GAM: the derivative and variable product, which are given, respectively, as follows:

$$\frac{d}{dt}\langle x\rangle_k(t) = \left\langle \frac{d}{dt}x \right\rangle_k(t) - jk\omega_{sw}\langle x\rangle_k(t) \tag{32}$$

$$\langle x\cdot y\rangle_k(t) = \sum_i \langle x\rangle_{k-i}(t)\cdot\langle y\rangle_i(t) \tag{33}$$

where k and i are the harmonic orders, and x and y are the two variables to be multiplied. In this case, only the zero- and first-order harmonics are considered ($k, i = -1, 0, 1$).

After expressing all state variables into their Fourier series representations and applying the properties in (32) and (33) to all derivatives and multiplications, the GAM of the Q-CLLC converter can be obtained as follows:

$$\frac{d}{dt}\langle v_{cu1}\rangle_0 = \frac{M_i}{C_{u1}}i_u + \frac{4\langle i_{Lrp}\rangle_{1I}}{\pi C_{u1}} \tag{34}$$

$$\frac{d}{dt}\langle v_{Crp}\rangle_{1R} = \frac{\langle i_{Lrp}\rangle_{1R}}{C_{rp}} + \omega_{sw}\langle v_{Crp}\rangle_{1I} \tag{35}$$

$$\frac{d}{dt}\langle v_{Crp}\rangle_{1I} = \frac{\langle i_{Lrp}\rangle_{1I}}{C_{rp}} - \omega_{sw}\langle v_{Crp}\rangle_{1R} \tag{36}$$

$$\frac{d}{dt}\langle v_{Crs}{}'\rangle_{1R} = \frac{\langle i_{Lrs}{}'\rangle_{1R}}{C_{rs}{}'} + \omega_{sw}\langle v_{Crs}{}'\rangle_{1I} \tag{37}$$

$$\frac{d}{dt}\langle v_{Crs}{}'\rangle_{1I} = \frac{\langle i_{Lrs}{}'\rangle_{1I}}{C_{rs}{}'} - \omega_{sw}\langle v_{Crs}{}'\rangle_{1R} \tag{38}$$

$$\frac{d}{dt}\langle i_{Lrp}\rangle_{1R} = -\frac{\langle v_{Crp}\rangle_{1R}}{L_{rp}} + \omega_{sw}\langle i_{Lrp}\rangle_{1I} - \frac{L_m}{L_{rp}}\frac{d\langle i_m\rangle_{1R}}{dt} + \omega_{sw}\frac{L_m}{L_{rp}}\langle i_m\rangle_{1I} \tag{39}$$

$$\frac{d}{dt}\langle i_{Lrp}\rangle_{1I} = -\frac{2}{\pi L_{rp}}\langle v_{Cu1}\rangle_0 - \frac{\langle v_{Crp}\rangle_{1I}}{L_{rp}} - \omega_{sw}\langle i_{Lrp}\rangle_{1R} - \frac{L_m}{L_{rp}}\frac{d\langle i_m\rangle_{1I}}{dt} - \omega_{sw}\frac{L_m}{L_{rp}}\langle i_m\rangle_{1R} \tag{40}$$

$$\frac{d}{dt}\langle i_{Lrs}{}'\rangle_{1R} = \omega_{sw}\langle i_{Lrs}{}'\rangle_{1I} + \frac{L_m}{L_{rs}{}'}\frac{d\langle i_m\rangle_{1R}}{dt} - \omega_{sw}\frac{L_m}{L_{rs}{}'}\langle i_m\rangle_{1I} - \frac{\langle v_{Crs}{}'\rangle_{1R}}{L_{rs}{}'} + \frac{2\sin d\langle v_{Co}{}'\rangle_0}{\pi L_{rs}{}'} \tag{41}$$

$$\frac{d}{dt}\langle i_{Lrs}{}'\rangle_{1I} = -\omega_{sw}\langle i_{Lrs}{}'\rangle_{1R} + \frac{L_m}{L_{rs}{}'}\frac{d\langle i_m\rangle_{1I}}{dt} + \omega_{sw}\frac{L_m}{L_{rs}{}'}\langle i_m\rangle_{1R} - \frac{\langle v_{Crs}{}'\rangle_{1I}}{L_{rs}{}'} + \frac{2\cos d\langle v_{Co}{}'\rangle_0}{\pi L_{rs}{}'} \tag{42}$$

$$\langle \dot{v}_{Co}'\rangle_0 = -\frac{4\sin(d)\langle i_{Lrs}{}'\rangle_{1R}}{\pi C_o{}'} - \frac{4\cos(d)\langle i_{Lrs}{}'\rangle_{1I}}{\pi C_o{}'} - \frac{\langle V_{Co}{}'\rangle_0}{R_o{}'C_o{}'}. \tag{43}$$

The ac variables are expressed in terms of real and imaginary components, whereas the dc variables represent their average values. Small-signal perturbation is applied to (34)–(43) and the small-signal model of the Q-CLLC converter is expressed as (A1)–(A10) in Appendix A.

C. BLOCK DIAGRAM REPRESENTATION AND MODEL VERIFICATION

Before designing the controller, related transfer functions should be derived. Therefore, the transfer functions of the small-signal models in (11)–(14) for the MMC and (A1)–(A10) for the Q-CLLC converter are represented in block diagram forms as shown in Figs. 23 and 24 for the MMC and Q-CLLC converter, respectively (see Appendix B). The block diagram is only for the upper arm, meanwhile for the lower arm is identical; thus, it is not drawn for simplicity. As can be seen, there are two control variables for the system: modulation index m_i and switching frequency ω_{sw}. All the state variables can be obtained by inputting these variables into the model. To verify the model accuracy, the control-to-output transfer functions for the MMC and Q-CLLC converter are derived.

First, the control-to-output transfer function for the MMC can be expressed as follows:

$$G_{CO-1}(s) = \frac{\tilde{v}_{Cu1}(s)}{\tilde{m}_i(s)} = \frac{\bar{I}_u - (NV_{Cu1} - 0.5V_{DC})\bar{M}_i G_1(s)}{sC_{u1} + N\bar{M}_i^2 G_1(s)}. \tag{44}$$

Notice that the time constant of balancing control system depends on L_{arm}, whose value is relatively large, since its main role is to reduce the circulating current. This large time constant limits the bandwidth of the conventional method and it is inevitable since L_{arm} naturally appears in the voltage

TABLE 4. Parameters for Simulation and Experiments

Symbol	Description	Value
MMC-side		
P_{MVAC}	Rated power of the MVAC port	1 kW
N	Number of submodules per arm	3
V_{dc}	DC-link voltage	400 V
C_{xyi}	Submodule capacitor	2.2 mF
L_{arm}	Arm inductor	2 mH
R_{arm}	ESR of L_{arm}	0.06 Ω
L_g	Grid inductance	2.2 mH
e_g	Grid voltage (rms)	110 V
f_g	Grid frequency	60 Hz
f_{sw}	Switching frequency	2500 Hz
Q-CLLC converter-side		
P_{LVDC}	Rated power of one LVDC port	700 W
V_{Co1}, V_{Co2}	LVDC port voltages	100 V
C_{in}	Half-bridge capacitor	10 μF
L_{rp}, L_{rs}	Resonant inductor	10 μH
C_{rp}, C_{rs}	Resonant capacitor	470 nF
L_m	Magnetizing inductance	258 μH
C_o	LVDC-side capacitor	2.2 mF
n	Transformer turn ratio	0.56
f_{res}	Resonant frequency	75 kHz
f_{sw}	Switching frequency	75 – 150 kHz

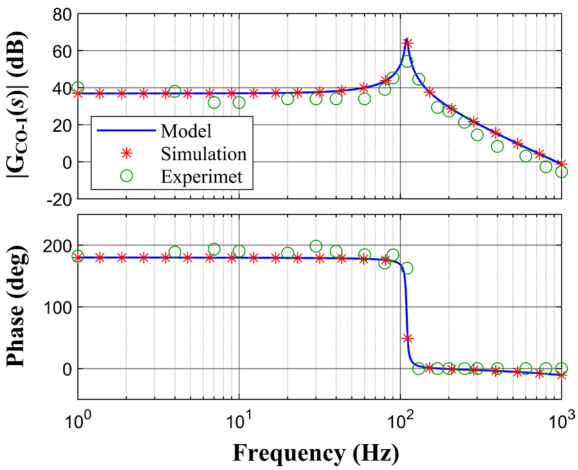

FIGURE 9. Bode plot verification of $G_{CO\text{-}1}(s)$.

balancing control loop. Using the parameters listed in Table 4, the Bode plot of (44) is drawn together with the simulation and experimental data in Fig. 9. It is noticed that the derived model is accurate.

For the Q-CLLC converter, the model contains several feedforward terms. In the imaginary part, there are some feedforward terms from the real part, e.g., $\langle\tilde{i}_{Lrp}\rangle_{1R}$ and $\langle\tilde{v}_{Crp}\rangle_{1R}$. When deriving the control-to-output transfer function, these terms can be neglected for simplification, as shown in Fig. 10. The gains are expressed as follows:

$$G_{\mathrm{Im1}}(s) = \langle\bar{I}_{Lrp}\rangle_{1R} + \langle\bar{I}_m\rangle_{1R}\frac{L_m}{L_{rp}} + \frac{\langle\bar{V}_{Crp}\rangle_{1R}}{sL_{rp}} \tag{45}$$

$$G_{\mathrm{Im2}}(s) = -\langle\bar{I}'_{Lrs}\rangle_{1R} + \langle\bar{I}_m\rangle_{1R}\frac{L_m}{L_{rs}'} + \frac{\langle\bar{V}'_{Crs}\rangle_{1R}}{sL_{rs}'} \tag{46}$$

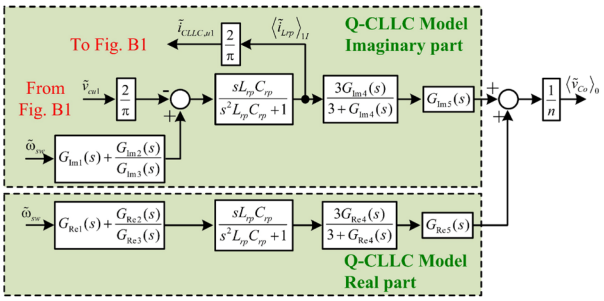

FIGURE 10. Simplified block diagram of Q-CLLC converter with all feedforward terms neglected.

$$G_{\mathrm{Im3}}(s) = G_{\mathrm{Re3}}(s) = \left(\frac{sL_{rp}C_{rp}}{s^2L_{rp}C_{rp}+1}\right)\left(\frac{3L_{rp}}{L_{rp}+3L_m}\right)\left(\frac{sL_m}{L_{rs}'}\right) \tag{47}$$

$$G_{\mathrm{Im4}}(s) = G_{\mathrm{Re4}}(s) = \left(\frac{3L_{rp}}{L_{rp}+3L_m}\right)\left(\frac{sL_m}{L_{rs}'}\right)\left(\frac{sL_{rs}'C_{rs}'}{s^2L_{rs}'C_{rs}'+1}\right) \tag{48}$$

$$G_{\mathrm{Im5}}(s) = \frac{-s\pi L_{rs}'\cos(d)G_2(s)}{s\pi L_{rs}' + 2\cos^2(d)G_2(s)} \tag{49}$$

$$G_{\mathrm{Re1}}(s) = \langle\bar{I}_{Lrp}\rangle_{1I} + \langle\bar{I}_m\rangle_{1I}\frac{L_m}{L_{rp}} + \frac{\langle\bar{V}_{Crp}\rangle_{1I}}{sL_{rp}} \tag{50}$$

$$G_{\mathrm{Re2}}(s) = \langle\bar{I}'_{Lrs}\rangle_{1I} - \langle\bar{I}_m\rangle_{1I}\frac{L_m}{L_{rs}'} + \frac{\langle\bar{V}'_{Crs}\rangle_{1I}}{sL_{rs}'} \tag{51}$$

$$G_{\mathrm{Re5}}(s) = \frac{-s\pi L_{rs}'\sin(d)G_2(s)}{s\pi L_{rs}' + 2\sin^2(d)G_2(s)} \tag{52}$$

$$G_2(s) = \frac{4}{\pi}\frac{R_o'}{sR_o'C_o'+1}. \tag{53}$$

Therefore, the control-to-output transfer functions of the Q-CLLC converter can be derived as follows:

$$G_{CO-2}(s) = \frac{\langle\tilde{v}_{Co}\rangle_0(s)}{\omega_{sw}(s)} = \frac{1}{n}\left[G_{f\_\mathrm{Im}}(s) + G_{f\_\mathrm{Re}}(s)\right] \tag{54}$$

$$G_{f\_\mathrm{Im}}(s) = \left(G_{\mathrm{Im1}}(s) + \frac{G_{\mathrm{Im2}}(s)}{G_{\mathrm{Im3}}(s)}\right) \times \left(\frac{sL_{rp}C_{rp}}{s^2L_{rp}C_{rp}+1}\right) \times \left(\frac{3G_{\mathrm{Im4}}(s)}{3+G_{\mathrm{Im4}}(s)}\right) \times G_{\mathrm{Im5}}(s) \tag{55}$$

$$G_{f\_\mathrm{Re}}(s) = \left(G_{\mathrm{Re1}}(s) + \frac{G_{\mathrm{Re2}}(s)}{G_{\mathrm{Re3}}(s)}\right) \times \left(\frac{sL_{rp}C_{rp}}{s^2L_{rp}C_{rp}+1}\right) \times \left(\frac{3G_{\mathrm{Re4}}(s)}{3+G_{\mathrm{Re4}}(s)}\right) \times G_{\mathrm{Re5}}(s). \tag{56}$$

Notice that differently from the conventional method, the time constant depends on the resonant inductance and capacitance values, which are much lower compared to L_{arm}. Consequently, the time constant is much shorter, and response

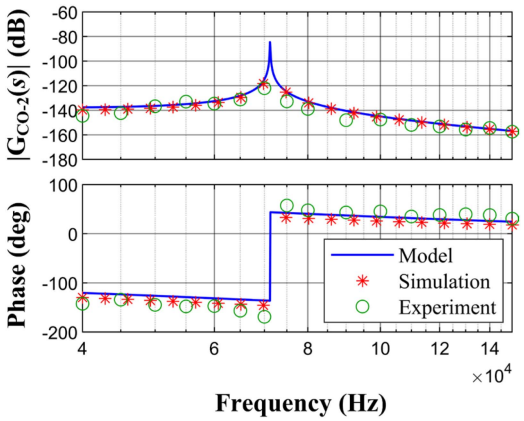

FIGURE 11. Bode plot verification of $G_{CO\text{-}2}(s)$.

time is much faster. The Bode plot of (54) is drawn in Fig. 11, and then compared with the simulation and experimental results. It is also shown that the model for the Q-CLLC converter is accurate.

IV. PROPOSED CONTROL SCHEME

For the MMC-based SST, the following three control objectives should be fulfilled.

1) MMC leg voltage control.
2) MMC submodule capacitor voltage balancing control.
3) LVDC port voltage control.

The first and third objectives are applied to the MMC and the Q-CLLC converter, respectively. As discussed in Section I, the submodule capacitor voltage balancing is crucial in modular systems. Conventionally, this balancing control is applied to the MMC. However, the MMC is operated at low switching frequency, which limits the controller bandwidth, leading to a slower dynamic response, and narrower stability margin.

To overcome these challenges, the balancing control can be applied to the Q-CLLC converter, which is operated at a high switching frequency. As a consequence, the balancing control loop has higher bandwidth, faster dynamic response, and wider stability margin.

The control-to-output transfer function for the proposed balancing scheme according to Figs. 10, 23, and 24 can be derived as follows:

$$G_{CO-3}(s) = \frac{\tilde{v}_{Cu}(s)}{\tilde{\omega}_{sw}(s)} = \frac{2}{s\pi C_{u1}}\left(G_{\mathrm{Im}1}(s)+\frac{G_{\mathrm{Im}2}(s)}{G_{\mathrm{Im}3}(s)}\right)\left(\frac{sL_{rp}C_{rp}}{s^2L_{rp}C_{rp}+1}\right). \quad (57)$$

The closed-loop voltage balancing controller is shown in Fig. 12, where the PI controller ($G_{\mathrm{PI}}(s) = K_p + K_i/s$) is used both for the conventional and proposed methods. In the conventional method, the PI controller output is the modulation signal m_i to balance the submodule capacitor voltages, whereas for the proposed method is the switching frequency ω_{sw}.

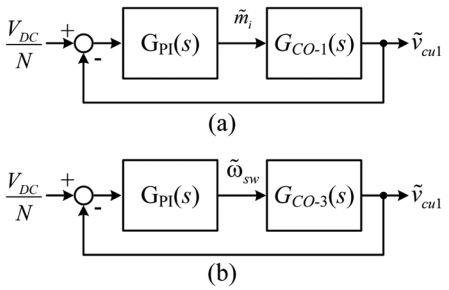

FIGURE 12. Closed-loop voltage balancing controller. (a) Conventional method. (b) Proposed method.

TABLE 5. Controller Gains for 60° Phase Margin

Conventional method		Proposed method	
K_p	K_i	K_p	K_i
0.006	0.006	0.479	271.27

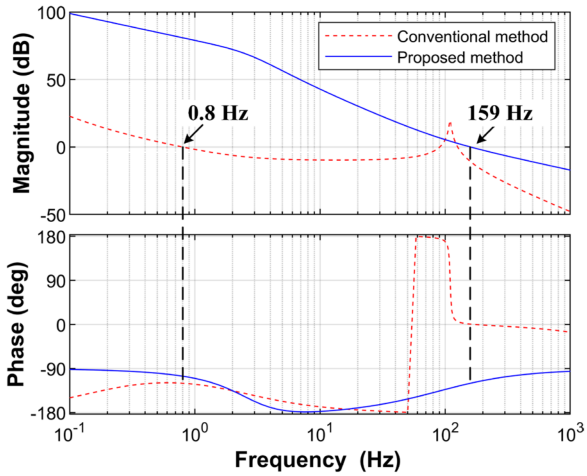

FIGURE 13. Bode plots of open-loop transfer functions in (58) and (59).

The open-loop transfer functions can be derived for the conventional and proposed methods, respectively, as follows:

$$G_O(s)|_{conv} = G_{\mathrm{PI}}(s) \times G_{CO-1}(s) \quad (58)$$

$$G_O(s)|_{prop} = G_{\mathrm{PI}}(s) \times G_{CO-3}(s). \quad (59)$$

To analyze the control-loop performance, the controller bandwidth is compared, where the phase margin of both controllers is set at 60°. The transfer functions in (58) and (59) are imported to MATLAB PIDTOOL and the values of K_p and K_i can be obtained. In Table 5, the controller gains are listed. The open-loop transfer functions are depicted in Fig. 13, from which the bandwidths for the conventional and proposed methods are 0.8 Hz and 159 Hz, respectively. With a higher bandwidth, the proposed controller has larger stability margin and faster response.

Pole-zero map and Nyquist path of the closed-loop transfer function are shown in Figs. 14 and 15, respectively. Fig. 14(a) shows that all the poles for both methods are located on the

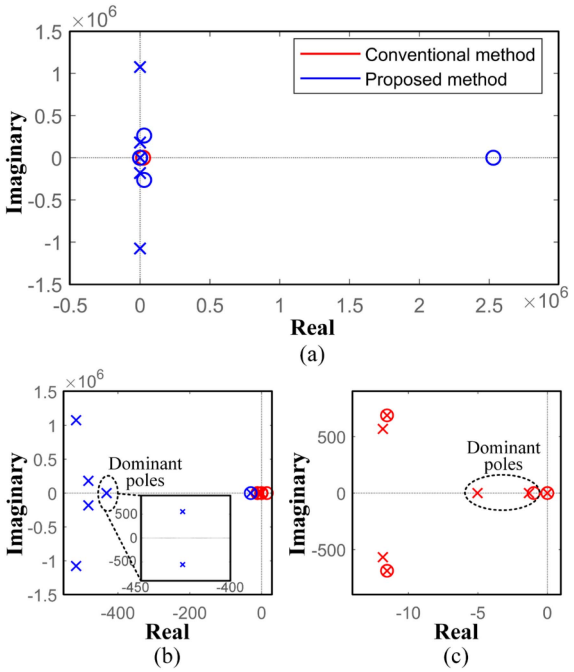

FIGURE 14. Pole-zero map of the closed-loop transfer functions of the conventional and proposed methods. (a) Zoomed-out view. (b) Zoomed-in view of the proposed method. (c) Zoomed-in view of the conventional method.

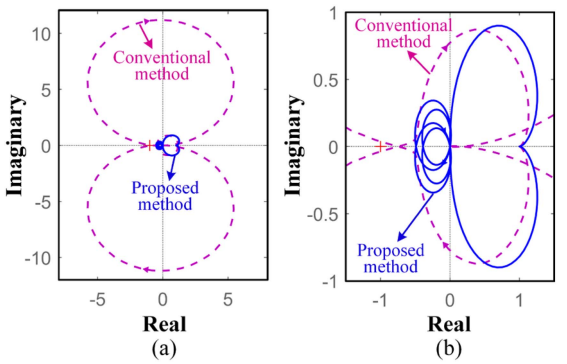

FIGURE 15. Nyquist path of the closed-loop transfer functions of the conventional and proposed methods. (a) Zoomed-out view. (b) Zoomed-in view near $-1 + j0$.

left-half plane, indicating both systems are stable. However, the pole locations in the conventional method are closer to the imaginary axis, as shown in Fig. 14(b) and (c). The dominant poles are of two distinct real values at -5 and -1.3, whereas the proposed method has a pair of complex conjugates at $-432 \pm$ j554. Moreover, Fig. 15 shows that the Nyquist path in the proposed method is farther from $-1 +$ j0. Therefore, it is verified that applying the balancing control to the Q-CLLC converter is more beneficial.

Finally, the overall control block diagram of the proposed method is shown in Fig. 16. The controller of MMC in Fig. 16(a) consists of average leg voltage, circulating current, and grid current controllers. For a three-phase system, this control scheme can be extended in the same manner. The

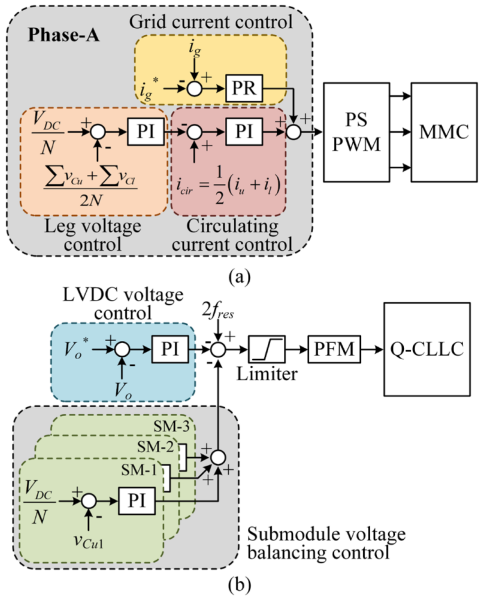

FIGURE 16. Control block diagram of the MMC-based SST for upper and lower arms. (a) MMC controller. (b) Q-CLLC converter controller.

PSPWM is applied to modulate MMC switches. Fig. 16(b) shows the controller of Q-CLLC converter controller, which consists of LVDC voltage and MMC submodule capacitor voltage balancers. The switching frequency is adjusted by using pulse frequency modulation to maintain a constant output voltage based on the input–output gain of the Q-CLLC converter. In this control scheme, the switching frequency is limited to twice the resonant frequency to limit the skin effect and core losses from the inductors and transformer [32].

V. EXPERIMENTAL RESULTS

To verify the effectiveness of the proposed method, a laboratory-scaled prototype with 2.4 kW total power has been built, as shown in Fig. 17, where GaN TP65H035WS is used for the switches and a TMS320F28379D DSP is used to control the system. The system parameters are listed in Table 4.

The operation of the MMC-based SST at the rated condition is shown in Fig. 18. The grid current is controlled at 10.6 A (rms) with the PR controller. The upper and lower submodule capacitor voltages are balanced with the proposed method, where the peak-to-peak ripple is maintained lower than 10 %. The proposed system consists of two separated LVDC ports and their voltages are maintained at 100 V by adjusting the switching frequency.

Fig. 19 shows the bridge voltage (v_{px} and v_s) and transformer currents of the Q-CLLC converter at the rated condition, both on the primary and secondary sides. It can be clearly seen that the switching frequency of the converter is 94 kHz with a 19° phase shift between the primary and secondary sides. The soft switching operation is confirmed by observing the waveforms of the switch voltage and transformer currents, as shown in Fig. 20. Note that only the operation of the upper leg switches is shown since that of the lower leg switches is

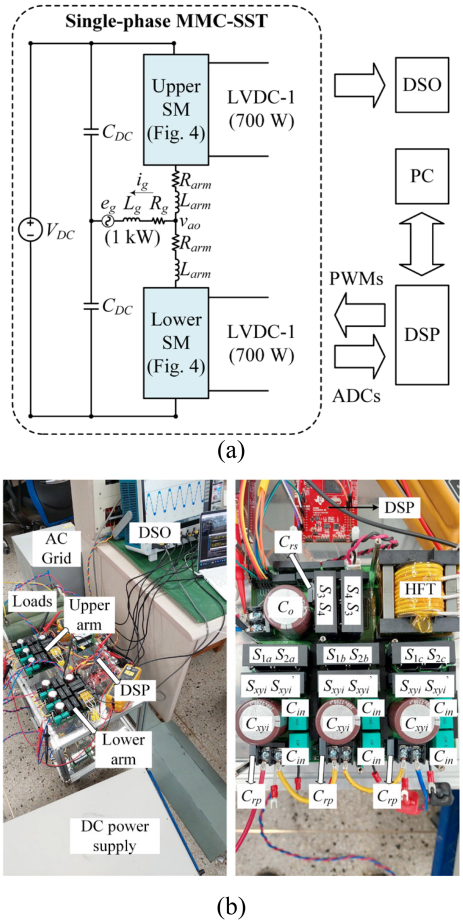

FIGURE 17. Experimental setup. (a) Configuration of the setup. (b) Hardware and submodule.

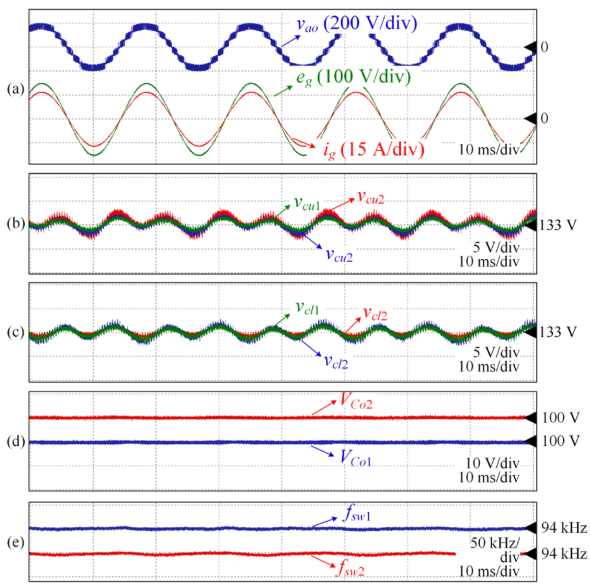

FIGURE 18. Experimental results of the MMC-based SST at rated condition. (a) MMC output voltage and grid current. (b) Upper arm submodule capacitor voltages. (c) Lower arm submodule capacitor voltages. (d) LVDC port voltages. (e) Switching frequencies of Q-CLLC converters.

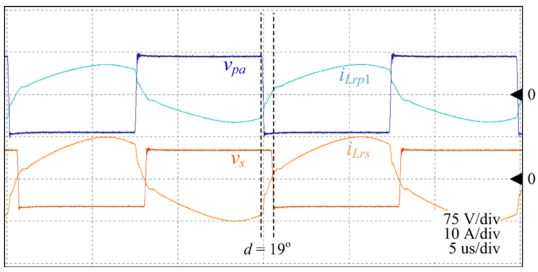

FIGURE 19. Bridge voltages and transformer currents of the Q-CLLC converter.

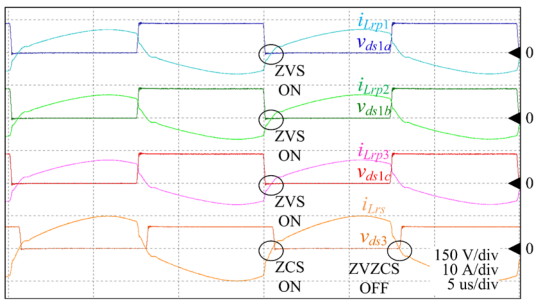

FIGURE 20. Switch voltages and transformer currents on primary and secondary sides.

the same. When the drain-to-source voltage (v_{ds}) of the switch is zero, the transformer current is still negative, indicating the body diode is still conducting. Thus, the switch begins to conduct when the voltage across it is zero, indicating zero voltage switching turn-ON. Since the converter is operated above the resonant frequency, soft switching cannot be achieved during the turn-OFF transition. On the other hand, body diodes are operating on the secondary side. Ideally, it may turn ON and OFF at zero voltage and zero current switching (ZVZCS). However, due to PCB nonidealities, it turns ON at zero current switching and turns OFF at ZVZCS. Furthermore, it is also shown that the resonant currents are balanced, which confirms the model verification developed in the previous section is valid.

Due to two separated LVDC ports, unbalanced power transfer may occur. Fig. 21 shows the MMC-based SST performance when the output power of LVDC 2 is decreased from 700 to 150 W while keeping that of LVDC 1 at 700 W. It can be seen that the LVDC output voltages are maintained constant at 100 V. The switching frequency is increased for the Q-CLLC converter at lower output power. Therefore, it corresponds to the input–output gain shown in Fig. 6. Moreover, the submodule capacitor voltages are maintained as balanced without any large overshoot and oscillation, which shows the effectiveness of the proposed control method.

The voltage balancing control performance is compared between the conventional and proposed methods, which is shown in Fig. 22. The load of LVDC 1 remains constant at 700 W, whereas the load of LVDC 2 is changed from 700 to 150 W and back to 700 W. With the conventional method,

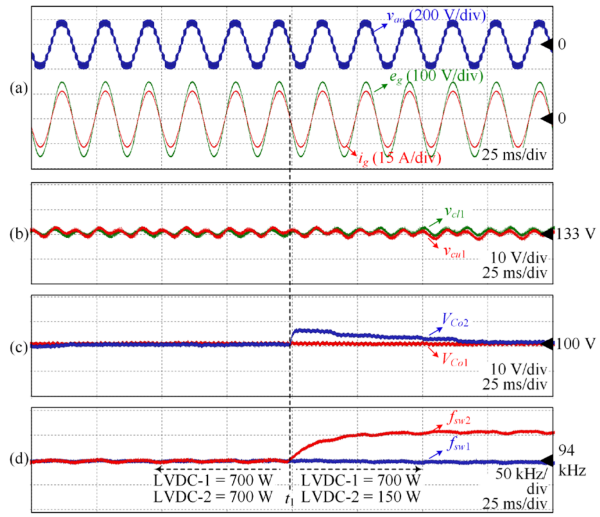

FIGURE 21. Experimental results when the load of LVDC 2 is changed from 700 to 150 W. (a) MMC output voltage and grid current. (b) First upper and lower submodule capacitor voltages. (c) LVDC port voltages. (d) Switching frequencies of Q-CLLC converters.

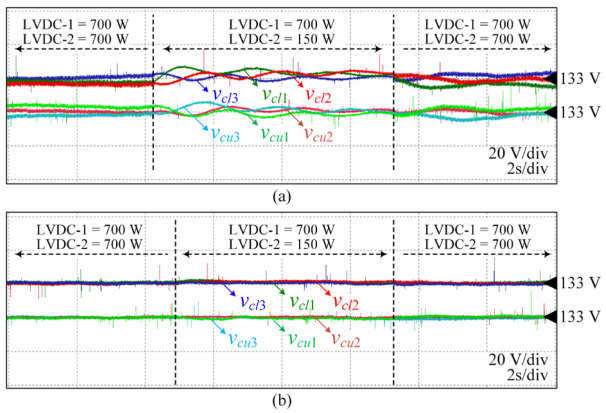

FIGURE 22. Transient responses of submodule capacitor voltages during step load change (700 to 150 W and back to 700 W) at port LVDC 2. (a) Conventional method. (b) Proposed method.

the submodule capacitor voltage oscillates with 8.8 % of overshoot during stepwise load change and takes a longer response time to reach the steady state. Note that the submodule capacitor voltages will converge to their nominal values after a longer time (approximately larger than 6 s). This problem can be solved by the balancing control applied to the Q-CLLC converter which has higher bandwidth and more stable region, as discussed in Section IV, with 1.5 % of overshoot and approximately 2 s of settling time.

VI. CONCLUSION

This article has proposed a novel balancing control scheme of submodule capacitor voltages for the four-port MMC-based SST system which consist of MVAC, MVDC, and two LVDC ports. For the SST isolation, the Q-CLLC converter has been adopted and analyzed in detail. Unlike the conventional method, the proposed balancing scheme is applied to

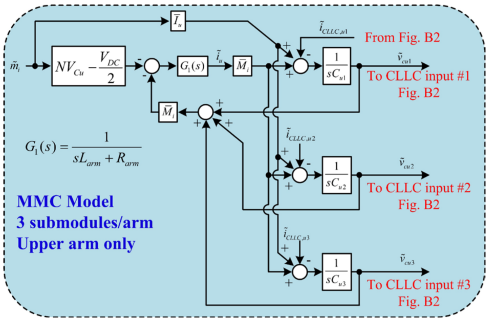

FIGURE 23. Block diagram of the upper arm MMC (the model for the lower arm is identical).

the Q-CLLC converter, which is operated at high switching frequency. The advantages of applying the balancing control to the Q-CLLC converter are higher bandwidth, faster response, and wider stability margin. The controller gains have been designed thoroughly, which begins from the derivation and verification of the small-signal model, block diagram representation, and transfer function analyses. Pole-zero map and Nyquist path analyses have also validated the stability of the voltage balancing control loop. Experimental results for a 2.4-kW prototype system have also verified the accuracy of the model and effectiveness of the proposed balancing control.

APPENDIX A
SMALL-SIGNAL MODEL OF Q-CLLC CONVERTER

This section continues the discussion in Section III-B. The small-signal model for the Q-CLLC converter after applying the small-signal perturbation to the GAM can be expressed as follows:

$$\frac{d}{dt}\langle\tilde{v}_{Cu1}\rangle_0 = \frac{1}{C_{u1}}\left[\bar{M}_i\tilde{i}_u + \bar{I}_u\tilde{m}_i + \frac{2\langle\tilde{i}_{Lrp}\rangle_{1I}}{\pi}\right] \tag{A1}$$

$$\frac{d}{dt}\langle\tilde{v}_{Crp}\rangle_{1R} = \frac{\langle\tilde{i}_{Lrp}\rangle_{1R}}{C_{rp}} + \bar{\Omega}_{sw}\langle\tilde{v}_{Crp}\rangle_{1I} + \langle\bar{V}_{Crp}\rangle_{1I}\tilde{\omega}_{sw} \tag{A2}$$

$$\frac{d}{dt}\langle\tilde{v}_{Crp}\rangle_{1I} = \frac{\langle\tilde{i}_{Lrp}\rangle_{1I}}{C_{rp}} - \bar{\Omega}_{sw}\langle\tilde{v}_{Crp}\rangle_{1R} - \langle\bar{V}_{Crp}\rangle_{1R}\tilde{\omega}_{sw} \tag{A3}$$

$$\frac{d}{dt}\langle\tilde{v}'_{Crs}\rangle_{1R} = \frac{\langle\tilde{i}'_{Lrs}\rangle_{1R}}{C_{rp}} + \bar{\Omega}_{sw}\langle\tilde{v}'_{Crs}\rangle_{1I} + \langle\bar{V}'_{Crs}\rangle_{1I}\tilde{\omega}_{sw} \tag{A4}$$

$$\frac{d}{dt}\langle\tilde{v}'_{Crs}\rangle_{1I} = \frac{\langle\tilde{i}'_{Lrs}\rangle_{1I}}{C_{rp}} - \bar{\Omega}_{sw}\langle\tilde{v}'_{Crs}\rangle_{1R} - \langle\bar{V}'_{Crs}\rangle_{1R}\tilde{\omega}_{sw} \tag{A5}$$

$$\frac{d}{dt}\langle\tilde{i}_{Lrp}\rangle_{1R} = -\frac{\langle\tilde{v}_{Crp}\rangle_{1R}}{L_{rp}} + \bar{\Omega}_{sw}\langle\tilde{i}_{Lrp}\rangle_{1I} + \frac{\bar{\Omega}_{sw}L_m}{L_{rp}}\langle\tilde{i}_m\rangle_{1I} - \frac{L_m}{L_{rp}}\frac{d}{dt}\langle\tilde{i}_m\rangle_{1R} + \left(\langle\bar{I}_{Lrp}\rangle_{1I} + \frac{\langle\bar{I}_m\rangle_{1I}L_m}{L_{rp}}\right)\tilde{\omega}_{sw} \tag{A6}$$

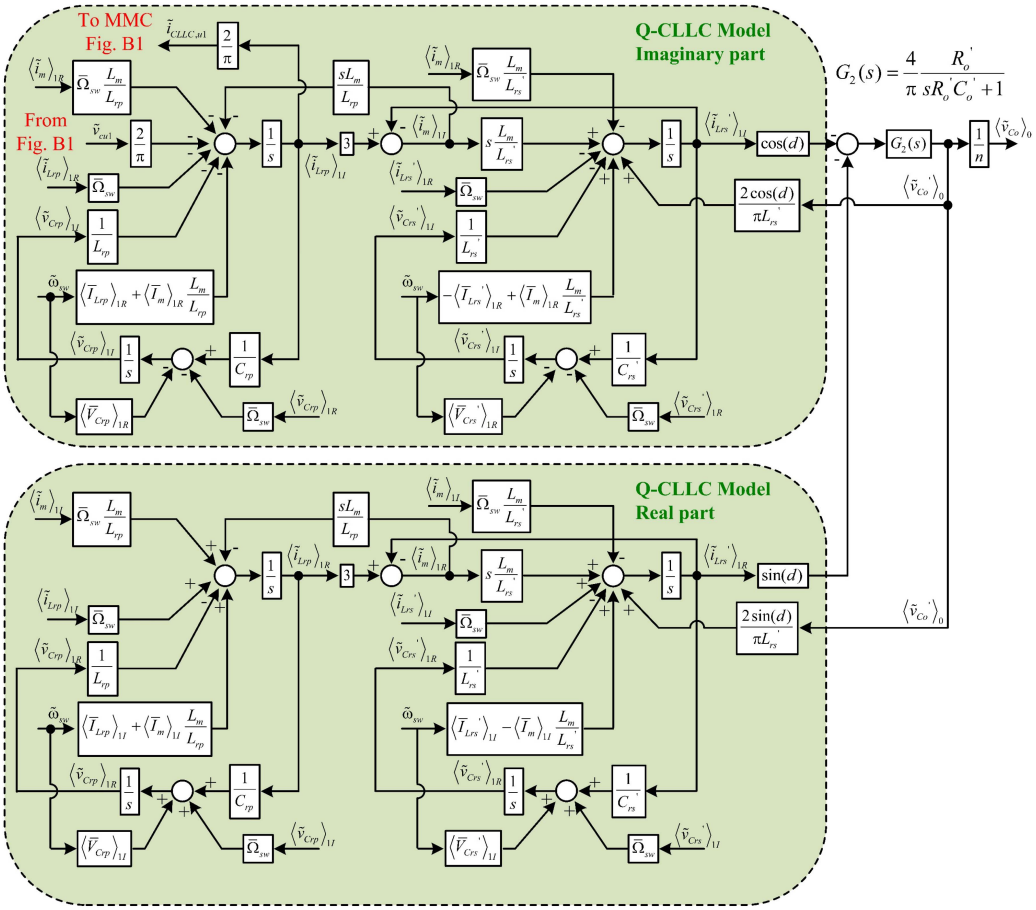

FIGURE 24. Block diagram of the Q-CLLC converter.

$$\frac{d}{dt}\langle\tilde{i}_{Lrp}\rangle_{1I} = -\frac{2\langle\tilde{v}_{Cu1}\rangle_{1I}}{\pi L_{rp}} - \frac{\langle\tilde{v}_{Crp}\rangle_{1I}}{L_{rp}} - \bar{\Omega}_{sw}\langle\tilde{i}_{Lrp}\rangle_{1R} - \frac{\bar{\Omega}_{sw}L_m}{L_{rp}}\langle\tilde{i}_m\rangle_{1R} - \frac{L_m}{L_{rp}}\frac{d}{dt}\langle\tilde{i}_m\rangle_{1I} - \left(\langle\bar{I}_{Lrp}\rangle_{1R} + \frac{\langle\bar{I}_m\rangle_{1R}L_m}{L_{rp}}\right)\tilde{\omega}_{sw} \tag{A7}$$

$$\frac{d}{dt}\langle\tilde{i}'_{Lrs}\rangle_{1R} = -\frac{\langle\tilde{v}'_{Crs}\rangle_{1R}}{L_{rs}'} + \frac{2\sin(d)}{\pi L_{rs}'}\langle\tilde{v}'_{Co}\rangle_0 + \bar{\Omega}_{sw}\langle\tilde{i}'_{Lrs}\rangle_{1I} - \frac{\bar{\Omega}_{sw}L_m}{L_{rs}'}\langle\tilde{i}_m\rangle_{1I} + \frac{L_m}{L_{rs}'}\frac{d}{dt}\langle\tilde{i}_m\rangle_{1R} + \left(\langle\bar{I}'_{Lrs}\rangle_{1I} - \frac{\langle\bar{I}_m\rangle_{1I}L_m}{L_{rs}'}\right)\tilde{\omega}_{sw} \tag{A8}$$

$$\frac{d}{dt}\langle\tilde{i}'_{Lrs}\rangle_{1I} = -\frac{\langle\tilde{v}'_{Crs}\rangle_{1I}}{L_{rs}'} + \frac{2\cos(d)}{\pi L_{rs}'}\langle\tilde{v}'_{Co}\rangle_0 - \bar{\Omega}_{sw}\langle\tilde{i}'_{Lrs}\rangle_{1R} + \frac{\bar{\Omega}_{sw}L_m}{L_{rs}'}\langle\tilde{i}_m\rangle_{1R} + \frac{L_m}{L_{rs}'}\frac{d}{dt}\langle\tilde{i}_m\rangle_{1I} - \left(\langle\bar{I}'_{Lrs}\rangle_{1R} - \frac{\langle\bar{I}_m\rangle_{1R}L_m}{L_{rs}'}\right)\tilde{\omega}_{sw} \tag{A9}$$

$$\frac{d}{dt}\langle v_{Co}'\rangle_0 = -\frac{4}{\pi C_o'}\left[\sin(d)\langle\tilde{i}'_{Lrs}\rangle_{1R} + \cos(d)\langle\tilde{i}'_{Lrs}\rangle_{1I}\right] - \frac{\langle v_{Co}'\rangle_0}{R_o'C_o'}. \tag{A10}$$

APPENDIX B
BLOCK DIAGRAM REPRESENTATION OF THE MMC-BASED SST SYSTEM

As discussed in Section III-C, to design the system controller, it is often desirable to represent all the equations in block diagrams. To do this, the Laplace transformation is performed to all equations, so that they can be represented in the frequency domain. The block diagram of the MMC-based SST system is shown in Figs. 23 and 24 for the MMC side and Q-CLLC converter side, respectively.

REFERENCES

[1] M. Rouhani and G. J. Kish, "Multiport DC–DC–AC modular multilevel converters for hybrid AC/DC power systems," *IEEE Trans. Power Del.*, vol. 35, no. 1, pp. 408–419, Feb. 2020, doi: 10.1109/TPWRD.2019.2927324.

[2] H. Yuan, H. S. Lam, N. Beniwal, S. C. Tan, J. Pou, and S. Y. R. Hui, "Cooperative voltage-balancing control for medium-voltage electric-spring system based on diode-clamped converter and dual active bridges," *IEEE Trans. Power Electron.*, vol. 38, no. 10, pp. 11997–12009, Oct. 2023, doi: 10.1109/TPEL.2023.3263184.

[3] N. D. Dao, H. V. Nguyen, and D. C. Lee, "Semi-modular solid-state transformers with reduced count of components based on single-stage AC/DC converters," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 8177–8189, Jul. 2022, doi: 10.1109/TPEL.2022.3152501.

[4] A. C. Nair and B. G. Fernandes, "Solid-state transformer based fast charging station for various categories of electric vehicles with batteries of vastly different ratings," *IEEE Trans. Ind. Electron.*, vol. 68, no. 11, pp. 10400–10411, Nov. 2021, doi: 10.1109/TIE.2020.3038091.

[5] L. Zheng, R. P. Kandula, and D. Divan, "Soft-switching solid-state transformer with reduced conduction loss," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5236–5249, May 2021, doi: 10.1109/TPEL.2020.3030795.

[6] Z. Bu, J. Teng, X. Sun, Y. Pan, and Y. Pan, "Low-frequency voltage ripples decoupling with switched-capacitor conversion for an MMC-based SST," *IEEE Trans. Ind. Electron.*, vol. 69, no. 11, pp. 11293–11303, Nov. 2022, doi: 10.1109/TIE.2021.3121715.

[7] J. Teng, Z. Bu, X. Sun, H. Fu, W. Zhao, and X. Li, "Common high-frequency bus-based cascaded multilevel solid-state transformer with ripple and unbalance power decoupling channel," *IEEE Trans. Power Electron.*, vol. 37, no. 8, pp. 9345–9361, Aug. 2022, doi: 10.1109/TPEL.2022.3153367.

[8] J. Teng et al., "An inductive-filtering strategy of submodule ripple-power in triple-port MMC-based SST applied to hybrid medium and low voltage AC/DC interface," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 8015–8032, Jul. 2022, doi: 10.1109/TPEL.2022.3144279.

[9] J. Zhou et al., "Design and control of power fluctuation delivery for cell capacitance optimization in multiport modular solid-state transformers," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1412–1427, Feb. 2021, doi: 10.1109/TPEL.2020.3006956.

[10] J. D. O. Pacheco, D. D. A. Honorio, and D. D. S. Oliveira, "An AC–DC isolated MMC-based structure suitable for MV SST traction applications," *IEEE Access*, vol. 7, pp. 106395–106406, 2019, doi: 10.1109/ACCESS.2019.2930810.

[11] G. Zheng, Y. Chen, and Y. Kang, "A modular multilevel converter (MMC) based solid-state transformer (SST) topology with simplified energy conversion process and magnetic integration," *IEEE Trans. Ind. Electron.*, vol. 68, no. 9, pp. 7725–7735, Sep. 2021, doi: 10.1109/TIE.2020.3013493.

[12] L. Wang, L. Zhang, and Y. Xiong, "Low-frequency suppression strategy based on MPC without common-mode voltage increases," *J. Power Electron.*, vol. 23, no. 5, pp. 769–778, May 2023, doi: 10.1007/s43236-022-00584-x.

[13] Y. Liu, Z. Duan, Q. Chen, B. Li, M. Ban, and Z. Li, "MMC-modified sub-module structure with double reverse blocking IGBTs," *J. Power Electron.*, vol. 23, no. 3, pp. 434–444, Mar. 2023, doi: 10.1007/s43236-022-00550-7.

[14] A. K. Muthavarapu, J. Biswas, and M. Barai, "An efficient sorting algorithm for capacitor voltage balance of modular multilevel converter with space vector pulsewidth modulation," *IEEE Trans. Power Electron.*, vol. 37, no. 8, pp. 9254–9265, Aug. 2022, doi: 10.1109/TPEL.2022.3160665.

[15] L. Wang, Y. Shi, M. Bosworth, D. Soto, and M. Steurer, "Modular multilevel converter switching frequency harmonics analysis and suppression through cell voltage control," *IEEE Open J. Power Electron.*, vol. 1, pp. 149–160, 2020, doi: 10.1109/OJPEL.2020.2997211.

[16] M. D. Islam, R. Razzaghi, and B. Bahrani, "Arm-sensorless sub-module voltage estimation and balancing of modular multilevel converters," *IEEE Trans. Power Del.*, vol. 35, no. 2, pp. 957–967, Apr. 2020, doi: 10.1109/TPWRD.2019.2931287.

[17] L. Zhang, J. Qin, Y. Zou, Q. Duan, and W. Sheng, "Analysis of capacitor charging characteristics and low-frequency ripple mitigation by two new voltage-balancing strategies for MMC-based solid-state transformers," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 1004–1017, Jan. 2021, doi: 10.1109/TPEL.2020.3000717.

[18] B. Li et al., "Closed-loop precharge control of modular multilevel converters during start-up processes," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 524–531, Feb. 2015, doi: 10.1109/TPEL.2014.2334055.

[19] Q. Hao, Z. Li, C. Yue, F. Gao, and S. Wang, "Small-signal model and dynamics of MMC-HVDC grid under unbalanced grid conditions," *IEEE Trans. Power Del.*, vol. 36, no. 5, pp. 3172–3184, Oct. 2021, doi: 10.1109/TPWRD.2020.3035650.

[20] G. Bergna-Diaz, J. Freytes, X. Guillaud, S. D'Arco, and J. A. Suul, "Generalized voltage-based state-space modeling of modular multilevel converters with constant equilibrium in steady state," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 2, pp. 707–725, Jun. 2018, doi: 10.1109/JESTPE.2018.2793159.

[21] S. P. Martin, X. Dong, and H. Li, "Model development and predictive control of a low-inertia DC solid-state transformer (SST)," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 6, pp. 6482–6494, Dec. 2022, doi: 10.1109/JESTPE.2022.3159621.

[22] G. Zheng, Y. Chen, and Y. Kang, "Modeling and control of the modular multilevel converter (MMC) based solid state transformer (SST) with magnetic integration," *CES Trans. Elect. Mach. Syst.*, vol. 4, no. 4, pp. 309–318, Jan. 2021, doi: 10.30941/cestems.2020.00038.

[23] D. Braeckle, P. Himmelmann, L. Groll, V. Hagenmeyer, and M. Hiller, "Energy pulsation reduction in modular multilevel converters using optimized current trajectories," *IEEE Open J. Power Electron.*, vol. 2, pp. 171–186, 2021, doi: 10.1109/OJPEL.2021.3065115.

[24] H. Qin and J. W. Kimball, "Generalized average modeling of dual active bridge DC–DC converter," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 2078–2084, Apr. 2012, doi: 10.1109/TPEL.2011.2165734.

[25] J. A. Mueller and J. W. Kimball, "An improved generalized average model of DC–DC dual active bridge converters," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9975–9988, Nov. 2018, doi: 10.1109/TPEL.2018.2797966.

[26] S. S. Shah and S. Bhattacharya, "A simple unified model for generic operation of dual active bridge converter," *IEEE Trans. Ind. Electron.*, vol. 66, no. 5, pp. 3486–3495, May 2019, doi: 10.1109/TIE.2018.2850012.

[27] L. F. Costa, G. Buticchi, and M. Liserre, "Modular smart transformer architectures: An overview and proposal of a interphase architecture," in *Proc. IEEE 8th Int. Symp. Power Electron. Distrib. Gener. Syst.*, 2017, pp. 1–7, doi: 10.1109/PEDG.2017.7972557.

[28] B. Li, R. Yang, D. Xu, G. Wang, W. Wang, and D. Xu, "Analysis of the phase-shifted carrier modulation for modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 297–310, Jan. 2015, doi: 10.1109/TPEL.2014.2299802.

[29] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. IEEE Bologna Power Tech Conf. Proc.*, 2003, doi: 10.1109/PTC.2003.1304403.

[30] Y. Cao and D. Dong, "Electronic-embedded transformer based DC transformer with trapezoidal current and natural current sharing," *IEEE Trans. Power Electron.*, vol. 38, no. 10, pp. 12348–12354, Oct. 2023, doi: 10.1109/TPEL.2023.3295130.

[31] Y. Cao, K. Ngo, and D. Dong, "A scalable electronic-embedded transformer, a new concept toward ultra-high-frequency high-power transformer in DC–DC converters," *IEEE Trans. Power Electron.*, vol. 38, no. 8, pp. 9278–9293, Aug. 2023, doi: 10.1109/TPEL.2023.3279259.

[32] Z. Li, E. Hsieh, Q. Li, and F. C. Lee, "High-frequency transformer design with medium-voltage insulation for resonant converter in solid-state transformer," *IEEE Trans. Power Electron.*, vol. 38, no. 8, pp. 9917–9932, Aug. 2023, doi: 10.1109/TPEL.2023.3279030.

[33] L. F. Costa, G. Buticchi, and M. Liserre, "Optimum design of a multiple-active-bridge DC–DC converter for smart transformer," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10112–10121, Dec. 2018, doi: 10.1109/TPEL.2018.2799680.

[34] N. Naseem and H. Cha, "Quad-active-bridge converter with current balancing coupled inductor for SST application," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 12528–12539, Nov. 2021, doi: 10.1109/TPEL.2021.3076460.

[35] T. Pereira, Y. Wei, Y. Pascal, H. A. Mantooth, and M. Liserre, "Self-tuning multiport resonant DC/DC converter based on actively-controlled inductors for hybrid storage system integration," *IEEE Trans. Power Electron.*, vol. 38, no. 4, pp. 4787–4804, Apr. 2023, doi: 10.1109/TPEL.2022.3232188.

[36] T. Guillod, D. Rothmund, and J. W. Kolar, "Active magnetizing current splitting ZVS modulation of a 7 kV/400 V DC transformer," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1293–1305, Feb. 2020, doi: 10.1109/TPEL.2019.2918622.

[37] S. Chakraborty and K. Hatua, "Modeling with beat frequency dynamics and phase-frequency control design for a dual-bridge series resonant converter," *IEEE Trans. Ind. Electron.*, vol. 69, no. 8, pp. 7952–7962, Aug. 2022, doi: 10.1109/TIE.2021.3109532.

[38] S. Tian, F. C. Lee, and Q. Li, "A simplified equivalent circuit model of series resonant converter," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3922–3931, May 2016, doi: 10.1109/TPEL.2015.2464351.

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