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Single-Phase Voltage-Doubler High-Power-Factor Ćuk Rectifier Operating in Discontinuous Conduction Mode

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ABSTRACT This article provides a comprehensive analysis, including static, dynamic, and experimental validation, of a voltage-doubler Ćuk rectifier operating in the discontinuous conduction mode (DCM) for single-phase applications. The proposed topology integrates two classic Ćuk rectifiers through a three-position switch, allowing for either a doubled output voltage or reduced voltage efforts compared to the conventional topology. The voltage gain is increased while maintaining the step-up/step-down characteristic of the Ćuk family, and power components are activated only in a half cycle of the electrical grid, thus reducing the current efforts in the semiconductors. These features make the Ćuk converter suitable for higher voltage applications. The proposed topology is analyzed in DCM, where a high power factor is naturally achieved without a current control loop. An experimental prototype of 1 kW is built to verify the theoretical analysis, and the results show an efficiency of 94.68% with an input current total harmonic distortion of 1.86% at a rated power, including an output voltage control loop. Furthermore, the proposed topology is compared to the conventional Ćuk rectifier, both operating in DCM and with power factor correction.

INDEX TERMS Ćuk voltage-doubler rectifier, discontinuous conduction mode (DCM), power factor correction (PFC).

I. INTRODUCTION

The development of technologies for converting ac to dc has been seeing a significant increase on the world stage due to the exponential growth of dc-powered devices, including dc motors, computer power supplies, cell phones, and battery chargers. Given the broad range of applications, various solutions for ac–dc converters (rectifiers) are required. These rectifiers can use passive or active switches, operate at low or high frequencies, and be single phase or three phase. In addition, to meet standards, rectifiers must provide a high power factor in the ac source [1], [2], [3], [4].

The cascade boost converter with a bridge rectifier is a popular choice for single-phase rectifiers with power factor correction (PFC), due to its current source characteristic and simplicity [5], [6]. However, the use of diode bridges in this configuration results in higher conduction losses when operating in discontinuous and critical conduction modes. In addition, input filters are required to reduce the total harmonic distortion (THD) [6], [7].

Recently, several topologies derived from the cascade boost converter with a diode bridge have been proposed in the literature. Among these, the most significant solutions for single-phase rectifiers are the bridgeless [4], [5], [7], [8], [9], [10], [11] and bridgeless totem-pole [12], [13], [14], [15], [16], [17] types. The study proposed in [12] employs an interleaved totem-pole boost bridgeless rectifier to address reduced reverse-recovery issues for PFC. In contrast, the authors in [14] and [15] utilize a totem-pole boost bridgeless rectifier to enhance noise performance. Meanwhile, the authors in [13], [16], and[17] employ an interleaved totem-pole rectifier with

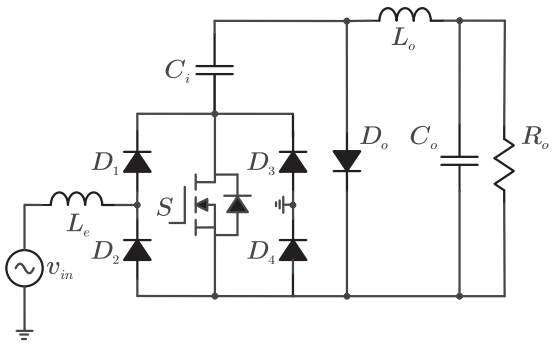

FIGURE 1. Conventional Ćuk rectifier.

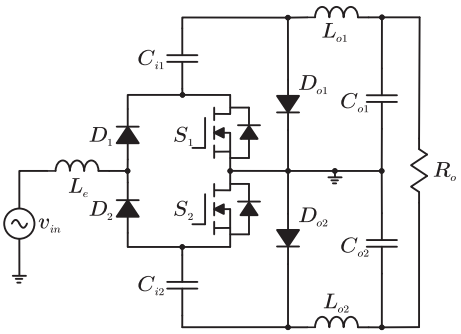

FIGURE 2. Propose voltage-doubler Ćuk rectifier.

zero voltage switching or zero current switching as a means to mitigate problems associated with power losses in semiconductors. These topologies have a lower number of power semiconductors in the current path than the conventional PFC rectifiers, resulting in reduced conduction losses and higher conversion efficiencies.

The concept of voltage-doubler rectifiers was introduced in [18] as a part of the evolution of rectifiers, in which different forms of implementation of the voltage-doubler boost rectifier were proposed. Subsequently, several works applied the concept of voltage doublers to other topologies [4], [8], [19], [20], [21], [22]. The implementation of PFC voltage-doubler rectifiers enables the use of different switching cells that integrate two rectifiers, allowing for the doubling of the output voltage and significantly reducing the voltage stresses on the semiconductors in comparison to the conventional and bridgeless topologies [23], [24], [25], [26]. In addition, Font et al. [25] present nine topologies that can be implemented by the Ćuk rectifier, each with its advantages, disadvantages, efficiency, THD, power factor comparisons, and the best applicable conduction mode for each topology.

Recent studies have shown that the Ćuk rectifier has a broad range of applications, such as in the input stage of power supplies [10], in the use of bridgeless topology for electric vehicle chargers [6], [27], [28], and in applications such as LED lamp drivers [29]. The use of the Ćuk converter as a PFC is mainly due to its interesting structure, which includes constant current sources at the input and output, eliminating the need for an input filter and naturally limiting the inrush current. These features make the topology suitable for single-stage AC-dc battery chargers [30], [31] and LED lamp drivers [32]. To aid in the understanding of the study, the conventional Ćuk rectifier's structure is presented in Fig. 1.

In this study, the voltage-doubler rectifier concept is applied to the classic Ćuk rectifier shown in Fig. 1. The resulting topology is the Ćuk voltage-doubler rectifier, as illustrated in Fig. 2. This topology integrates two conventional Ćuk rectifiers, with each rectifier operating during half of the electrical grid's cycle and adding their voltages at the output.

The proposed voltage-doubler Ćuk rectifier offers additional benefits to the structures based on the Ćuk rectifier. In addition to the step-up/step-down characteristics, constant current input, and the absence of input filter on the discontinuous conduction mode (DCM), it also doubles the output voltage and reduces the stresses on the elements as compared to the conventional Ćuk rectifier.

Comparing the classic Ćuk rectifier in Fig. 1 with the proposed topology shown in Fig. 2, it should be noted that the current path is established using only two power semiconductors instead of three in the former. In addition, the voltage stresses are reduced by half, while the output voltage is doubled for the same duty cycle value.

In this context, this article introduces an extension of the voltage-doubler concept to the Ćuk rectifier. As a result, a novel rectifier is proposed, characterized by a high-power factor, low harmonic distortion rates, reduced voltage stress on the semiconductor, and most importantly, an extended voltage gain. The objective of this article is to conduct static and dynamic analysis of a single-phase voltage-doubler Ćuk rectifier operating in DCM. The rest of this article is organized as follows. Section II introduces the topological states and main waveforms of the rectifier, while Section III covers the global analysis. The control and dynamic models are developed in Section IV, and Section V presents the experimental results. Finally, Section VI concludes this article.

II. SINGLE-PHASE VOLTAGE-DOUBLER PFC ĆUK RECTIFIER

The proposed Ćuk rectifier is a combination of two conventional Ćuk rectifiers using three-position switches, as described in [26]. Each rectifier operates during a half cycle of the electrical grid, and the switches integrate the two structures to supply power to the output capacitors (C_{o1} and C_{o2}). The switches also connect the output capacitors in series, resulting in twice the output voltage of the conventional topology. Although the topology increases the voltage gain, it still maintains the step-up/step-down feature.

Fig. 3 illustrates the topology of the Ćuk voltage-doubler rectifier and highlights the conduction of each rectifier during the positive and negative cycles of the electrical grid.

The switching cell selected for the Ćuk voltage-doubler rectifier consists of two switches and two diodes (S_1, S_2, D_1,

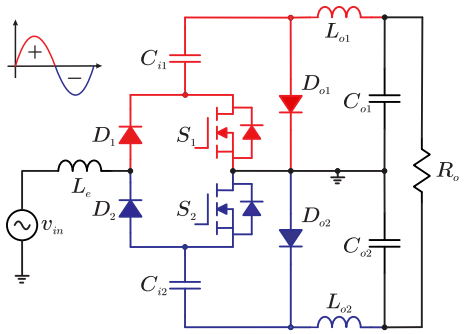

FIGURE 3. Operation of the proposed voltage-doubler Ćuk rectifier for each half cycle of the electrical grid.

and D_2) and is denoted as 2S, as described in [26]. The structure under investigation includes two input capacitors (C_{i1} and C_{i2}), two output inductors (L_{o1} and L_{o2}), and a low-frequency inductor (L_e) that provides current source characteristics to the rectifier. Fig. 3 illustrates this configuration, which depicts the conduction of each rectifier during the positive and negative cycles of the electrical grid.

The proposed voltage-doubler Ćuk rectifier can be operated in all operating modes, however, this article provides an analysis of the operation in DCM. When operating in DCM, the converter is able to emulate a resistance, the sinusoidal input current naturally follows the input voltage, thus the topology does not require a controller for the input current [33], [34], [35]. This behavior emulates that of a resistive load and provides a power factor close to unity. DCM operation of the rectifier during a switching period T_s can be divided into three steps, as shown in Fig. 4 and explained as follows.

A. FIRST STAGE OF OPERATION

Fig. 4(a) illustrates the first topological state, which begins when switch S_1 conducts. At the input, the inductor L_e receives energy from the ac power supply. At the output, the energy from the capacitor C_{i1} is transferred to the inductor L_{o1} and output capacitor C_{o1}, while the diode D_{o1} is reverse biased. During this state, the current in the inductors L_e and L_{o1} increases linearly at a rate proportional to the input voltage v_{in}, as given by

$$\frac{di_{Ln}}{dt} = \frac{v_{\text{in}}}{L_n}, \qquad n = e, o1. \tag{1}$$

Furthermore, based on the analysis of Fig. 4(a), the voltage across capacitor C_{i1} can be expressed as

$$v_{Ci1}(t) = v_{\text{in}}(t) + V_{Co1}, \quad 0 \le t \le \pi. \tag{2}$$

B. SECOND STAGE OF OPERATION

The second topological state, as shown in Fig. 4(b), begins when switch S_1 is turned OFF, and at the same time, the diode D_{o1} starts conducting. As a result, the energy stored in inductors L_e and L_{o1} is transferred to capacitors C_{i1} and C_{o1}, respectively. During this stage, the currents in the inductors

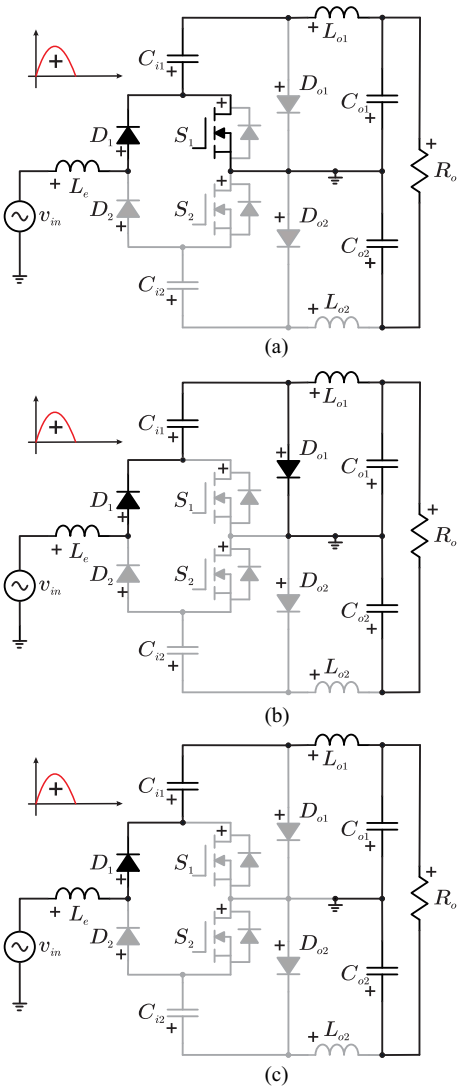

FIGURE 4. Topological states of the voltage-doubler Ćuk rectifier during a switching period T_s for the positive half cycle. (a) S1 switch leading (ΔT_1). (b) S1 switch blocked (ΔT_2). (c) Discontinuous conduction mode (DCM) (ΔT_3).

decrease linearly at a rate proportional to the voltage across C_{o1}, denoted as V_{Co1} as follows:

$$\frac{di_{Ln}}{dt} = \frac{-V_{Co1}}{L_n}, \qquad n = e, o1. \tag{3}$$

At the end of the second topological state, the diode current i_{Do1} becomes zero, and the diode D_{o1} is reverse-biased again. Therefore, the duty cycle of this state can be determined using the following equation:

$$d_2 = 2\alpha d_1 \sin(\omega t) \tag{4}$$

where α is defined as the ratio between the peak value of the input voltage (V_{inp}) and the average value of the output voltage (V_o), while ω represents the angular frequency, and d_1 represents the duty cycle of the switch S_1.

C. THIRD STAGE OF OPERATION

During this operating state, depicted in Fig. 4(c), the currents in the inductors L_e and L_{o1} have the same magnitude but opposite signs, resulting in a zero diode current i_{Do1}, which characterizes the DCM. It should be noted that the currents in the inductors remain constant and nonzero, providing direct current input and high power factor characteristics to the rectifier. At this stage, the capacitors C_{o1} and C_{o2} supply power to the load R_o. Once the duty cycle of the second stage of the operation is defined using (4), the duty cycle of the discontinuity stage (d_3) can be calculated as follows:

$$d_3 = 1 - d_1 - d_2 = 1 - d_1\,(1 - 2\alpha \sin(\omega t))\,. \tag{5}$$

Fig. 5 illustrates the main theoretical waveforms during the three operating stages of a switching period T_s. On the other hand, Fig. 6 shows the waveforms of the input voltage and current, the voltage across the coupling capacitors, the voltage across output capacitors, and the current in the inductors for a mains period.

III. STATIC ANALYSIS OF THE PFC VOLTAGE-DOUBLER ĆUK RECTIFIER

The objective of this section is to calculate the static gain, determine the operating range of the DCM, and derive the equations for the maximum and minimum currents and stresses on power semiconductor devices.

A. VOLTAGE STATIC GAIN

The static voltage gain ($G = V_o/V_{\text{inp}}$) of the Ćuk voltage-doubler rectifier, in terms of the topology parameters, can be determined by calculating the average value of the current in the diode D_{o1} (I_{Do1}) over a half cycle of the electrical grid

$$I_{Do1} = \frac{1}{T}\int_0^T \langle i_{Do1}\rangle\, dt. \tag{6}$$

The average value of the current in the diode D_{o1} during a switching period T_s (as shown in the current waveform in Fig. 5), can be defined as follows:

$$\langle i_{Do1}\rangle = \frac{{V_{\text{inp}}}^2 \sin^2(\omega t) D^2 T_s}{2 L_x V_o} \tag{7}$$

where the value of L_x is given by

$$L_x = \frac{L_e L_{oy}}{L_e + L_{oy}}, \qquad y = 1, 2. \tag{8}$$

Substituting (7) into (6) yields

$$I_{Do1} = \frac{{V_{\text{inp}}}^2 D^2 T_s}{4 L_x V_o}. \tag{9}$$

As the average current in the diode D_{o1} is equal to the average current in the load for one half cycle of the electrical grid, the static gain can be expressed as

$$G = \frac{V_o}{V_{\text{inp}}} = D\sqrt{\frac{R_o}{4 L_x f_s}} \tag{10}$$

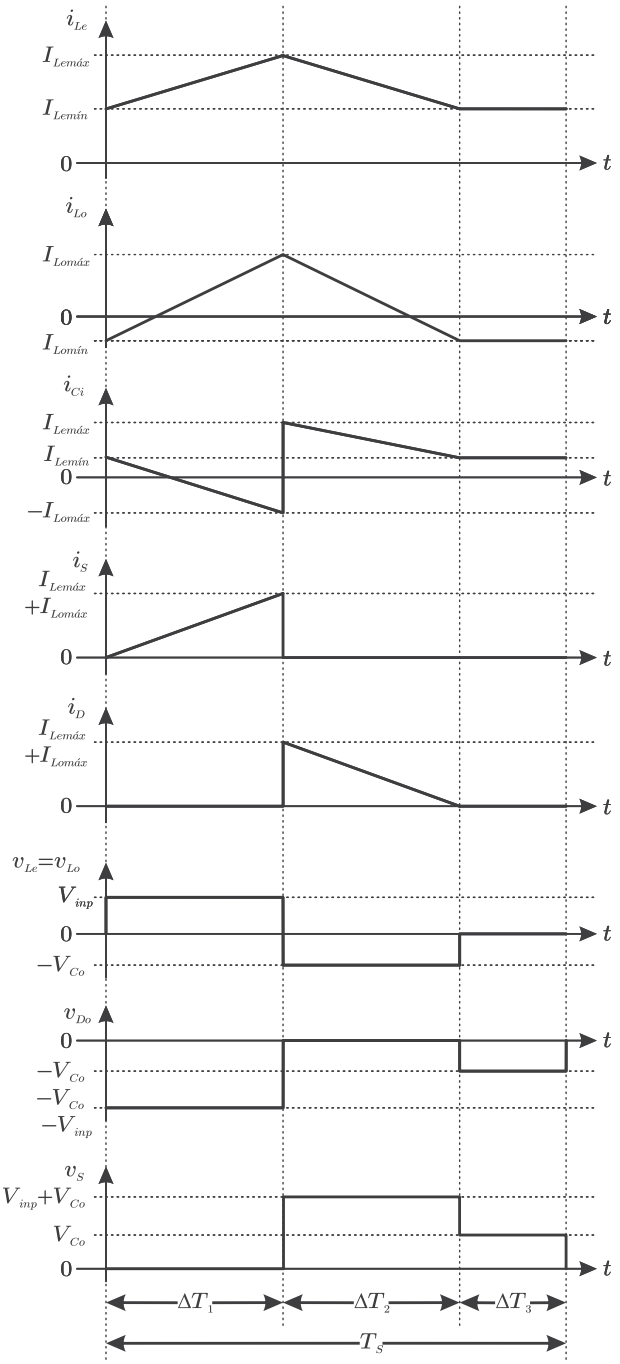

FIGURE 5. Theoretical waveforms of the Ćuk voltage-doubler rectifier for operation in the DCM during a switching period T_s.

where f_s is the switching frequency and R_o is the load resistance.

The gain of the converter, as a feature of the DCM, is dependent on the load and can be confirmed by (10).

B. BOUNDARY BETWEEN CONTINUOUS CONDUCTION MODE (CCM) AND DCM

In order to determine the operating region of the Ćuk voltage-doubler rectifier, it is necessary to define the critical limit for

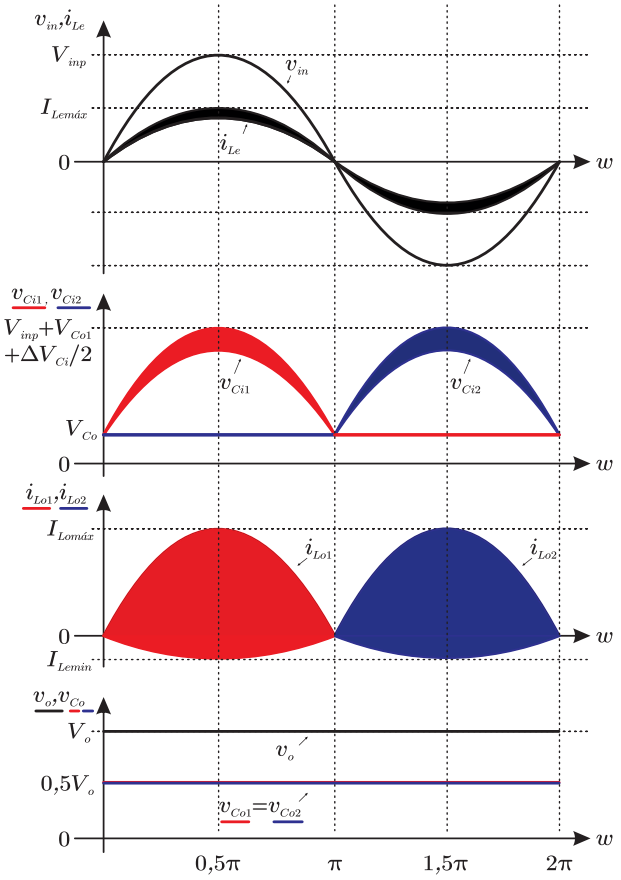

FIGURE 6. Theoretical waveforms of the Ćuk voltage-doubler rectifier for operation in DCM during a switching period *T*.

discontinuous conduction. This critical condition occurs when the static gain of the converter operating in DCM becomes equal to the gain in CCM. The gain in CCM is defined as follows:

$$G_{\text{CCM}} = \frac{V_o}{V_{\text{inp}}} = \frac{D}{1-D}. \tag{11}$$

By (10) and (11), we can obtain the expression for the maximum duty cycle ($D_{\max}$) to ensure DCM operation, which is given by

$$D_{\max} \leq 1 - \sqrt{\frac{4L_x f_s}{R_o}}. \tag{12}$$

Fig. 7 illustrates the static gain of the rectifier for various values of the parameter K_x, as defined by (13), and the duty cycle D. It is observed that for each K_x value, there is a maximum duty cycle value ($D_{\max}$) given by (12), which determines the operation mode of the converter. For duty cycle values greater than $D_{\max}$, the converter operates in CCM, and for values smaller than $D_{\max}$, it operates in DCM.

$$K_x = \sqrt{\frac{R_o(L_e + L_{oy})}{2L_e L_{oy} f_s}}. \tag{13}$$

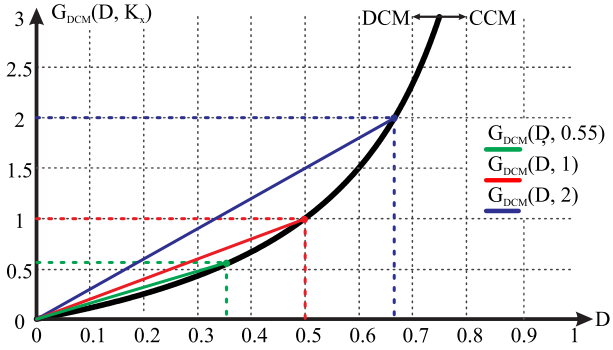

FIGURE 7. Ćuk voltage-doubler rectifier static gain in DCM and operating limit.

C. CALCULATION OF INDUCTANCES

The inductances L_e, L_{o1}, and L_{o2} can be determined by analyzing the waveforms of the equivalent currents in each inductor (as shown in Fig. 5). Therefore, L_e can be dimensioned through a current ripple specification, as follows:

$$L_e = \frac{V_{\text{inp}} D}{\Delta I_{Le} f_s} \tag{14}$$

where ΔI_{Le} is the designed current ripple of the input inductor.

On the other hand, to design the values of inductances L_{o1} and L_{o2}, it is necessary to consider that the average value of the load current is equal to the average value of the current in diode D_{o1}, as previously determined in (9).

$$I_{Do1} = \frac{V_o}{R_o} = \frac{V_{\text{inp}}{}^2 D^2 T_s}{4L_x V_o}. \tag{15}$$

Replacing (8) in (15) and simplifying the resulting expression, the following equation is obtained, which defines the values of L_{o1} and L_{o2}:

$$L_{o1} = L_{o2} = \frac{V_{\text{inp}}{}^2 D^2 L_e R_o}{4V_o{}^2 L_e f_s - V_{\text{inp}}{}^2 D^2 R_o}. \tag{16}$$

In addition, to perform the magnetic design of the inductors, the root-mean-square (rms) currents can be calculated as follows:

$$I_{Le\text{rms}} = \sqrt{\frac{D^3 V_{\text{inp}}{}^2}{72\pi V_o{}^2 L_e{}^2 L_o{}^2 f_s{}^2}\left[D\begin{bmatrix}9\pi L_e V_o{}^2 (L_e + 2L_o)\\ +3L_o{}^2 V_{\text{inp}}\\ (-9\pi V_{\text{inp}} - 32V_o)\\ +4L_o{}^2 V_o (3\pi V_o + 16V_{\text{inp}})\end{bmatrix}\right]} \tag{17}$$

$$I_{Lo\text{rms}} = \sqrt{\frac{D^3 V_{\text{inp}}{}^2}{144\pi V_o{}^2 L_e{}^2 L_o{}^2 f_s{}^2}\left[V_o L_e{}^2\begin{bmatrix}3\pi V_o (4-3D)\\ +32V_{\text{inp}} (2-3D)\end{bmatrix}\right.} \left.\begin{bmatrix}\\ +27\pi D V_{\text{inp}}{}^2 L_o (2L_e + L_o)\end{bmatrix}\right]. \tag{18}$$

D. CALCULATION OF CAPACITANCES

The design process for the output capacitors C_{o1} and C_{o2} involves satisfying the voltage ripple criteria at the frequency of the electrical grid, which can be calculated using (19). In addition, the capacitors must meet the condition for the rms current value.

$$C_{o1} = C_{o2} = \frac{P_o}{2\pi f_r {V_o}^2 \Delta V_{o\%}}. \tag{19}$$

where $\Delta V_{o\%}$ represents the percentage of output voltage ripple, P_o denotes the output power, and f_r the electrical grid frequency.

The waveforms in Fig. 5 can be used to derive the expression for calculating the input capacitors C_{i1} and C_{i2} during the first stage of operation. The equation of the line is applied at the instant when the current crosses zero until it reaches the maximum value

$$\Delta_{\mathrm{TC}} = \frac{I_{Le\min} \mathrm{DT}_s}{I_{Le\min} + I_{Lo\max}}. \tag{20}$$

Once the interval Δ_{TC} is determined, the following expression can be used to calculate the input capacitor as a function of voltage ripple ΔV_{Cix} on its terminals

$$C_{ix} = \frac{1}{\Delta V_{Cix}} \left[\int_{\Delta_{\mathrm{TC}}}^{\mathrm{DT}_s} I_{Le\min} - \frac{I_{Le\min} + I_{Loy\max}}{DT_s} t \right] dt. \tag{21}$$

The maximum and minimum currents in each inductor can be calculated using the following equation:

$$I_{Le\max} = I_{Le\min} + \frac{V_{\mathrm{inp}} \mathrm{DT}_s}{L_e}. \tag{22}$$

$$I_{Loy\max} = -I_{Le\min} + \frac{V_{\mathrm{inp}} \mathrm{DT}_s}{L_{oy}}. \tag{23}$$

The aforementioned equations have three variables ($I_{Le\min}$, $I_{Le\max}$, and $I_{Loy\max}$). To solve for these variables, a third equation is needed. This equation can be obtained by considering that the average value of the current in the input capacitor during the computation period is equal to zero, as shown in the following equation:

$$i_{Cix\mathrm{avg}} = \frac{\left(I_{Le\min} - I_{Loy\max}\right) D}{2} + \frac{\left(I_{Le\max} + I_{Le\min}\right) D_2}{2} + I_{Le\min} D_3 = 0. \tag{24}$$

Solving the linear system consisting (22), (23), and (24), we obtain

$$I_{Le\min} = \frac{D^2 V_{\mathrm{inp}} \left(V_o L_e - 2 V_{\mathrm{inp}} L_{oy}\right)}{2 V_o L_e L_{oy} f_s} \tag{25}$$

$$I_{Le\max} = \frac{D V_{\mathrm{inp}} \left[2 V_o L_{oy} + D \left(V_o L_e - 2 V_{\mathrm{inp}} L_{oy}\right)\right]}{2 V_o L_e L_{oy} f_s} \tag{26}$$

$$I_{Loy\max} = \frac{D V_{\mathrm{inp}} \left[2 V_o L_e - D \left(V_o L_e - 2 V_{\mathrm{inp}} L_{oy}\right)\right]}{2 V_o L_e L_{oy} f_s}. \tag{27}$$

Therefore, substituting (25)–(27) into (21), the expression for the design of input capacitors is given by

$$C_{i1} = C_{i2} = \frac{D^2 V_{\mathrm{inp}} \left[D \left(V_{\mathrm{inp}} L_{oy} - V_o L_e\right) + 2 V_o L_e\right]^2}{8 {V_o}^2 {L_e}^2 L_{oy} \Delta V_{Ci} {f_s}^2}. \tag{28}$$

In addition, the equation for calculating the rms current in the input capacitors is defined as

$$I_{Ci\mathrm{rms}} = \sqrt{\frac{D^3 {V_{\mathrm{inp}}}^2}{144\pi {V_o}^2 {L_e}^2 {L_{oy}}^2 {f_s}^2} \left[L_e V_o \left[\begin{matrix} 3\pi (4 L_e V_o \\ -3 D L_e V_o) \\ +32 D L_{oy} V_{\mathrm{inp}} \end{matrix} \right] + {L_{oy}}^2 V_{\mathrm{inp}} \left(\begin{matrix} 64 V_o \\ -27\pi D V_{\mathrm{inp}} \end{matrix} \right) \right]}. \tag{29}$$

E. STRESS IN SEMICONDUCTORS

The power semiconductors of the rectifier were dimensioned based on their current stress (average and rms values) and voltage (maximum values). The average and rms current values for diodes D_{o1} and D_{o2} are given by

$$I_{Do,\mathrm{avg}} = \frac{{V_{\mathrm{inp}}}^2 D^2}{4 V_o L_x f_s}. \tag{30}$$

and

$$I_{Do,\mathrm{rms}} = \frac{2 D V_{\mathrm{inp}}}{3 L_x f_s} \sqrt{\frac{V_{\mathrm{inp}} D}{V_o \pi}}. \tag{31}$$

In addition, the maximum reverse voltage value across diodes D_{o1} and D_{o2} is given by

$$V_{Do1,\max} = V_{Do2,\max} = V_{\mathrm{inp}} + 0.5 V_o. \tag{32}$$

The maximum current values, rms current, and maximum voltage stresses on switches $S1$ and $S2$ are also determined in the same way as for the diodes

$$I_{S,\mathrm{avg}} = \frac{V_{\mathrm{inp}} D^2}{2\pi L_x f_s} \tag{33}$$

$$I_{S,\mathrm{rms}} = \frac{V_{\mathrm{inp}} D}{2 L_x f_s} \sqrt{\frac{D}{3}} \tag{34}$$

$$V_{S1,\max} = V_{S2,\max} = V_{\mathrm{inp}} + 0.5 V_o. \tag{35}$$

IV. DYNAMIC MODELING AND CONTROL STRATEGY

This section presents the dynamic design-oriented model of the control for Ćuk voltage-doubler rectifier, which provides the model to design the output voltage loop controller.

A. CONTROL STRATEGY

The control system adopted for the Ćuk voltage-doubler rectifier uses pulse width modulation (PWM) with a constant switching frequency. Therefore, the proposed system only requires one compensator to regulate the overall output voltage, as shown in the block diagram of Fig. 8. It is important to note that the topology does not require voltage balance control of the capacitor when the load is only applied at full voltage.

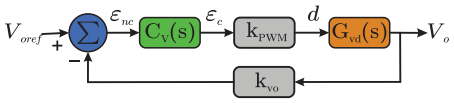

FIGURE 8. Block diagram for output voltage control.

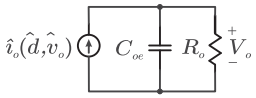

FIGURE 9. Simplified equivalent circuit for controlling the output voltage of the Ćuk voltage-doubler rectifier.

The variables in the block diagram shown in Fig. 8 are as follows: V_{oref} is the output voltage reference, V_o is the output voltage, ϵ_{nc} is the uncompensated error, $C_v(s)$ is the voltage compensator, ϵ_c is the compensated error, k_{PWM} is the PWM modulator gain, and $G_{vd}(s)$ is the converter plant for output voltage control.

B. DYNAMIC MODEL FOR OUTPUT VOLTAGE CONTROL

To design the voltage compensator, it is essential to establish the dynamic model of the output voltage with respect to the duty cycle (G_{vd}) of the rectifier. To analyze the static and dynamic characteristics of the topology, the simplified equivalent electrical circuit shown in Fig. 9 is employed.

The dynamic model of the output voltage as a function of the duty cycle is obtained using the equivalent circuit in Fig. 9, as follows:

$$\hat{i}_o\left(\hat{d},\hat{v}_o\right) = C_{oe}\frac{d\hat{v}_o}{dt} + \frac{\hat{v}_o}{R_o} \tag{36}$$

where C_{oe} is the equivalent output capacitor, it is defined as follows:

$$C_{oe} = \frac{C_{o1}C_{o2}}{C_{o1}+C_{o2}}. \tag{37}$$

According to (36), it is observed that the output current i_o is affected when either the output voltage v_o or duty cycle d is changed. However, it should be noted that v_o is also dependent on d, resulting in a correlation between the variables i_o, v_o, and d, given by

$$\hat{i}_o\left(\hat{d},\hat{v}_o\right) = C_{oe}\frac{d\hat{v}_o}{dt} + \frac{\hat{v}_o}{R_o} = \frac{\partial i_o}{\partial D}\hat{d} + \frac{\partial i_o}{\partial V_o}\hat{v}_o. \tag{38}$$

By differentiating (38) with respect to the average output current presented in (15), we obtain

$$\frac{\partial i_o}{\partial D} = \frac{{V_{inp}}^2 D}{2L_x V_o f_s} \tag{39}$$

$$\frac{\partial i_o}{\partial V_o} = -\frac{{V_{inp}}^2 D^2}{4L_x {V_o}^2 f_s}. \tag{40}$$

Replacing (39) and (40) in (38), it yields

$$\frac{{V_{inp}}^2 D}{2L_x V_o f_s}\hat{d} - \frac{{V_{inp}}^2 D^2}{4L_x {V_o}^2 f_s}\hat{v}_o = C_{oe}\frac{d\hat{v}_o}{dt} + \frac{\hat{v}_o}{R_o}. \tag{41}$$

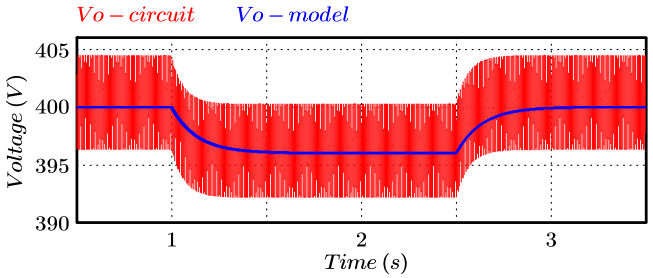

FIGURE 10. Validation of the dynamic control model.

Applying the Laplace transform to (41), and isolating the relationship $\hat{v}_o/\hat{d}$, we obtain

$$G_{vd}(s) = \frac{\hat{v}_o}{\hat{d}} = \frac{2\alpha^2 D V_o R_o}{4sC_o R_o L_x f_s + \alpha^2 D^2 R_o + 4L_x f_s}. \tag{42}$$

C. DYNAMIC MODEL VALIDATION

The small-signal model for controlling the output voltage of the Ćuk voltage-doubler rectifier was validated through numerical simulations using the software PSIM. The transfer function (42) and the switched circuit were simulated simultaneously, and the response of the output voltage is shown in Fig. 10.

To validate the transfer function, a disturbance of 2% was applied to the rectifier's duty cycle value at $t = 1$ s. At $t = 2.5$ s, the duty cycle was increased by 2%, returning to the original operating point. It was observed that the model presented in Fig. 10 (V_o-model) adequately represents the behavior of the switched circuit (V_o-circuit). The ripple observed in the V_o-circuit variable was due to the switching frequency, which was not taken into account in the model.

D. CONTROLLER DESIGN

The chosen control structure aims to achieve zero steady-state error for a step input (generated by an integral term), reject noise and disturbances (handled by a proportional term that enables adjustment of the cut-off frequency), and allow for a phase variation of 0° to 90°. To complete these requirements, a proportional-integral compensator was selected, which is represented by the transfer function

$$C(s) = \frac{k_c\,(s+\omega_z)}{s}. \tag{43}$$

The avoid compensating for the ripple existing in the output voltage at the electrical grid frequency, the voltage loop crossover frequency of the single-phase voltage-doubler rectifier should be set a decade below the grid frequency. Therefore, a design criterion of a cutoff frequency of 6 Hz and a phase margin of 60° was chosen for the compensated open-loop transfer function. This resulted in the calculated values of k_c and ω_z being 0.000510 e 47.69 rad/s, respectively.

To verify the robustness of the designed controller, the frequency response of the compensated system is presented in Fig. 11. The blue line in Fig. 11 represents the frequency

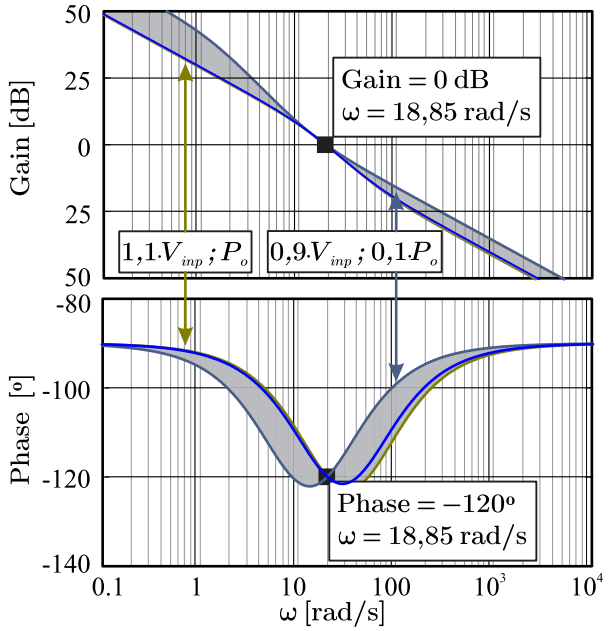

FIGURE 11. Frequency response of the compensated system.

TABLE 1. Prototype Design Specifications

Specification	Value
Output power (P_o)	1000 W
RMS input voltage (V_{in})	220 V
Output voltage (V_o)	400 V
Electrical grid frequency (f_r)	60 Hz
Switching frequency (f_s)	50 kHz
Maximum duty cycle ($D_{\max}$)	0.35
Output voltage ripple ($\Delta_{Vo\%}$)	1%
Voltage ripple in input capacitors ($\Delta_{VCi\%}$)	20%
Input current ripple (Δ_{Le})	10%

response of the system operating under nominal conditions as specified in Table 1. To analyze the robustness of the controller against parametric variations, the system was subjected to a 10% input voltage variation and a load variation ranging from 10% to 100%. The shaded areas in Fig. 11 represent the variation range of the magnitude and phase of the compensated system under these variations. The critical operation of the converter, where the output power was at 10% of the rated power and input voltage at 90% of the rated voltage, was also analyzed, and it was found that the converter remained stable. It is worth noting that the crossover frequency and phase margin of the compensated system remained unchanged under these variations, ensuring the stability of the system and the robustness of the designed controller.

A closed-loop simulation under positive and negative load steps (1000 to 500 W and vice versa) is shown in Fig. 12. The control system achieved a steady state in about 27 cycles of the electrical grid, with a maximum overshoot of 60 V. The result verifies that the proposed converter may be designed to operate in a closed loop using the dynamic model from 42, the controller shown 43, and the controller design method proposed in Section IV-D.

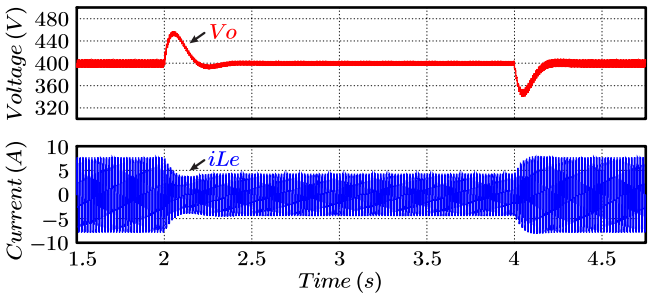

FIGURE 12. Validation of the control model with dynamic response to load steps.

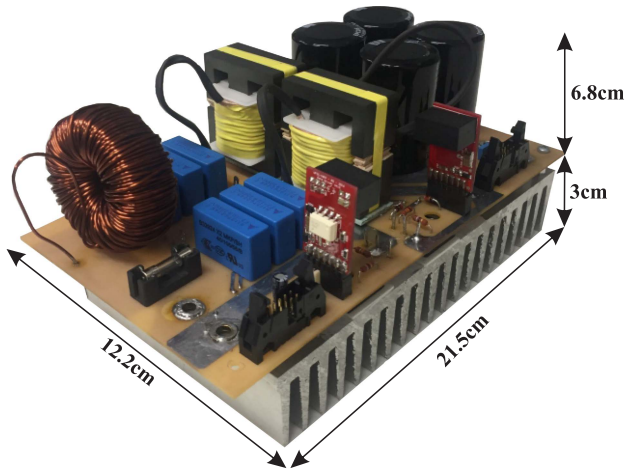

FIGURE 13. Implemented prototype of the proposed Ćuk voltage-doubler rectifier with a power density of 523 W/kg.

TABLE 2. Commercial Components Used in the Prototype of the Proposed Rectifier

Component	Description
Input inductor	3.388 mH, Core: AmoFlux 0088439A7 N° of turns: 156, Wire: 1x17 AWG
Output inductors	60.34 μH, Core: EE 42/20 N° of turns: 26, Wire: Litz 32x32 AWG
Input capacitors	3 x 1 μF/600 V
Output capacitors	4 x 1000 μF/250 V
MOSFETs switches	SCT2120AF, 29 A/650 V
Bridge diodes	MUR860, 8 A/600 V
Output diodes	C3D10060A, 14.5 A/600 V

V. EXPERIMENTAL VALIDATION

The experimental results presented in this section verify the proposed topology of the Ćuk voltage-doubler rectifier and validate the analysis presented in this study. In addition to validating the proposed Ćuk converter, topology comparisons were also made with the conventional Ćuk rectifier. The prototypes were designed using the equations outlined in Section III for sizing the energy storage elements and semiconductors.

Figs. 13 and 14 display photographs of the prototypes. Table 1 enumerates the specifications of the project, whereas

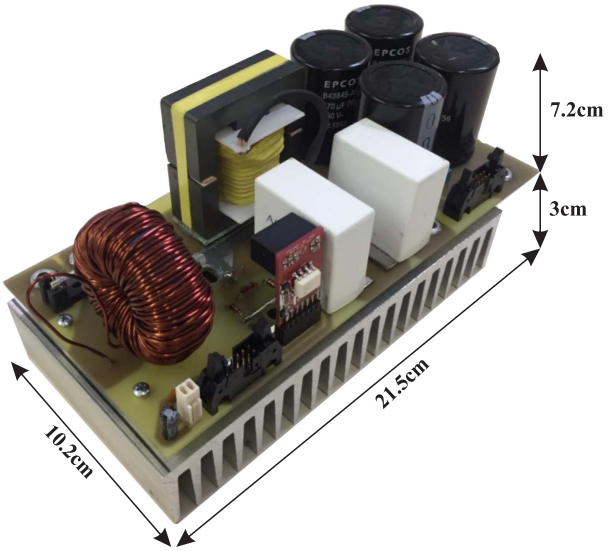

FIGURE 14. Implemented prototype of the conventional Ćuk rectifier with power density of 578 W/kg.

TABLE 3. Commercial Components Used in the Conventional Rectifier Prototype

Component	Description
Input inductor	3.388 mH, Core: AmoFlux 0088439A7 N° of turns: 156, Wire: 1x17 AWG
Output inductors	60.34 μH, Core: EE 55/21 N° of turns: 21, Wire: Litz 150x38 AWG
Input capacitors	2 x 1 μF/600 V
Output capacitors	4 x 470 μF/450 V
Switches	C3M0075120K, 30 A/1200 V
Bridge diodes	C4D05120A, 5 A/1200 V
Output diodes	C2D05120A, 8.5 A/1200 V

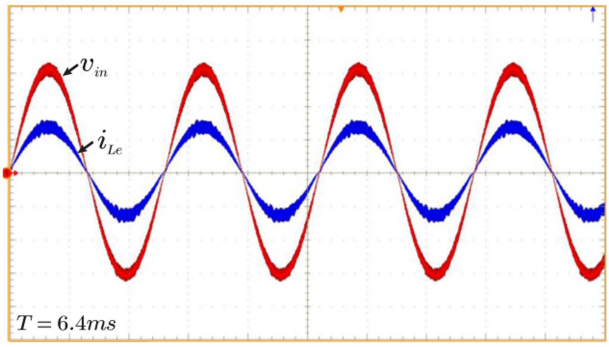

FIGURE 15. Input voltage (100 V/div) and input current (5 A/div) of the proposed Ćuk voltage-doubler rectifier for rated power of 1 kW.

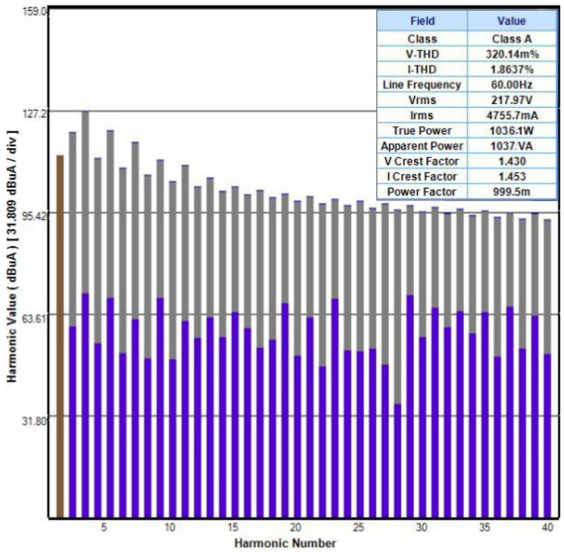

FIGURE 16. Comparison of current amplitude in harmonic order with the IEC61000-3-2 standard. The result was obtained with DPO 5054B oscilloscope.

Tables 2 and 3 present the commercial components chosen from the project methodology.

The rectifiers were digitally controlled using the DSP TMS320F28377 from Texas Instruments, which was directly coupled with a signal conditioning and drive board.

The DSP was utilized for the digital control of both the conventional and voltage-doubler rectifier, as they both employ a single PWM output. The switches of the voltage-doubler rectifier are triggered with the same command pulse since each switch conducts only half a cycle of the electrical grid and remains inactive during the other half. Furthermore, the voltage-doubler rectifier permits operation with two distinct loads, whereby the loads are connected in parallel to the output capacitors C_{o1} and C_{o2}. Nonetheless, to apply this strategy, it is imperative to integrate a control loop that equalizes the voltage on each capacitor, an aspect that was not addressed in this study.

The ac source Agilent 6813B was utilized to generate an input alternating voltage with low THD for the experimental tests. The results presented as follows were obtained using MOSFET technology switches. The first experimental test conducted involves the converter operating at rated power (1 kW). The input voltage (v_{in}) and the current in the input inductor L_e (i_{Le}) for this situation can be seen in Fig. 15. The current presents a sinusoidal shape and is in phase with the input voltage, with a THD of 1.86% and a power factor of 0.9995, considering a voltage THD of 0.320%. The harmonic spectrum of the current was compared to the values established by the IEC61000-3-2 standard in Fig. 16. It can be observed that the harmonic components of the input current are significantly lower than the limits set by the standard.

Fig. 17 shows the output voltage (V_o) and output current (I_o) during operation at the rated power. The output voltage is stable at 400 V, while the output current is at the expected value of 2.5 A, confirming the proper functioning of the rectifier. This test was conducted with the voltage control system activated, thereby validating the closed-loop operation of the rectifier under steady-state conditions.

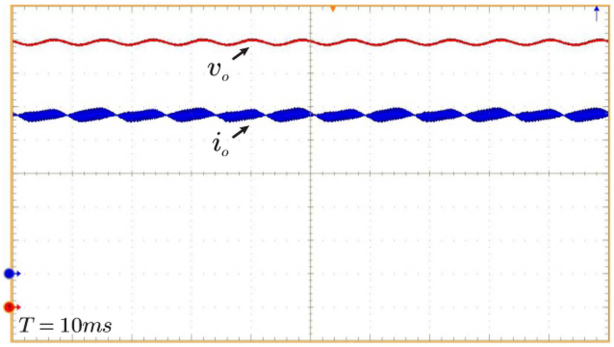

FIGURE 17. Output voltage (50 V/div) and output current (500 mA/div) of the proposed voltage-doubler Ćuk rectifier.

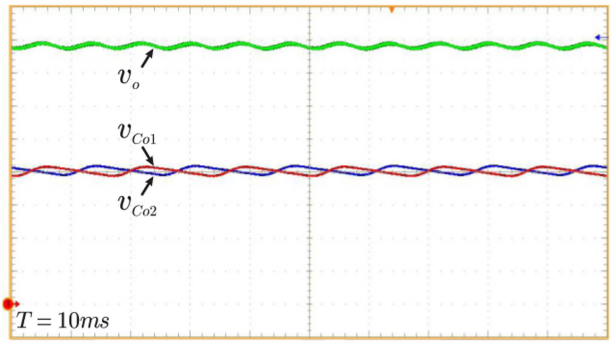

FIGURE 18. Output voltage V_o (50 V/div) and voltage across capacitors C_{o1} and C_{o2} (50 V/div) of the proposed Ćuk voltage-doubler rectifier.

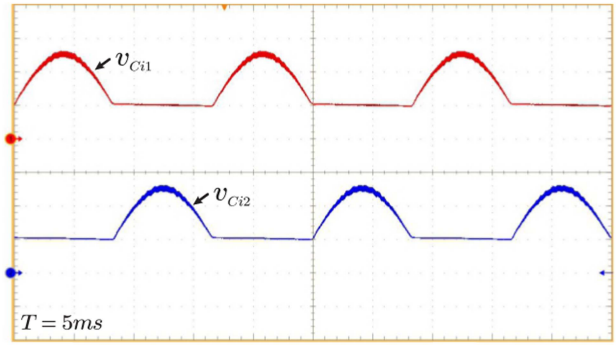

FIGURE 19. Voltage across coupling capacitors C_{i1} and C_{i2} (200 V/div) of the proposed voltage-doubler Ćuk rectifier.

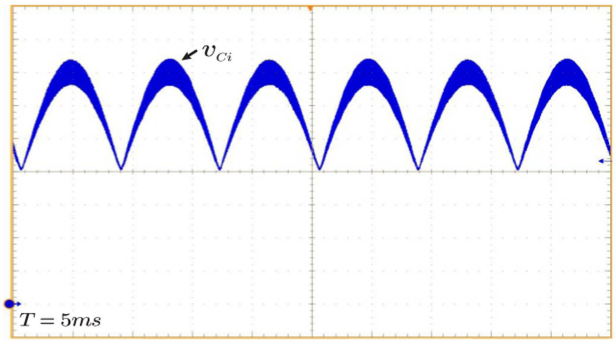

FIGURE 20. Voltage across the input capacitor C_i (200 V/div) of a conventional Ćuk rectifier with the same specifications.

Fig. 18 shows that the voltage of the output capacitors, C_{o1} and C_{o2}, is half of the output voltage ($V_o/2$). The equilibrium of voltage across the capacitors relies on the structural parameters of the converter. Disparities in impedances between the two converters can lead to an imbalance in the voltage across capacitors C_{o1} and C_{o2}. Balanced voltage in the capacitors can be achieved reliably through the implementation of a control loop for voltage balance in capacitors. This allows the converter to supply different loads with the equilibrated voltage, enhancing the topology's versatility by offering a capacity of functionality with two output voltage levels. The voltage ripple frequency across the capacitors is 60 Hz, while the output voltage V_o has a frequency of 120 Hz.

Fig. 19 displays the voltages across the input capacitors C_{i1} and C_{i2} of the proposed rectifier, where each capacitor conducts for one half-cycle of the input voltage. The voltages across the capacitors consist of an average value, one component at low frequency (60 Hz) and another component at switching frequency (50 kHz). The waveforms agree with the theoretical study presented in Fig. 6, and the maximum voltage across the capacitors is 522.5 V. For comparison purposes, Fig. 20 shows the voltage waveform on the coupling capacitors of the conventional Ćuk rectifier with the same specifications, where the maximum voltage across the capacitor is 737 V. It is observed that the proposed topology provides lower stresses on this component.

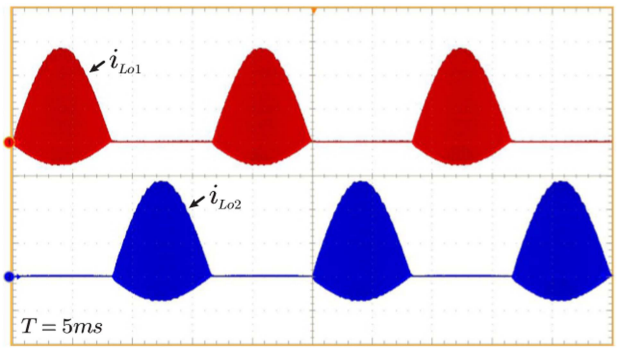

FIGURE 21. Current in the inductors L_{o1} and L_{o2} (10 A/div) of the proposed voltage-doubler Ćuk rectifier.

The current waveforms through the output inductors L_{o1} and L_{o2} are illustrated in Fig. 21, also for rated power. As each inductor conducts during half cycle of the input voltage, the currents are complementary, as predicted by the theoretical analysis. The waveforms in Fig. 21 reveal that the current in the output inductors has two components, one at the mains frequency (60 Hz) and the other at the switching frequency (50 kHz). The maximum, minimum, and rms values of the currents in the output inductors are 28.520, −6.846, and 7.705 A, respectively, which is consistent with the equation derived in Section III.

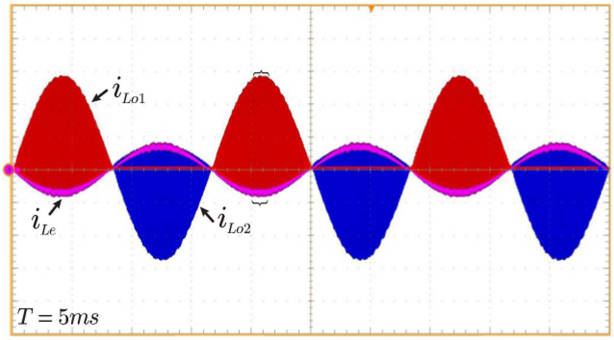

FIGURE 22. Current in the input inductor L_e (10 A/div) and in the output inductors L_{o1} and L_{o2} (10 A/div) of the proposed voltage-doubler Ćuk.

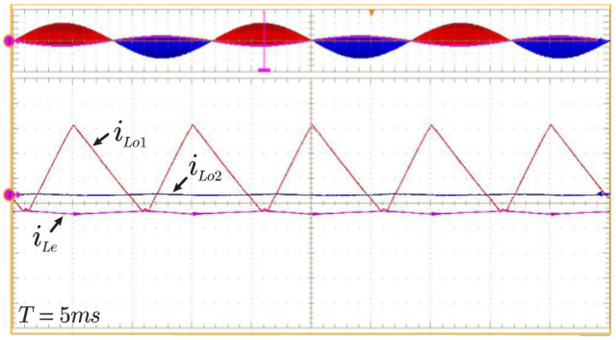

FIGURE 23. Highlight of the current in the input inductor L_e (10 A/div) and in the output inductors L_{o1} and L_{o2} (10 A/div) of the Ćuk voltage-doubler rectifier.

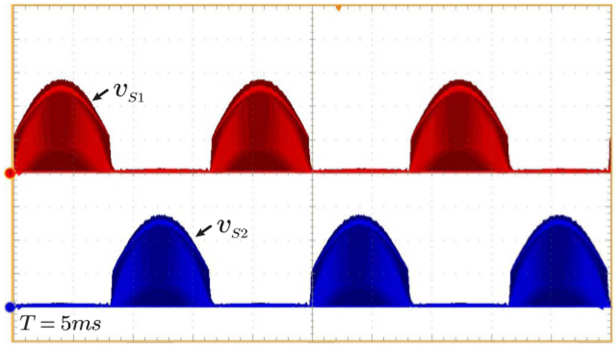

FIGURE 24. Voltage at switches S_1 and S_2 of the proposed Ćuk voltage-doubler rectifier.

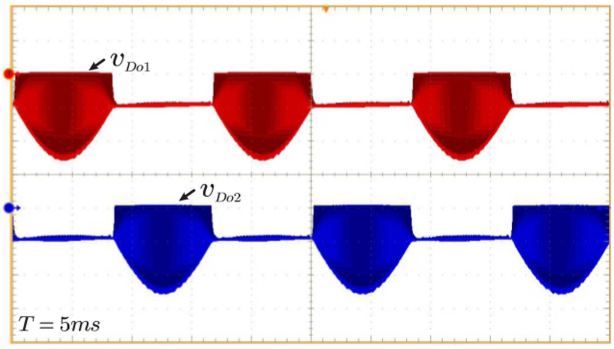

FIGURE 25. Voltage on the diodes D_{o1} and D_{o2} of the proposed voltage-doubler Ćuk rectifier.

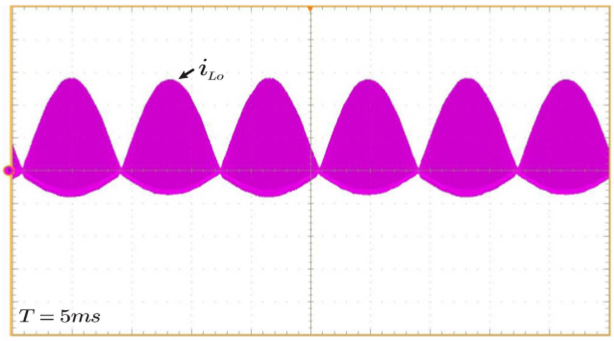

FIGURE 26. Current in the L_o inductor (10 A/div) of the conventional Ćuk rectifier.

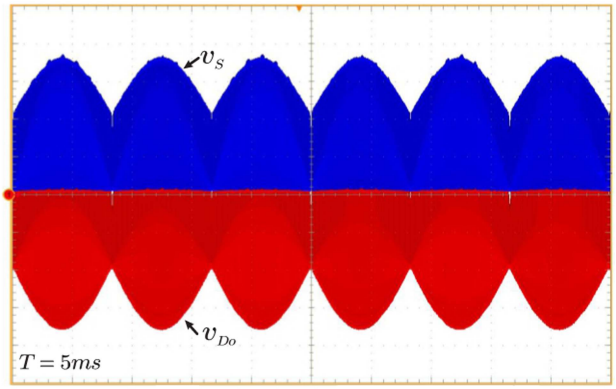

FIGURE 27. Voltages on switch S (200 V/div) and diode D_o (200 V/div) of the conventional Ćuk rectifier with the same specifications as the proposed.

As explained in Section III and depicted in Fig. 4, the DCM is characterized by the condition in which the current flowing through the inductors L_{o1} and L_{o2} is equal to the current in inductor L_e. In the positive cycle, when the current in inductor L_{o1} equals the current in the inductor L_e, the current in the diode D_{o1} becomes zero, and the diode becomes blocked. Therefore, Fig. 22 shows the current waveforms for the inductors, while Fig. 23 zooms in on the stage of discontinuity.

Figs. 24 and 25 depict the voltages waveforms across the switches (S_1 and S_2) and output diodes (D_{o1} and D_{o2}), respectively. One significant advantage of the proposed Ćuk rectifier over the conventional one is the lower voltage stresses on the semiconductors, even when they produce the same output voltage. The same holds for the current flowing through the output inductor L_o, which operates throughout the complete cycle, as shown in Fig. 26.

In Figs. 24 and 25, it is observed that the maximum voltage values across the switches and output diodes, respectively, are equal to 558.3 and 519.2 V. In comparison, Fig. 27 shows the waveforms of voltages across the switch and output diode of a

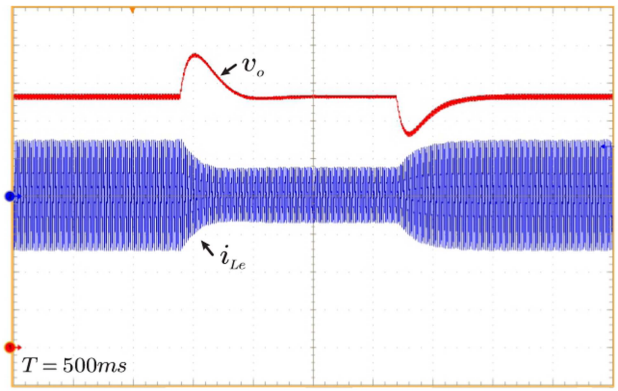

FIGURE 28. Dynamic response to the load steps of the proposed voltage-doubler Ćuk rectifier: V_o (60 V/div) and i_{Le} (5 A/div).

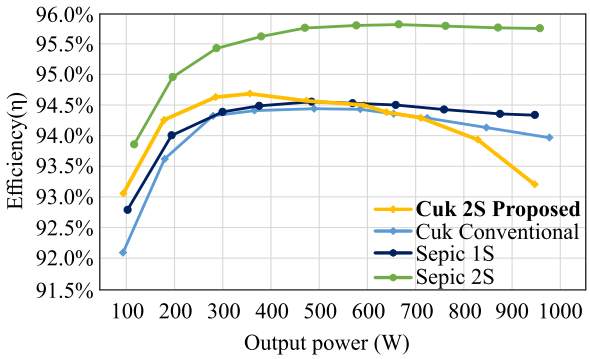

FIGURE 29. Efficiency curves.

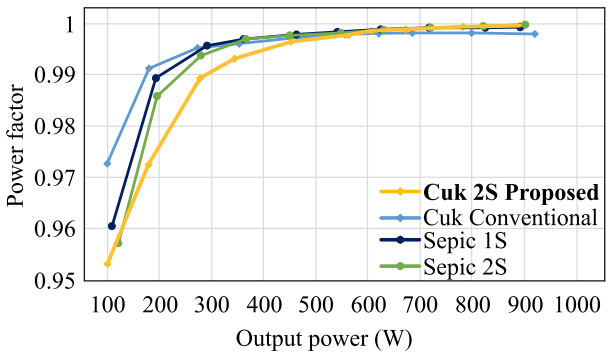

FIGURE 30. Power factor curves.

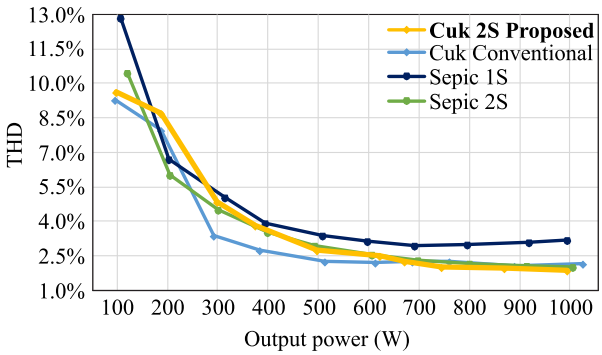

FIGURE 31. THD curves of the input current.

TABLE 4. Efficiency Comparison (η), Power Factor (PF), and THD of the Ćuk Voltage-Doubler Rectifier

Rectifier	η	PF	THD
Ćuk proposed	93.53%	0.9966	1.86%
Ćuk conventional	93.97%	0.9979	2.14%
SEPIC 1S	94.33%	0.9992	3.20%
SEPIC 2S	95.75%	0.9997	2.02%

TABLE 5. Comparison of Experimental Voltage Stresses in the Ćuk Voltage-Doubler Rectifier and the Conventional ćuk Rectifier

Rectifier	V_{Smax}	V_{Domax}	V_{Co}	i_{LoRMS}
Ćuk conventional	702 V	725 V	400 V	9.3 A
Ćuk proposed	558 V	519 V	202 V	7.0 A
SEPIC 2S	543 V	557 V	202 V	7.2 A

TABLE 6. Validation of the Equations in Theoretical, Simulation, and Experimental in the Ćuk Voltage-Doubler Rectifier

Variable	Theoretical	Simulation	Experimental	Error(%)
I_{Lerms}	4.853 A	5.166 A	4.926 A	1.5
I_{Lo1rms}	7.245 A	7.266 A	7.253 A	0.1
I_{Lo2rms}	7.245 A	7.266 A	7.250 A	0.06
I_{Lemin}	7.141 A	7.143 A	6.846 A	4.13
I_{Lemax}	7.784 A	7.766 A	7.705 A	1.01
I_{Lomax}	29.949 A	28.326 A	28.520 A	4.77
I_{Cirms}	5.309 A	5.445 A	-	2.56
I_{Doavg}	2.500 A	2.590 A	-	3.60
I_{Dorms}	8.209 A	8.030 A	-	2.18
I_{Savg}	2.046 A	1.835 A	-	10.31
I_{Srms}	6.273 A	5.777 A	-	7.90
V_{D1max}	-511 V	-527 V	-558 V	8.42
V_{Domax}	-511 V	-521 V	-519 V	1.54
V_{Smax}	511 V	521 V	558 V	8.42

conventional Ćuk rectifier, whose maximum voltage is equal to 741 and 719.2 V, respectively. These results confirm the high voltage stress in the conventional Ćuk rectifier and highlight the reduction of these stresses in the proposed structure.

The simulation results of the dynamic behavior of the Ćuk rectifier were verified with positive and negative load steps (see Fig. 12), and the experimental results of the dynamic behavior were carried out under the same conditions. Small-signal analysis characterizes the system's behavior around an already established operating point. The steady-state model determines the operating point, while small-signal analysis controls the system's dynamic response near that point . The dynamic experimental result is shown in Fig. 28, confirming that (42) and Fig. 12 validate the dynamic model presented in Fig. 10. The control system achieved a steady state in about 27 cycles of the electrical grid, with a maximum overshoot of 60 V.

Using a Yokogawa WT500 power analyzer, efficiency, power factor, and THD of the input current were measured at various output power, as shown in Figs. 29–31. It is important to note that the results are compared to those of the conventional Ćuk rectifier, as well as to the proposed Ćuk rectifier,

TABLE 7. Qualitative and Quantitative Analysis of the Ćuk Voltage Doubler, Ćuk Bridgeless, Ćuk Conventional, SEPIC Voltage Doubler, Conventional SEPIC, Boost CCM and Boost DCM Rectifiers

	Ćuk voltage-doubler	Ćuk bridgeless	Ćuk conventional	SEPIC voltage-doubler	SEPIC conventional	Boost CCM	Boost DCM
G	$\sqrt{\frac{{D_1}^2 R_o}{4L_x f_s}}$	$\sqrt{\frac{{D_1}^2 R_o}{4L_e f_s}}$	$\sqrt{\frac{{D_1}^2 R_o}{4L_e f_s}}$	$\sqrt{\frac{{D_1}^2 R_o}{4L_x f_s}}$	$\sqrt{\frac{{D_1}^2 R_o}{4L_e f_s}}$	$\frac{1}{1-D}$	$1+\frac{V_p D^2}{2f_s L I_o}$
V_{Smax}	$0.5V_o + V_{ac}$	$V_o + V_{ac}$	$V_o + V_{ac}$	$0.5V_o + V_{ac}$	$V_o + V_{ac}$	V_o	V_o
V_{Dmax}	$0.5V_o + V_{ac}$	$V_o + V_{ac}$	$V_o + V_{ac}$	$0.5V_o + V_{ac}$	$V_o + V_{ac}$	V_o	V_o
I_{Savg}	$\frac{V_p {D_1}^2}{2\pi L_x f_s}$	$\frac{V_p {D_1}^2}{2L_e \pi f_s}$	$\frac{V_p {D_1}^2}{L_e \pi f_s}$	$\frac{V_p {D_1}^2}{2\pi L_x f_s}$	$\frac{V_p {D_1}^2}{2L_e \pi f_s}$	$I_o \frac{(4-\pi\alpha)}{\pi\alpha}$	$\frac{1}{\pi}\frac{V_p D^2}{f_s L}$
I_{Srms}	$\frac{V_p D_1}{2L_x f_s}\sqrt{\frac{D_1}{3}}$	$\frac{V_p D_1}{2L_e f_s}\sqrt{\frac{D_1}{3}}$	$\frac{V_p D_1}{L_e f_s}\sqrt{\frac{D_1}{3}}$	$\frac{V_p D_1}{2L_x f_s}\sqrt{\frac{D_1}{3}}$	$\frac{V_p D_1}{2L_e f_s}\sqrt{\frac{D_1}{3}}$	$\frac{2I_o}{\alpha}\sqrt{\frac{3\pi-8\alpha}{6\pi}}$	$\frac{V_p}{f_s L}\sqrt{\frac{D^3}{6}}$
I_{Doavg}	$\frac{{V_p}^2 {D_1}^2}{4V_o L_x f_s}$	$\frac{{V_p}^2 {D_1}^2}{4L_e V_o f_s}$	$\frac{{V_p}^2 {D_1}^2}{4L_e V_o f_s}$	$\frac{{V_p}^2 {D_1}^2}{4V_o L_x f_s}$	$\frac{{V_p}^2 {D_1}^2}{4L_e V_o f_s}$	I_o	$\frac{1}{\pi}\frac{V_p D^2}{2f_s L}Y_1(\alpha)$
I_{Dorms}	$\frac{2V_p D_1}{3L_x f_s}\sqrt{\frac{V_p D_1}{V_o \pi}}$	$\frac{2V_p D_1}{3L_e f_s}\sqrt{\frac{V_p D_1}{V_o \pi}}$	$\frac{{V_p}^2 {D_1}^2}{L_e V_o f_s}\sqrt{\frac{3}{8}}$	$\frac{2V_p D_1}{3L_x f_s}\sqrt{\frac{V_p D_1}{V_o \pi}}$	$\frac{2V_p D_1}{3L_e f_s}\sqrt{\frac{V_p D_1}{V_o \pi}}$	$4I_o\sqrt{\frac{1}{3\pi\alpha}}$	$\frac{V_p}{f_s L}\sqrt{\frac{D^3}{3\pi}Y_2(\alpha)}$
Input	Current	Current	Current	Current	Current	Current	Current
Output	Current	Current	Current	Voltage	Voltage	Voltage	Voltage
Step-up	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Step-down	Yes	Yes	Yes	Yes	Yes	No	No
Input current sensor	No	No	No	No	No	Yes	No
Input voltage sensor	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Current sensor	0	0	0	0	0	1	0
Voltage sensor	1	1	1	1	1	1	1
Number of switches	2	2	1	2	2	1	1
Number of fast diodes	2	1	1	2	1	1	1
Number of standard diodes	2	2	4	2	2	4	4
Number of inductors	3	3	2	3	3	1	1
Number of capacitors	4	3	2	4	3	1	1

and the SEPIC rectifiers proposed by [19] with one switch (SEPIC 1S) and two switches (SEPIC 2S).

Table 4 summarizes the results obtained for efficiency, power factor, and THD of the input current at full load. The rectifier met the THD limits established by the IEC61000-3-2 standard in both tests and achieved a power factor close to unity. During the experimental tests, the thermal analyses were performed, and it was found that the maximum temperature on the semiconductors and inductors did not exceed 60 °C.

Furthermore, Table 5 analyzes the reduction in voltage and current stresses on the components of the proposed Ćuk rectifier compared to the conventional Ćuk. Table 6 presents the theoretical, simulation, and experimental results for all derived equations of the proposed converter. This table is designed to validate the mathematical modeling, simulations, and experimental tests. It showcases the errors between the obtained results to validate their accuracy. The current in the capacitors, switches, and diodes was not derived from the experimental results due to the stray inductance issues that the circuit's layout would introduce.

To highlight the advantages of the proposed rectifier, Table 7 presents a qualitative analysis of the proposed rectifier, the Ćuk conventional rectifier, the Ćuk bridgeless rectifier, the SEPIC voltage-doubler rectifier, the SEPIC conventional rectifier, the Boost CCM conventional rectifier, and the Boost DCM conventional rectifier. Table 7 also presents a quantitative comparison regarding the number of components. The proposed rectifier includes an extra inductor and two additional capacitors compared to the conventional topologies of Ćuk and SEPIC, on the other hand, it offers double the gain and reduces voltage stress by half compared to the conventional. Conversely, the conventional Ćuk and SEPIC topologies, as well as the Boost CCM and DCM, feature additional diodes. In comparison to the bridgeless topologies, the proposed rectifier employs an additional capacitor and a fast diode.

A study was conducted to analyze the distribution of theoretical losses in the voltage-doubler rectifier with the use of MOSFETs, emphasizing its efficiency. Fig. 32 presents the results, which indicate that the majority of the losses are concentrated on the switches. This is due to the current peaks

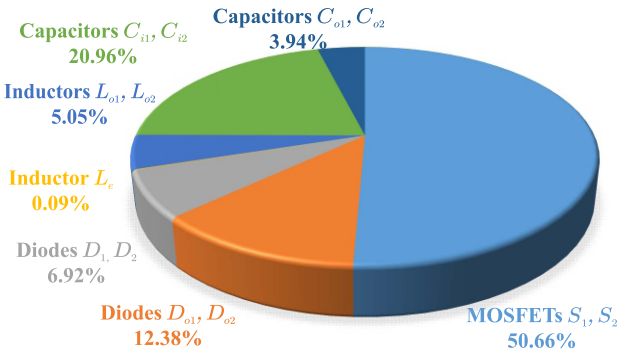

FIGURE 32. Rectifier loss distribution.

that occur during the discontinuity period. The equations employed for calculating conduction and switching losses are derived from [36] and [37], with necessary adjustments made to suit this topology. The percentage division of conduction and switching losses of semiconductors in MOSFETs are: switching losses (P_{swiS}): 19% and conduction losses (P_{conS}): 81%; in Diodes is: switching losses (P_{swiD}): 28% and conduction losses (P_{conD}): 72%.

The advantage of using a voltage doubler is the step-up without the stress of the switches like a conventional topology. The biggest advantages are correlated with the reduction of current and voltage stress on components according to the increase in voltage. Furthermore, the basic topologies (buck and boost) are capable of operating only as, step-down or step-up, respectively. The proposed topology has the possibility of operating as a step-down and/or step-up. In addition to the possibility of operating with different loads connected to each of the output capacitors, as well as feeding a third load in the total bus.

Another significant advantage over the SEPIC converter is directly related to the output configuration. In the SEPIC converter, the output is predominantly voltage based, whereas in the Ćuk converter, the output has an inductor, which reduces the current ripple. This characteristic makes the Ćuk converter particularly suitable for certain applications, offering unique benefits compared to the SEPIC topology, which has only a capacitor in the output. Furthermore, the Ćuk converter's inherent capability to predominantly deliver a current output makes it well suited for various applications, including battery charging and water electrolysis for hydrogen generation. In addition, the presence of the output inductor facilitates the parallel connection of multiple modules.

VI. CONCLUSION

This article discusses the validation of a single-phase Ćuk voltage-doubler PFC rectifier in DCM. The rectifier is based on the switching cell proposed by Costa et al. [19], and this study provides a detailed analysis of its operation, including static and dynamic modeling. In addition, the article presents experimental results that validate the theoretical analysis. To the best of our knowledge, this is the first study that provides a comprehensive analysis and experimental validation of this topology. Thus, the contributions of this article include the derivation of design equations and experimental validation.

The proposed Ćuk voltage-doubler rectifier was implemented using MOSFET switch technology. The experimental results obtained from the 1-kW prototype operating in DCM were consistent with the theoretical analysis. In DCM, the converter can emulate a resistance, and the input current naturally follows the input voltage shape. The input drain current exhibited excellent quality with THD values less than 2% (considering a voltage THD of 0.32%) at rated power and harmonic content levels below those established by the IEC61000-3-2 standard. The rectifier had a peak efficiency of 94.69% and a power factor close to unity.

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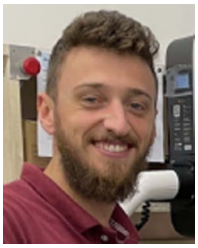

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