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# Developed AC/DC/AC Converter Structure Based on Shunt Active Filter and Advanced Modulation Approach for Asymmetrical Cascade H-Bridge Multilevel Inverters

**NABIL KARANIA [1,2] (Member, IEEE), MOHAMAD ALAAEDDIN ALALI [2] (Member, IEEE), STEFANO DI GENNARO [1] (Member, IEEE), AND JEAN-PIERRE BARBOT [3] (Member, IEEE)**

[1]Department of Information Engineering, Computer Science and Mathematics, and Center of Excellence DEWS, University of L'Aquila, 67100 L'Aquila, Italy
[2]QUARTZ Laboratory, EA 7393, ENSEA, 95014 Cergy-Pontoise, France
[3]LS2N-UMR 6004-CNRS, 44300 Nantes, France

CORRESPONDING AUTHOR: NABIL KARANIA (e-mail: nabil.karania@graduate.univaq.it)

**ABSTRACT** This article presents a free-harmonic ac/dc/ac converter structure using a novel modulation approach for asymmetrical cascade H-bridge multilevel inverter and, conventional rectifiers combined with a shunt active filter, for grid integration. The novel approach SMT-SHE combines two modulation techniques: the staircase modulation technique (SMT); and the selective harmonics elimination (SHE). SMT-SHE approach achieves a sinusoidal-like output stepping voltage with variable output voltage amplitude and free of wideband or/and specific harmonics to fulfill the sensitive loads' specifications; by determining the appropriate SHE switching angles. The precalculated switching angles are optimized to minimize the number of H-bridge modules and lower the dc capacitor rating. Furthermore, a restriction on the switching angles is proposed to prevent the appearance of undesired harmonics (zeros, even) and, consequently, overcome the limitation of the SHE algorithm applicability. Finally, a real case study in the textile factory is conducted, using real measurements provided by power quality analyzer measuring devices, to validate the proposed ac/dc/ac converter supplying a sensitive load of 50 kVA, given by an asynchronous motor drive.

**INDEX TERMS** AC/DC/AC converter, asymmetrical cascade H-bridge (ACHB), asynchronous motor drive, case study, MATLAB/Simscape electrical, modulation technique, shunt active filter (SAF).

## I. INTRODUCTION

Multilevel inverters (MLIs) are applied to a variety of distributed power sources, such as photovoltaics, fuel cells, supercapacitors, and batteries, due to their capability of generating the appropriate stepping ac voltage from multiple dc sources. MLI operates at the fundamental switching frequency, which helps to improve inverter efficiency, reduce voltage stress, and minimize conduction losses compared with the traditional two-level pulsewidth modulation (PWM) inverters. In addition, traditional PWM inverters operate at high switching frequencies that can cause motor failures, bearing failures, and windings insulation breakdown due to the fast voltage changes applied to the electrical motors [1]. Furthermore, multilevel converters, including MLI, can operate without power transformers at medium voltage (MV), with high power ratings. This feature is particularly advantageous for transformerless MLIs, which can replace traditional power inverters, such as 12-, 24-, and 48-pulse inverters [2].

Numerous modulation algorithms have been proposed in the literature to control the output stepping voltage of MLI at the fundamental switching frequency and minimize its harmonic content [3], [4], [5], [6], [7], [8], [9], [10], [11]. Furthermore, several topologies have been developed to integrate this structure into the grid side while satisfying two constraints: stabilizing and regulating the dc voltages at each cascaded module without affecting the power quality at the grid side [12], [13], [14].

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A generalized technique for harmonic elimination was proposed by Patel and Hoft [3] that allows the mitigation of a finite number of harmonics at the output voltage of both half- and full-bridge inverters, as well as the remaining uneliminated higher order harmonics attenuated by output filter at the load side. In [4], an analytical approach using the selective harmonic elimination (SHE) algorithm was introduced for the five-level symmetrical cascaded H-bridge (SCHB). Moreover, in [5], a simple computational method of the switching angles for nine-level SCHB MLI was proposed. In [6], a new particle swarm optimization approach was developed as a solution for the harmonic minimization problems for a five-level SCHB. However, in [7], the genetic algorithm was proposed to compute the switching angles of the SCHB inverter. This genetic optimization approach is limited in this article, as well as in [3], [4], [5], and [6], to the symmetrical MLI structure.

On the other hand, a novel approach to modulate the amplitude with fixed width was presented in [8], which allows eliminating the harmonic contents from the output voltage except the harmonic order $(2Lk \pm 1)$, where $L$ is the number of levels, and $k = 1, 2, 3, \ldots$. However, the main drawback of this technique is the output voltage waveform that has a total harmonic distortion (THD) ratio higher than the IEEE-519 standard. In [9], a self-elimination approach was developed for single-phase applications by mitigating the triplen harmonic only without considering the conventional harmonics of the rank $(6k \pm 1)$, with $k = 1, 2, 3$, etc.

From the perspective of the MLIs power circuit structure, SCHB ensures the diminishing of the THD and obtaining an output voltage waveform close to a sinusoidal waveform, such as [4], [5], and [7]. The main drawback of the SCHB structures is the higher number of cascaded H-bridge (CHB) modules required to ensure an output voltage signal close to the sinusoidal waveform. For instance, to obtain a THD less than 5%, one should set up 17 levels, 8 modules of SCHB-MLI inverter—while for a harmonic elimination up to the 49th order, a 27-level inverter is required, i.e., [13 modules of SCHB-MLI] [8].

To overcome this practical/industrial limitation, asymmetrical cascade H-bridge (ACHB) schemes have been suggested as an alternative solution to SCHB. The ACHB structure allows an increase in the number of voltage levels with a limited number of CHB modules. For example, in [10], different configurations were introduced for ACHB-MLIs based on three ACHBs with dc-voltage configurations/ratios of {1:2:4}, {1:2:6}, and {1:3:9}. These topologies generate, respectively, 15, 19, and 27 levels in the output voltage, respectively. In [11], four ACHB modules were used with ratios {1:2:4:8} to generate an output stepping voltage with 31 levels.

Moreover, the majority of works considered dc sources as constant and/or isolated dc sources, such as Photovoltaic (PV) systems or batteries [3], [4], [5], [6], [9], whereas only a few research articles introduced a full solution as ac/dc/ac converter based on the cascade MLI, which are more adapted with the reality than the constant/isolated dc sources-based structures. In this context, the *LCL* grid-connected PWM-active front-end topology, connected to the grid by a phase-shifted multiwinding transformer, is proposed to energize the CHB modules [12]. It is worth noting that the use of the *LCL* filter is restricted by the control complexity and the destructive phenomenon of series and/or parallel resonances/antiresonance with the grid [15]. Also, Lezana et al. [16] suggested a single-phase (reduced cell-CHB) topology connected to the ac grid side through passive *L*-series filter; the reduced cell consists of two insulated gate bipolar transistors (IGBTs) and two capacitors. The main disadvantage of this structure is that the input current is twice that of the active rectifier-CHB.

Moreover, in [13], a single-phase back-to-back CHB is employed as a solution for MV motor-drive application. However, a complex control strategy, based on two controllers: average dc-link voltage controller and voltage-balancing controller, was proposed in this article to regulate the dc-link voltages. Besides, this structure requires an active rectifier for each CHB, while the interface coupling system (*L*-series filter) is employed to ensure the grid connection through the tertiary winding transformer. Finally, for automotive applications, Khoucha et al. [14] introduce the three-phase rectifier, without transformer, for each CHB module, with *LC* filters at dc side. This structure generates distorted load voltage.

### A. NOVELTY/IMPROVEMENT

The novelty/improvement of this work, with respect to the literature, lies in proposing an advanced ac/dc/ac converter structure based on two main aspects: an advanced modulation approach for ACHB-MLI, using a combination of staircase modulation technique (SMT) and SHE techniques that calculates, adapts, and limits the switching angles while minimizing the number of CHB modules. This approach also ensures, with a low rating of dc-side capacitors, output voltage devoid of specific harmonics for sensitive load (SL) applications, including those that could appear if the maximum limit of the switching angles, detailed in this research, is exceeded. The idea of these advanced/combined control techniques (SMT-SHE), applied to the proposed ACHB-MLI structure, is to minimize the number of CHB modules while compensating the reduction effect by integrating an adapted SHE algorithm. Indeed, the reduction of the CHB modules leads to the degradation of output voltage harmonic mitigation, while good selection of the switching angles of the SHE algorithm offers a targeted elimination of predominant/specific harmonics. As a result, combined control techniques (SMT-SHE) validate both THD recommendations as well as the elimination of undesirable specific harmonics for SLs while minimizing the number of CHB modules and the dc-side capacitors' ratings. The second aspect is a combination of multiwinding transformers and conventional diode rectifiers associated with one or a limited number of three-phase shunt active filter (SAF) to simplify the ac/dc structure and significantly improve the power quality on the grid side, thus maintaining the low rating of the dc-side capacitors.

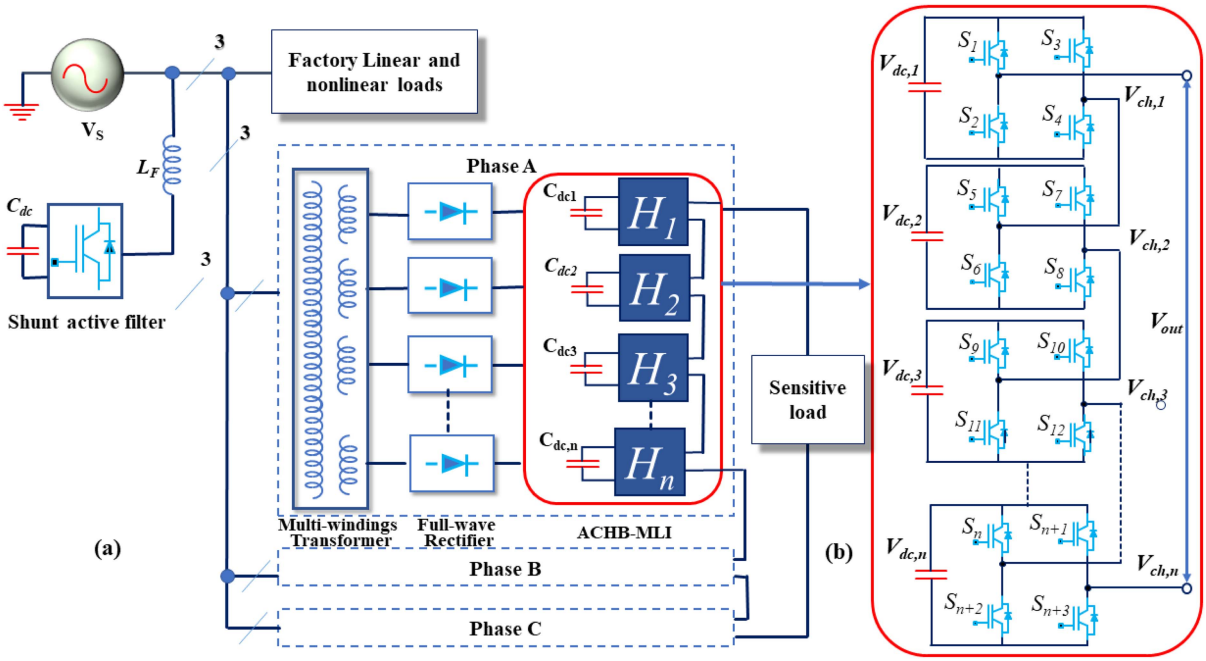


**FIGURE 1.** (a) General scheme of the proposed ac/dc/ac structure. (b) ACHB-MLI with *n* CHB modules.

Finally, the performance and effectiveness of the proposed advanced structure will be validated within a real environment, textile factory, by taking site measurements on its network using power quality analyzers. To address this issue, this structure will be designed to eliminate the harmonic content at the output voltage applied on an SL, i.e., asynchronous motor, that suffers from the effect of specific harmonics while improving the power quality on the grid side. The contribution of this work, which introduces the proposed ac/dc/ac converter operating within the constraints of harmonic reduction as specified by the IEEE-519 norm for THD in load and grid voltages, is outlined in the following key aspects.

1) Determine the minimum number of the CHB modules, knowing that the increase of the modules number leads to obtain an output voltage of the MLI closer to sinusoidal shape and to reduce consequently the THD of the MLI output voltage.
2) Identify the appropriate dc configuration of the ACHB-MLI, noting that increasing the difference between the dc voltages results in raising the voltage levels and the switching angles of the SHE algorithm. Consequently, the output voltage waveform is closer to sinusoidal, devoid of specific/predominant harmonics.
3) Make a tradeoff between the previous constraints (1) and (2) considering accepted/industrial values of the dc-side capacitors. It is worth noting that the capacitor rating of each CHB is inversely proportional to the number of modules and the level of the output voltage.
4) Apply the proposed/controlled SMT-SHE-based ACHB -MLI structure to supply/drive an asynchronous motor, which is very sensitive to specific ranks of torque and voltage harmonics and requires controlled output voltage amplitude for motor speed variation; this latter is ensured by a variation of the modulation index parameter of the SHE.
5) Provide a grid-side real-time harmonic mitigation ac/dc structure that is easy to design, install, and maintain, for instance, the conventional diode rectifiers, associated with three-phase SAF.

## II. PROPOSED AC/DC/AC STRUCTURE FOR HARMONIC DISTORTION REDUCTION

The proposed ac/dc/ac topology is illustrated in Fig. 1(a). This structure ensures a three-phase voltage waveform that closely approaches a sinusoidal waveform at both load and grid sides. The suggested ACHB-MLI can be built, without constraints, with *n* number of CHB modules per phase, whose outputs are connected in series. The dc voltages of these modules are configured asymmetrically to obtain different output stepping voltages. These modules are energized by the combination of a single-phase multiwinding transformer with single-phase full-wave conventional diode-based rectifiers. These rectifiers are equal in number to the cascade *H*-bridges' modules as well as to the secondary windings of the multiwinding transformer whose primary windings of the three phases are connected, to the grid, in a delta configuration to avoid the propagation of the triplen harmonics.

However, the ac/dc front-end converter-based rectifier pollutes the grid by harmonic current components, leading to poor local power quality and affecting neighboring loads. To mitigate these harmonics' impacts, an SAF (SAF) is employed to cancel out these harmonic perturbations to obtain a grid

current and, consequently, a grid voltage, as close as possible to a sinusoidal waveform.

Using this ac/dc/ac topology, a tradeoff between the complexity of the converter structure and the power quality can be realized, along with several further advantages. First, the use of multiwinding transformer eliminates the need for dc-voltage regulators, as described in [12]. Second, unlike other topologies, it does not require bulky damping inductors connected in series with each full-wave rectifier or higher order *LCL* filters connected to the active PWM rectifiers to mitigate its switching frequency. However, this *LCL* filter interacts with the equivalent grid-side inductance, causing the destructive resonance/antiresonance phenomenon. Third, there is no need for notch filters to eliminate the second-order frequencies, common on the dc sides [14] or huge capacitors, as stated in [11].

Besides, for SL application, i.e., asynchronous motor drive, the proposed structure of dc/ac side should ensure a variable amplitude of an output fundamental voltage closer to sinusoidal and free of specific/undesired harmonics. These undesired/specific harmonics distort the rotating magnetic field produced by the stator. Consequently, the rotor will experience additional torque fluctuations, specifically named harmonic torques, which affect, among other things, the motor speed, overheating of the motor winding, and develop braking torques imposed by the inverse/negative harmonic components [17], [18], [19]. It is important to highlight that these specific/undesired harmonic ranks vary according to the air-gap MMF harmonic, the saturation of the machine core, and the teeth body.

Therefore, this article presents an appropriate combination SMT-SHE modulation technique adapted to ACHB-MLI structure. The proposed dc/ac structure ensures an almost sinusoidal shape with a variable amplitude of the output voltage according to the motor speed variation, as well as a wideband free of predominant harmonics, including the specific/undesired ones.

## III. NOVEL MODULATION APPROACH SMT-SHE FOR ACHB-MLI

In this section, an advanced modulation technique is proposed for ACHB-MLI suitable for various applications, such as MV, low-voltage, motor-drive, 60/50 Hz frequency converter, automotive, and industrial. This novel modulation approach is configured by adapting and optimizing a combination of two modulation techniques as one modulation algorithm. Particularly, in SMT and SHE, the SMT uses various configurations/combinations of the dc sources to generate, depending on the number of modules, an approximately sinusoidal output voltage signal. Meanwhile, the SHE modulation technique allows determining the switching angles corresponding to each voltage step generated by SMT technique to eliminate individual and predominant and/or specific harmonics in the output voltage signal. As a result, the novel approach aims to achieve the following objectives.

**TABLE 1. THD% for the Line Voltage of ACHB Three and Four Modules**

| Number of modules | Configuration | Number of levels | THD% |
|---|---|---|---|
| 3 | [1:2:4] | 15 | 8.18% |
| 3 | [1:2:6] | 19 | 6.03% |
| 3 | [1:3:9] | 27 | 4.17% |
| 4 | [1:2:3:4] | 21 | 5.07% |

1) Improve the power quality of the output voltage applied to ac loads by reducing the THD ratio according to the IEEE-519 standard by using the SMT technique and the minimum number of ACHBs.
2) Eliminate, using the adapted SHE technique, a bandwidth of specific harmonics that disturb the optimal operation of certain SLs, such as the asynchronous motor drive.
3) Identify the number of output voltage levels, for a minimum number of ASHB, and the corresponding dc-side capacitor values to meet the industrial requirements.
4) Study in depth the limitations of the SHE switching angles for a three-phase system.

### A. PROBLEM STATEMENT AND SOME RECALLS FOR A SINGLE-PHASE STRUCTURE

#### 1) ACHB-MLI BASED ON THE SMT

SMT is a technique used in asymmetric MLIs to increase the output voltage level without requiring additional CHB modules. It works by dividing the dc input voltages into multiple levels and generating a staircase waveform for the output voltage. By using different ratios of dc-voltage levels, the staircase waveform can be varied to achieve different output voltage levels. The resulting waveform of the output voltage has reduced its harmonic content compared with traditional inverters or MLIs, such as SCHB-MLI. In all cases, it is important to carefully select capacitors suitable for industrial use, especially when the structure is energized by the grid through ac/dc rectifiers.

In [20], SMT was proposed for 3 modules, ACHB-MLI, with 2 dc voltages' configurations to generate 19 and 27 voltage levels, respectively. These configurations use ratios of [1:2:6] and [1:3:9], where the second one corresponds to the independent dc voltages of [24, 48, 144] V.

In order to motivate the choice of the number of ACHB modules associated with the SMT algorithm, a complementary study, via-a-vis the literature, is made in this research. In this context, a comparison between three and four modules SMT-SCHB structure supplying/driving a low-voltage SL, for instance, asynchronous motor, is made, as presented in Table 1. Noting that beyond four modules based structures, reliability, economic, and industrial constraints limit their implementation.

From Table 1, apparently, the three modules raise the voltage level up to 27, to reduce the THD ratio to 4.17%. However, this configuration is limited by the capacitors' ratings since their HB modules are connected in series. In the same context,

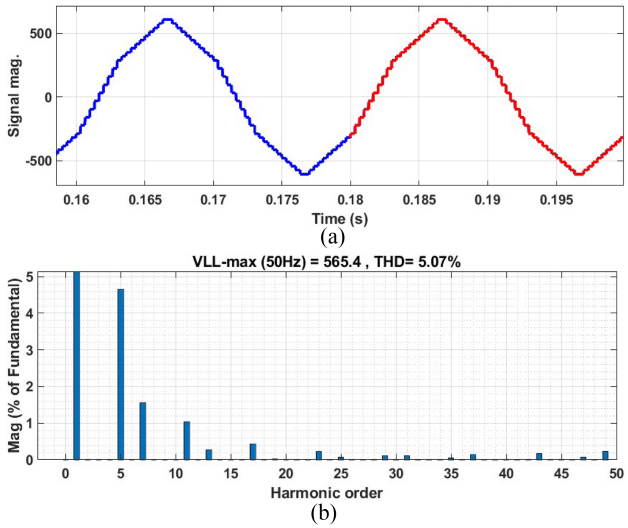


**FIGURE 2.** **Output voltage of four modules ACHB commanded by SMT. (a) Time domain. (b) Frequency domain.**

the minimum voltage level of the four modules reduces the THD ratio of the output voltage to 5.07%, as demonstrated in Fig. 2(b). The corresponding time-domain waveform, as demonstrated in Fig. 2(a), is distorted by predominant low harmonic ranks, including the fifth, in which its individual distortion ratio is 4.6% of the fundamental line voltage of 400 V. It is worth noting that these individual/predominant harmonics could severely affect certain SLs; see Section IV-C.

In the same context, the SMT accompanied by space vector modulation was proposed for 3 modules ACHB-MLI to generate 42 voltage levels in [21]. This configuration was set up as [1:4:16] that corresponds to dc voltages of [5,20,80] V with identical capacitors of 11 mF. The THD of the resulting line voltage was reduced to below 2%. However, a voltage-level jump occurred at each nonreachable level as the maximum achievable level from three modules' topology is 27.

In the MV application, SMT technique was suggested for four modules ACHB structure in [11]. These modules are configured to generate 31 voltage levels as follows [1:2:4:8], which correspond to the dc voltages [575, 1150, 2300, 4600] V; each module was equipped with an identical capacitor of 10 mF. This configuration limits the harmonic reduction of line voltage to a THD of 2.75% since the IEEE-519 norm for the producer side of the MV networks is 3% max. Moreover, this structure was performed depending on self-balancing capacitors where the first module is fed by an isolated master dc source, and the remaining three modules are fed by three floating capacitors.

Finally, based on the literature and the complementary study of this research, the SMT technique needs to be reinforced to obtain a validated THD voltage and eliminate some predominant harmonics, which can severely affect certain SLs.

#### 2) SCHB-MLI BASED ON SHE

SHE modulation technique is commonly used to synthesize the output stepping voltage waveform of the single-phase symmetric SCHB-MLI inverter. This approach computes numerically the switching angles needed to SCHB-MLI to mitigate the individual and predominant harmonics at its output voltage signal [3], [4], [5], [7], [22]. This numerical computation is made offline by solving a series of nonlinear transcendental equations, while a lookup table is exploited to store the desired switching angles for real-time implementation [5].

In [5], SHE-based linear system solution (LSS) is used to generate nine voltage levels for a single-phase SCHB-MLI structure based on four CHB modules. To set up this structure, independent dc sources are employed. The switching angles are calculated for two cases: First, to mitigate the harmonics orders third, fifth, seventh, and their odd multiples; second, to mitigate the harmonics orders third, fifth, and their odd multiples, while imposing the modulation index to ensure output voltage variations. The first case results in a reduction of the output voltage THD to 10.89%, while in the second case, a higher THD ratio is obtained with the modulation index varying from 0.3 to 1. Besides, the switching angles calculated, at a modulation index of 0.3–0.7, have at least one angle exceeding the 90°, which reduces the output voltage level.

In [8], a new pulse active width modulation (PAWM) was applied on three modules, single-phase SCHB-MLI, to generate seven voltage levels. As a result, the output voltage had a THD ratio of 11.86%, which was achieved using three independent dc voltages of [164.9, 132.2, 73.38] V. In [22], a genetic algorithm is used to determine the real-time switching angles for three modules, single-phase SCHB-MLI with independent dc supplies. The resultant output voltage is generated with seven levels, free of harmonic orders third, fifth, and with a predetermined modulation index. Despite these achievements, the THD ratio of output voltage remained higher than 18% and, in certain cases, it reached 31.1%.

The main drawback of using SHE with SCHB-MLI is the requirement of a large number of CHB modules and switching angles to meet the power quality standard IEEE-519-2014. To overcome this drawback and achieve higher voltage levels with a minimum number of CHB modules, we propose the ACHB-MLI structure commanded/controlled through a novel modulation technique based on both SMT and SHE that is able to reduce the THD and to eliminate the wideband of *predominant* harmonics in the generated voltage.

### *B. ACHB-MLI-BASED NOVEL MODULATION APPROACH SMT-SHE*

The ACHB topology is commonly associated with the use of SMT, while SHE is typically utilized with SCHB structure. However, in this research, a combination of two techniques is employed together in ACHB-MLIs, aiming to achieve improved performance, increased output voltage levels with a

reduced number of CHB modules, reduction of the overall output voltage THD, elimination of a wideband of specific harmonics, and variation of the output voltage amplitude for specific loads, for instance, asynchronous motor drive. However, the main objective of the SHE algorithm is to define a set of harmonic ranks to be eliminated by the SHE-SMT algorithm. Thus, one can eliminate the lowest harmonic orders at the output voltage waveform of the ACHB-MLI or the predominant harmonic orders that might be generated by an SL.

Let us consider an ACHB-MLI structure with $n$ CHB modules supplied by the voltages $V_{\mathrm{dc},1} = k_1 V_{\mathrm{dc}}, \ldots, V_{\mathrm{dc},n} = k_n \mathrm{V}_{\mathrm{dc}}$, where $k_1, \ldots, k_n$ are the positive real numbers. One can represent the dc sources configuration as $\{1, k_2/k_1, \ldots, k_n/\mathrm{k}_1\}$, meaning that $V_{\mathrm{dc},1}/V_{\mathrm{dc},2} = k_1/k_2, \ldots, V_{\mathrm{dc},1}/V_{\mathrm{dc},n} = k_1/k_n$. Each configuration of dc sources produces a unique output stepping voltage. For example, for $n = 3$ CHB modules, one can have configurations, such as {1:2:4}, {1:2:5}, {1:2:6}, and {1:3:9}, which provide, respectively, 15, 17, 19, and 27 output voltage levels. The selection of dc configuration depends on the associated capacitors' ratings and the desired power quality of the output voltage of the inverter. Indeed, increasing the difference between the dc voltages leads to increased voltage levels of the SMT as well as the switching angles of the SHE algorithms. Therefore, the output voltage is, respectively, closer to sinusoidal shape and free of specific/predominant harmonics.

However, the equivalent dc voltage $V_{\mathrm{dc}}^{*}$ for this topology is given by $V_{\mathrm{dc}}^{*} = \varkappa\, V_{\mathrm{dc}}$, where $\varkappa$ is the number of voltage steps per quarter cycle. In addition, one can denote the output voltages for each H-bridge module by $v_{\mathrm{ch},k}$; $k = 1, 2, \ldots, n$. Therefore, the output phase voltage $v_{\mathrm{out}}$ becomes $v_{\mathrm{out}} = v_{\mathrm{ch},1} + v_{\mathrm{ch},2} + \cdots + v_{\mathrm{ch},n}$.

Since the higher the number of voltage levels, the lower the lowest asymmetrical dc voltage, and consequently, the higher the related capacitor value, we will concentrate to a minimum, with respect to the SMT technology, of three CHB modules with $\{1, k_2/k_1, k_3/k_1\}$ same configuration, as depicted in Fig. 1(b), for three modules instead of $n$. It is worth noting that the results of this work can be easily extended to more general configurations and number of modules as we will demonstrate in the case study. Thus, the dc sources can configure as $k_1 = 1$, $k_2 = 2$, and $k_3 = 4$ with the voltage ratios {1:2:4}, such as

$$\begin{aligned} & V_{\mathrm{dc},1} = 1 \text{ PU} \\ \rightarrow\ & V_{\mathrm{dc},2} = \frac{V_{\mathrm{dc},1}}{2} = 0.5 \text{ PU} \\ \rightarrow\ & V_{\mathrm{dc},3} = \frac{V_{\mathrm{dc},1}}{4} = 0.25 \text{ PU}. \end{aligned} \tag{1}$$

In this context, PU means "per unit." By setting $V_{\mathrm{dc},3} = V_{\mathrm{dc}}$, clearly, $V_{\mathrm{dc},1} = 4V_{\mathrm{dc}}$ and $V_{\mathrm{dc},2} = 2V_{\mathrm{dc}}$, where $V_{\mathrm{dc}}$ is a base dc-voltage value fixed in accordance with the required load voltage. In this case, the modulation technique has seven symmetric switching angles and seven voltage steps for each quarter-cycle waveform, as well as a zero-voltage level. This results in a total of 15 voltage levels in the output, as shown in Fig. 2. In fact, the number of the output voltage levels $L$ for this asymmetrical topology is given by

$$L = 2\left(V_{\mathrm{dc},1} + V_{\mathrm{dc},2} + V_{\mathrm{dc},3}\right) + 1 = 15\, V_{\mathrm{dc}}. \tag{2}$$

**TABLE 2. Switching Patterns for ACHB—3 Modules, 15 Levels**

| $V_{out}$ | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ | $S_7$ | $S_8$ | $S_9$ | $S_{10}$ | $S_{11}$ | $S_{12}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| $E_1$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| $E_2$ | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| $E_3$ | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| $E_4$ | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $E_5$ | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| $E_6$ | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| $E_7$ | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |

Two choices of switching angles can be considered. The switching angles can be computed to eliminate only the predominant harmonics (seven harmonics' ranks in this case). Alternatively, with the same configuration, one can eliminate six harmonics as well as adjust the amplitude of the fundamental output voltage. In ACHB-MLI topology, one can consider that the number of switching angles $\alpha_k$ and the number of voltage steps $\varkappa$ are equal per quarter cycle, where $k = 1, 2, 3, \ldots, \varkappa$. Therefore, in a single-phase application, the switching angles $\alpha_k$ have to satisfy the condition $0° \leq \alpha_1 < \alpha_2 < \cdots < \alpha_{\varkappa} \leq 90°$ [4]. However, in a three-phase application, these angle values should be optimized to prevent generating the even and zeros harmonics. In this article, we consider symmetric output voltage waveform $v_{\mathrm{out}}(\omega t)$. This implies that even harmonics are not present at the output voltage waveform for $\theta \in [0, \pi/2]$, which permits us to express the output voltage waveform as a Fourier series containing only odd harmonics.

To set up the switching states of the ACHB-MLI, we will consider, for clarity, the three ACHB modules with {1:2:4} configuration. The states of these ACHB switches $S_i$; $i = 1, \ldots, 12$, can take values in the set {0,1}, and the string $S_i$ of 0/1 values is called a "switching pattern." The switching patterns required to realize the 15 voltage levels are provided in Table 2 for one positive quarter cycle. It is worth noting that the output voltage steps $V_i$ could be realized with more than one pattern.

After assigning the switching pattern for each voltage step, one can generate the output voltage steps $E_1, \ldots, E_7$ during the interval [0°,90°], as depicted in Fig. 3(a). Each switching pattern is scheduled to turn ON/OFF the transistors associated with $S_1, \ldots, S_{12}$ at specific switching angles $\alpha_1, \ldots, \alpha_{\varkappa}$. To impose the ON/OFF values to the transistors, considering for simplicity just the switches $S_1, \ldots, S_4$ [upper module of Fig. 1(b)], it is possible to compare the value of a sawtooth signal generator $\mathbb{N}$ with a desired switching angle $\alpha$, using two comparators and two logic AND gates, as appeared in Fig. 3(b). They constitute a "block," here called Block (A), that commands $S_1, \ldots, S_4$. Similar blocks can be used for the other switches. If

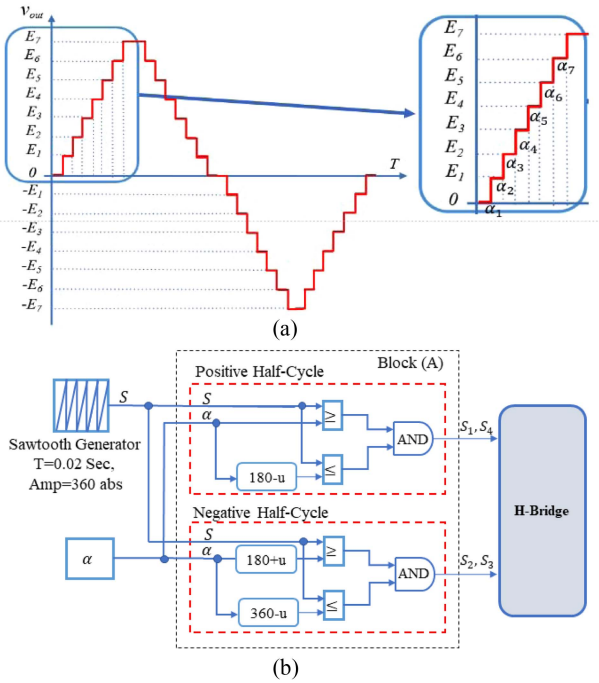


**FIGURE 3.** **(a) Output voltage $v_{out}$ for ACHB-MLI—3 Modules, 15 levels. (b) SHE-SMT technique scheme for one switching angle.**

$\mathbb{N} \in [\alpha, 180° - \alpha]$, the transistors corresponding to ($S_1$, $S_4$) are turned ON, during the positive quarter cycle. If $\mathbb{N} \in [180° + \alpha,\ 360° - \alpha]$, then those corresponding to ($S_2$, $S_3$) are turned ON, during the negative half-cycle. Repeating the same for the other two modules of the H-bridges of Fig. 1(b), one finally obtains the output of Fig. 3(b) imposing one switching angle to the upper module, three to the central module, and seven to the lower module.

In order to formulate the output voltage as a function of the switching angles and the harmonic ranks $\mathcal{H}$ needed to be eliminated, let us define the general harmonic rank as the set of integers from $j = 2$ until $j_{\max} = 49$ representing the harmonic orders contributing to the signal $v_{\text{out}}(t)$, where $j_{\max}$ is chosen so that the contribution to the output signal due to higher harmonics is considered negligible.

The harmonic rank for a single-phase system is the set of odd harmonics' components $j = 3,\ \ldots,\ j_{\max}$, while the harmonic rank for a three-phase system is given by $j \in \{6j \pm 1 \,|\, j = 1, 2,\ \ldots, j_{\max}\}$. To control the amplitude of the fundamental component $v_1$, $j = 1$ is addressed. Following [1] and [2], the output voltage $v_{\text{out}}(t)$ can be written as a Fourier series

$$v_{\text{out}}(\omega t) = \sum_{j=1}^{j_{\max}} v_j \cdot \sin(j\omega t)$$

$$v_j = \frac{4}{\pi} \cdot \frac{V_{\text{dc}}^*}{j} \sum_{k=1}^{\varkappa} \cos(j\alpha_k) \tag{3}$$

where, in the case of a single phase where one considers only the odd harmonics, one imposes $\varkappa$ constraint, with $\varkappa$ the odd integer indicating the voltage steps of the ACHB MLI output voltage

$$\begin{aligned} v_1 &= \frac{4}{\pi} \cdot V_{\text{dc}}^* [\cos(\alpha_1) + \cdots + \cos(\alpha_\varkappa)] \\ v_3 &= \frac{4}{\pi} \cdot \frac{V_{\text{dc}}^*}{3} [\cos(3\alpha_1) + \cdots + \cos(3\alpha_\varkappa)] = 0 \\ &\vdots \\ v_j &= \frac{4}{\pi} \cdot \frac{V_{\text{dc}}^*}{j} [\cos(j\alpha_1) + \cdots + \cos(j\alpha_\varkappa)] = 0,\ \ j = \varkappa. \end{aligned} \tag{4}$$

Clearly, with these conditions, one imposes for the fundamental component a desired amplitude and the mitigation of the first $\varkappa - 1 = \mathcal{H}$ low-order harmonics. Under the assumption of symmetric waveforms, considering the $\varkappa$ switching angles and $v_j$ the voltage harmonic to be eliminated, one can impose the following conditions:

$$v_1 = \frac{4}{\pi} V_{\text{dc}}^* \sum_{k=1}^{\varkappa} \cos(j\alpha_i),\ \ v_j = \sum_{k=1}^{\varkappa} \cos(j\alpha_i) = 0. \tag{5}$$

## IV. NUMERICAL CASE STUDY OF THE NOVEL MODULATION APPROACH

The techniques of the SMT and the SHE, as recalled in Section III, are combined to obtain improved performance for the ($n$) CHB modules based ACHB-MLI.

### A. TRIGGERING ANGLES ALGORITHM (GENERAL CASE)

Referring to the single-phase case and applying the SHE for finite voltage steps $\varkappa$, the triggering angles can be determined by solving an optimal problem that minimizes the function in (4) to be zeroed. The constraint on these predetermined angles is that the resulting solutions $\alpha_1,\ \ldots,\ \alpha_\varkappa$ should fall within their range of $\alpha_{\min} \le \alpha_1 + \delta_{\min} \le \alpha_2 + \delta_{\min} \le \cdots \le \alpha_\varkappa + \delta_{\min} \le \alpha_{\max}$, where $\alpha_{\min} = 0°$ and $\alpha_{\max} = 90°$ are the minimum and maximum angle values, and $\delta_{\min}$ is the switch gap. Furthermore, the desired fundamental output voltage $v_1$, which varies according to specific modulation index $M$, is calculated in (6a), while the modulation index is determined in (6b), with $C$ a definitive positive number [5]

$$\begin{aligned} v_1 &= \frac{4\, V_{\text{dc}}^*}{\pi} \sum_{k=1}^{\varkappa} \cos(\alpha_i) \\ &\rightarrow \left[ \sum_{k=1}^{\varkappa} \cos(j\alpha_i) \right] - \frac{\pi \cdot \varkappa \cdot M}{4} = 0 \end{aligned} \tag{6a}$$

$$M = \frac{v_1}{V_{\text{dc}}^*} = \frac{v_1}{\varkappa \cdot V_{\text{dc}}},\ V_{\text{dc}}^* = C \cdot M,$$

$$C = \frac{\varkappa}{\sum_{k=1}^{\varkappa} \cos(\alpha_k)} > 0. \tag{6b}$$

The remaining $\varkappa - 1$ conditions (3) can be exploited to mitigate the $\varkappa - 1$ harmonics in $\mathcal{H}$. These $\varkappa - 1$ harmonics are low-order ones that have a higher amplitude and appear

right after the fundamental frequency. To solve (4), for instance, Newton-Raphson's (NR) method can be employed as the following procedure [3].

1) Select the $(\varkappa-1)$ predominant/specific harmonics, according to SL specifications, to be eliminated.
2) Fix some appropriate initial value for the switching angle vector $\alpha_{k,0} = (\alpha_{1,0},\ \alpha_{2,0}, \ldots, \alpha_{\varkappa,0})^T$ with respecting the angle constraint.
3) For the iterative steps $j = 1, 2, \ldots, \varkappa$ and $k = 1, 2, \ldots, \varkappa$, compute the matrices

$$F_j = \begin{pmatrix} v_1 \\ \vdots \\ v_h \\ \vdots \\ \vdots \end{pmatrix}, \quad \frac{\partial F_j}{\partial \alpha} = \begin{pmatrix} -\sum_{k=1}^{\varkappa} j \cdot \sin(j\alpha_k) \\ \vdots \\ -\sum_{k=1}^{\varkappa} j \cdot \sin(j\alpha_k) \\ \vdots \\ \vdots \end{pmatrix}, \ \alpha_k = \alpha_{k,0} \quad (7)$$

and the new angle vector

$$\alpha_{k+1} = \alpha_k - \left(\frac{\partial F_j}{\partial \alpha}\right)^{-1} |_{\alpha_k} F_j |_{\alpha_k} \rightarrow \alpha_{k,0} = \alpha_{k+1}. \quad (8)$$

1) Validate the range of the switching angle's constraints.
2) Finally, the iterations end when a certain (fixed) accuracy is reached at the final step $\mathcal{M}$.

After calculating the switching angles using the SHE technique for a certain harmonic rank, the obtained switching angles are set as starting points for the desired voltage levels generated by the ACHB-MLI structure via the SMT technique, as illustrated in Fig. 3(a) and (b).

Section IV-B examines this method in two potential scenarios for switching angle determination in single-phase applications. Subsequently, the calculation of switching angles will be extended to be suitable for three-phase applications in Section IV-C.

### B. SWITCHING ANGLES CALCULATION OF THE SMT-SHE APPROACH AT VARIOUS MODULATION INDICES

The modulation index is a crucial parameter to control the output voltage for a grid-tied inverter. This allows the output voltage to be varied for a fixed grid-side input voltage. Meanwhile, in motor-drive applications, the variation of inverter output voltage, depending on the required torque and speed, further affects the motor voltage and torque harmonic problem and imposes various specific harmonic ranks to be eliminated. Therefore, the precise determination of the switching angles leads to the best motor-drive performance. In fact, some methods have limitations in calculating the modulation index, for instance, Buccella et al. [5] use the SHE-based linear solution method to assign switching angles for SCHB four modules. Indeed, four angles had been selected; one angle is predefined to adjust the modulation index and three switching angles are trajected to mitigate two harmonics and their multiples. However, the lowest THD was 10.89% and the resulting switching angles exceeded the angles' constraints of 90° at the modulation index $M = 0.7$.

**TABLE 3. Switching Angles for a Single-Phase 15-Level ACHB-MLI With and Without Modulation Index Variation**

| $M$ | $\alpha_1$ | $\alpha_2$ | $\alpha_3$ | $\alpha_4$ | $\alpha_5$ | $\alpha_6$ | $\alpha_\varkappa$ | $THD\%$ |
|---|---|---|---|---|---|---|---|---|
| 1 | 8.62° | 10.32° | 24.53° | 33.55° | 45.54° | 61.64° | 87.47° | 6.91% |
| 0.9 | 9.47° | 9.47° | 24.56° | 33.5° | 45.521° | 61.69° | 87.46° | 7.24% |
| 0.7 | 6.82° | 15.77° | 29.71° | 41.83° | 60.25° | 88.82° | 88.82° | 7.44% |

In order to supply, in this research, an SL by the proposed SMT-SHE algorithm-based ACHB-MLI structure, ensuring output voltage fulfilled with the THD recommendations, devoid of the predominant/specific harmonics, associated with amplitude variation of the output voltage, the tradeoff was made. Indeed, to ensure these latter specifications/constraints, a minimum CHB module associated with appropriate dc-voltage configuration and, thus, low/industrial dc-side capacitors' ratings, only 3 CHB modules-based structure, configured as [1:2:4], to generate 15 levels is adopted. To evaluate the effectiveness of the single-phase topology of the adopted structure, one can examine two scenarios. In the first scenario, the switching angles are calculated to realize a predefined modulation index and to eliminate a specific harmonic spectrum. In the second scenario, the switching angles are calculated to eliminate a wide harmonic spectrum.

For both scenarios, SMT-SHE calculated seven switching angles. One angle is set to assign $M$ and six angles are set to eliminate the lowest/predominant orders of the harmonics in the first scenario. Therefore, one can examine $M$ taking the values of $M = [0.9,0.7]$ and $\mathcal{H} = \{3, 5, 7, 9, 11, 13\}$. In the second scenario, the seven angles are subjected to eliminate a harmonics rank consisting of seven lowest harmonic orders, such as $\mathcal{H} = \{3, 5, 7, 9, 11, 13, 17\}$ and $M = 1$. Therefore, one can determine the switching angles for both scenarios, as reported in Table 3, including the THD% for each case, which is expressed as the following notation:

$$\text{THD\%} = \sqrt{\frac{\sum_{i=2}^{\infty} v_i^2}{v_1^2}}. \quad (9)$$

It is worth noting that this research opted for the elimination of the 17th harmonic rank instead of 15th, according to specifications related to certain SLs, i.e., asynchronous motor drive [19]. Table 3 illustrates that the lowest harmonic distortion of the output voltage occurred in the second scenario when its THD% was reduced to 6.91%. Despite the control of the fundamental component of the output voltage, in the first scenario, the THD% of the output voltage reduced at each value of $M$ is set to 7.24% and 7.44%, respectively. Notably, the THD percentage is bigger than the first scenario due to the

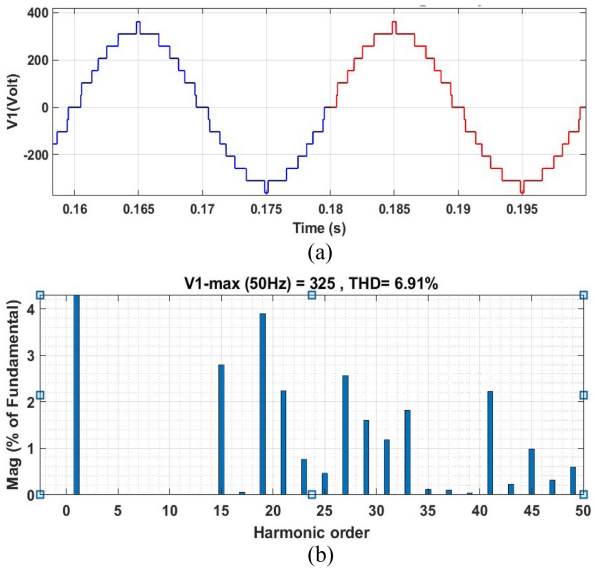


**FIGURE 4.** Output voltage of a 15-level single-phase ACHB-MLI. (a) Time domain. (b) Spectrum analysis.

presence of harmonic order 17th in comparison with the first scenario.

The output voltage of the second scenario was analyzed in the time and frequency domains, as shown in Fig. 4(a) and (b), respectively, using MATLAB/Simulink/Simscape electrical. Clearly, the output voltage waveform had seven voltage steps per quarter cycle, with a maximum value of $v_1 = \sqrt{2}\ 230$ V and THD of 6.91% in the frequency domain.

### C. SMT-SHE TECHNIQUE FOR THREE-PHASE SYSTEMS (SWITCHING ANGLE LIMITATION)

In a three-phase asynchronous motor drive, the harmonic components $h$ take the rank of $\{h = 6j \pm 1 \mid j = 1, 2, \ldots, j_{\max}\}$. Therefore, the interaction of the air-gap flux $\Psi$ with rotor current $I_r$ generates a harmonic torque $\tau_h$ that can be computed as follows [26]:

$$\tau_h \sin(h\omega t + \delta_h) = k\left[\Psi_1\left(I_{r,h-1} - I_{r,h+1}\right)\right]\sin(h\omega t) + \left[\Psi_{h-1} + \Psi_{h+1}\right] I_{r,1}\cos(h\omega t)] \quad (10)$$

where

$k$ motor constants;

$\delta_h$ phase angle at $h$ harmonic rank of the torque;

$\omega$ angular velocity.

Let us consider the first harmonic component of this SL [i.e., $h = 6$]. Therefore, the first term at the right side of (10) represents the interaction between the fundamental air-gap flux and the fifth and seventh harmonic ranks of current. Similarly, the second term on the right side of (10) represents the interaction between the fundamental current and the fifth and seventh harmonic flux. As a result, this interaction generates the harmonic torque $\tau_6$, which increases the losses, reduces the efficiency, and decreases the power quality of the motor. Therefore, it is crucial to study the limitations of the

**TABLE 4.** Switching Angles for 3-Phase, 3 Modules, 15-Level ACHB-MLI

| Switching angles | $\alpha_1$ | $\alpha_2$ | $\alpha_3$ | $\alpha_4$ | $\alpha_5$ | $\alpha_6$ | $\alpha_7$=$\alpha_\varkappa$ |
|---|---|---|---|---|---|---|---|
| SMT-SHE with Switching angle limitation | 3.577° | 12.256° | 13.528° | 23.4307° | 29.480° | 41.185° | 58.537° |
| SMT-SHE with Switching angle limitation | 8.623° | 10.317° | 24.525° | 33.546° | 45.545° | 1.642° | 87.468° |

MLI-based proposed structure, from two points of view, the validation of the THD recommendations, and the elimination of the predominant/specific harmonics for the three-phase industrial configurations.

In this context, let us consider the line voltage $u$ is expressed as $\vec{u} \in \{\vec{u}_{ab} = \vec{u}_a - \vec{u}_b,\ \vec{u}_{bc} = \vec{u}_b - \vec{u}_c,\ \vec{u}_{ca} = \vec{u}_c - \vec{u}_a\}$. This line voltage $u(\theta)$ as a function of angle $\theta$ is symmetrical, and evenly spaced with respect to $\pi/3$, if $u(\pi/3 + \theta) = u(\pi/3 - \theta)$, and for $\theta \in [0, \pi/3]$. In addition, $u(\theta)$ is a balanced three-phase system, if $\vec{u}_{ab} + \vec{u}_{bc} + \vec{u}_{ca} = 0$, for $\theta \in [0, 2\pi]$, while the triplen harmonics are automatically eliminated in this system [9].

To satisfy the balanced and symmetrical output voltages of the ACHB-MLI, let us consider the switching angles that correspond to the three-phase system $(a,b,c)$ as $\alpha_k, \alpha_\beta$, and $\alpha_\gamma$, where $k, \beta, \gamma \in [1, \ldots, \varkappa]$. In this three-phase configuration, the triplen harmonics are automatically eliminated, and the seven angles are precalculated to eliminate the predominant/lowest seven harmonic ranks, for instance, $\mathcal{H} = \{5, 7, 11, 13, 17, 19, 23\}$, while $M = 1$. These angles are shifted apart 120° per phase. Therefore, the switching angles' values of phase (a) have to lay in the interval $[0, \pi/3]$ to avoid simultaneous command of two sequenced phases, without a 120° phase shift, and to prevent the appearance of nonconventional harmonic components in the output voltage of the ACHB-MLI. However, one can impose the balancing constraint of the three-phase system within the time interval $[0, 2\pi/3]$ to solve (4), from a harmonic limitation standpoint, as follows:

$$\begin{aligned} &\alpha_{\min} \le \alpha_1 + \delta_{\min} \le \alpha_2 + \delta_{\min} \le \cdots 0 \le \alpha_\varkappa \\ &\qquad + \delta_{\min} \le \alpha_{\max} \\ &\alpha_{\min} = 0^\circ, \quad \alpha_{\max} = 60^\circ. \end{aligned} \quad (11)$$

Once again, the NR method is used iteratively to satisfy (9). As a result, almost complete elimination is obtained for the predominant $\varkappa$ harmonic ranks (for $M = 1$) of the line voltage $\vec{u}_{ab}$. The resulting switching angles needed to perform the SMT-SHE with switching angles limitation for the ACHB-MLI configured as {1:2:4} to generate 15 levels are shown in Table 4. It is important to mention that the switching angles of the second and third phases $\alpha_\beta$ and $\alpha_\gamma$ take $\alpha_k$ values with phase shifting of $-120°$ and $-240°$, respectively.

To evaluate the performance of the SMT-SHE approach, including switching angle limitation, on the ACHB-MLI, 15 levels, the resulting switching angles are compared with

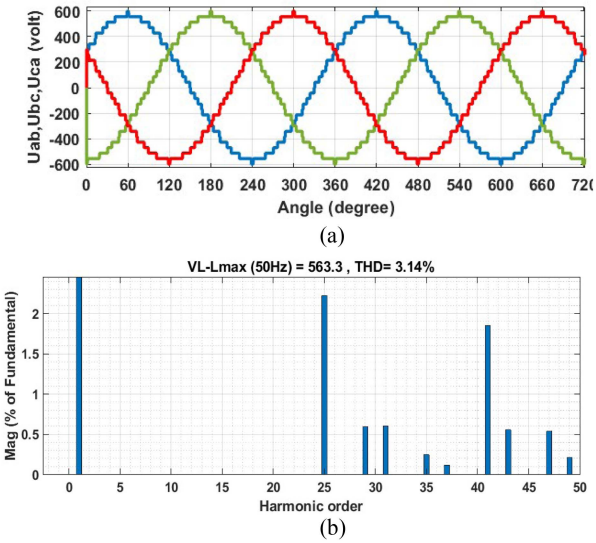


**FIGURE 5.** Line voltages $u_{ab}$, $u_{bc}$, and $u_{ca}$ using SMT-SHE with switching angle limitation (a) in the time domain and (b) $u_{ab}$ voltage in the frequency domain.

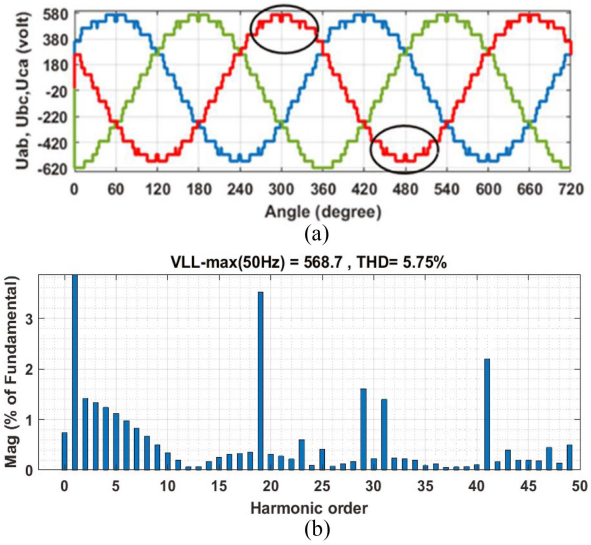


**FIGURE 6.** Line voltages $u_{ab}$, $u_{bc}$, and $u_{ca}$ using SMT-SHE without switching angle limitation (a) in the time domain and (b) $u_{ab}$ voltage in the frequency domain.

those obtained without switching angle limitation, as defined in Table 4.

It is evident that the switching angles for the three-phase system were simultaneously triggered. Therefore, when the maximum switching angle exceeds 60° in each quarter cycle, two sequenced phases, without a 120° phase shift, will experience simultaneous command during a time interval of $(\alpha_{\max} - 60)$.

Indeed, the simultaneous *L–L* command occurs during the two intervals $(\alpha_6 - 60)$ and $(\alpha_7 - 60)$ (see Table 4). This results in an unbalanced voltage system and, thus, a negative voltage sequence, inversely proportional to the angle differences of $(\alpha_{\max} - 60)$, along with other related nonconventional disturbing components that might be appeared.

To quantify the impact of the switching angles on the SMT-SHE/ACHB structure performance, Fig. 5(a) and (b) shows the (a) three-phase line voltages in the time domain as well as the (b) line voltage $u_{ab}$ in frequency domain for the two cases, with and without switching angle limitation, respectively.

From Fig. 6(a), it is clear that the SMT-SHE with limitation results in an output line voltage that closely resembles a sinusoidal waveform with a THD of 3.14%, satisfying the IEEE-519-2014 norm. In addition, an almost complete elimination of the predominant/low harmonics rank in $\mathcal{H}$ is achieved.

On the contrary, the SMT-SHE approach without limitation causes a simultaneous *L–L* switching angle injection and generates, consequently, a negative-sequence voltage component (of 1.2% in this case) as well as even, zero, and dc disturbing voltage components, while amplification of the odd harmonics, as shown in Fig. 6(b). So, the output voltage waveform is no longer closed to sinusoidal, as shown in Fig. 6(a). This distorted waveform is confirmed by an increase of the voltage THD% up to 5.75% [see Fig. 6(b)]. It is worth noting that these additional disturbing voltage components have undesired consequences on the overall ac/dc/ac structure, including the supplied loads (i.e., magnetic circuits, rotating machines, protection systems, switching circuits, etc.).

### D. DC-LINK CAPACITORS RATING SELECTION

The capacitor rating of the ACHB-MLI structure requires to satisfy various contradictory constraints. Indeed, the capacitors must be high enough to maintain a constant dc voltage during transient consumption periods while limiting the ripple frequency of the dc voltage and, consequently, not degrading the load voltage THD. On the other hand, both economic and industrial approaches require limited values of capacitors.

A limited amount of research deals with the sizing of the capacitors in MLI structures. Indeed, in [11], the identical capacitor of 10 mF for each module of ACHB-MLI four modules was energized by an isolated master dc source and three modules were fed by three floating capacitors. However, this topology is designed to feed two typical loads with a power rating of 15 kW and an *R–L* value of 100 Ω, 80 mH, as well as the dc-voltage ripple set to ±10%. This relatively high ripple ratio and low connected loads make the capacitance value very large and unsuitable from the industrial perspective. Furthermore, in [23], the ACHB-MLI topology with 3 modules configured as [1:3:9] is utilized to generate 27 voltage levels, while each module is energized by a storage capacitor of 33 mF. This topology is designed to operate at MV network, with an output voltage of 3.3 kV, and is intended to supply a three-phase load with power rate of 100 kW.

In this research, the sizing of the dc-link capacitors $C_{\text{dc}}$ was determined by designing the minimum capacitance value required to attenuate the voltage ripple at the dc side of the

ACHB-MLI. The equivalent capacitance selection for each CHB module will correspond to the industrial demand. In this context, the following expression is derived and adapted to our study [24]

$$C_{dc} = \frac{\sqrt{2} \cdot I_{max} \cdot r}{8 \cdot \pi \cdot f_{grid} . \Delta V} \quad (12)$$

where $I_{max}$ denotes the peak value of the fundamental load current component, $\Delta V$ denotes the peak-to-peak voltage ripple, $f_{grid}$ denotes the fundamental frequency, and $r$ denotes the modulation depth (usually less than 0.90).

### E. SYNTHESIS OF THE PROPOSED SMT-SHE APPROACH FOR ACHB-MLI

The SHE-SMT algorithm proved its effectiveness to eliminate all the targeted harmonics to control the amplitude of the fundamental component, to reduce the number of the CHB modules, and to significantly reduce the harmonic distortion. Indeed, with only 3 cascaded H-bridge and 15 voltage levels, the THD voltage is 3.14% [see Fig. 5(b)]. Moreover, according to Table 1, the ACHB-MLI structure commanded by SMT technique requires at least four ACHB modules to reach a THD of 5.07% but with a high level of individual low rank/predominant harmonics' voltages. Indeed, the fifth individual harmonic rank ratio is 4.6%, as shown in Fig. 2(b), of the fundamental line voltage, which can greatly deteriorate the optimal operation of certain SLs, such as asynchronous motors. It is worth noting that, in the proposed SMT-SHE approach, the predominant low harmonic ranks are completely eliminated [see Fig. 5(b)].

Finally, for the MLI structures based on 4 ACHB modules and more, with a minimum of 21 voltage levels, the dc-side capacitors must be overrated. Indeed, according to [11], a set of 10 mF capacitors is necessary to supply a load of only 1.5 kW. Meanwhile, the new SMT-SHE, with 3 modules and 15 voltage levels, requires only 9 mF for an SL of 50 kW [see Section VI-C]. Meanwhile, Section IV-A compares SMT-SHE with other modulation techniques.

### F. COMPARISON STUDY OF THE PROPOSED SMT-SHE WITH OTHER MODULATION TECHNIQUES

To validate the proposed SMT-SHE approach, it should be compared with other algorithms, available in the literature, to prove its effectiveness across different design aspects, such as controlled structure, number of output level $L$, number of H-bridge modules $n$, number of phases, modulation index $M$, and harmonic distortion of the output stepping voltage $THD_v\%$, as shown in Table 5.

Apparently from Table 5, the ACHB topology controlled by SMT or SMT-SVM approach requires a higher output voltage level to reach the desired reduction of harmonic distortion. However, significant low dc voltages should be configured for the second and subsequent HB modules to avoid raising the number of HB modules, as defined by (2). The configuration of these low dc voltages requires higher capacitors, which limits the applicability of these approaches in real applications.

**TABLE 5. Comparison Among Different Algorithm Structures**

| Algorithm | Controlled topology | Network Type | n | L | M | Phase | $THD_v\%$ |
|---|---|---|---|---|---|---|---|
| SMT-SHE | ACHB | LV | 3 | 15 | 1 | 1 | 6.91% |
| SMT-SHE | ACHB | LV | 3 | 15 | 1 | 3 | 3.14% |
| SMT | ACHB | LV | 3 | 27 | 1 | 3 | 4.17% |
| SMT -SVM | ACHB | LV | 3 | 42 | 1 | 3 | 1.5 % |
| SMT -SVM | ACHB | MV | 4 | 31 | 1 | 3 | 2.75% |
| SHE-LSS | SCHB | LV | 4 | 9 | 1 | 1 | 10.89% |
| PAWM | SCHB | LV | 3 | 7 | 1 | 1 | 11.86%, |
| GA-PWM | SCHB | LV | 3 | 7 | 1 | 1 | >18% |

Moreover, the SCHB topology controlled by SHE-LSS, PAWM, or GA-PWM requires a higher number of HB modules to fulfill a wide spectrum elimination of the harmonic components from the output voltage. These approaches can mitigate one harmonic per module at the output voltage, except the SHE-LSS approach, where one of its HB modules can be set to mitigate a harmonic component with its multiples. As a result, these approaches present a high harmonic content on the output voltage.

The proposed SMT-SHE approach reduces the harmonic distortion of the output voltage to 3.14% with 3 HB modules configured to generate 15 levels. Furthermore, this approach grants mitigation a wide harmonic rank, including those affecting the performance of SL. Besides, it fulfills the industrial requirement of the dc links at the HB inputs by presenting an adequate capacitor size derived from the applied dc voltage and the capacitance rating.

## V. SAF DESIGN FOR THE PROPOSED AC/DC/AC STRUCTURE

SAF topology has recently gained widespread use in industrial and commercial applications. This topology is considered a real-time current compensator that is typically connected in parallel, on the perturbing/nonlinear load side, between the load and the grid [20], [21], [22], [23], [24], [26]. With appropriate control, it mitigates precisely undesired perturbations, such as harmonics, unbalanced conditions, and reactive power compensation on the grid side [26], [27].

### A. GENERAL STRUCTURE OF SAF

This filtration/compensation solution, associated with the classical ac/dc rectifier, is the alternative to the complex ac/dc active or simple rectifiers with passive filters [11], [13], [16]. Although the classical ac/dc rectifier is considered a polluting source of harmonics, it is, in addition to its economic aspect, very simple to install and maintain. Besides, active filters can be installed regardless of the load types and the perturbations to be eliminated; only their rated power must be a percentage of the perturbating loads [28]. SAF can compensate the perturbations caused by the nonlinear loads, particularly power electronics based loads, while continuously tracking their changes [24].

A typical SAF consists of two main parts (power and control part). The power part comprises a two-level voltage-source inverter (VSI), a dc capacitor storage system, and an

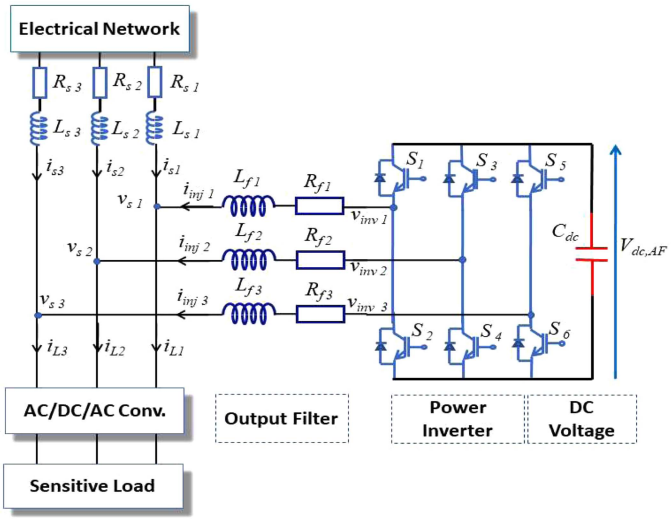


**FIGURE 7.** SAF structure: power part.

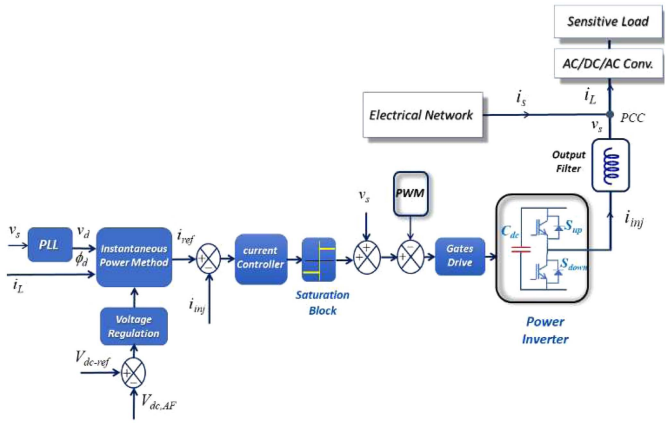


**FIGURE 8.** SAF structure: control part.

output filter, as illustrated in Fig. 7 [29]. Meanwhile, the typical control part relies on the identification of the perturbing load current and two control loops: an inner loop to compensate the perturbing currents into the grid and an outer loop to regulate the dc voltage across the storage capacitor, as well as a pulsewidth modulation (PWM), as depicted in Fig. 8. To configure the control strategy of the SAF, its instantaneous model should be defined at first.

### *B. INSTANTANEOUS MODEL AND CONTROL STRATEGY OF SAF*

The SAF structure includes the inverter with the downstream storage element and the upstream output filter.

In this context, a VSI is widely used; it is usually associated with a first-order output filter [29].

The first-order output filter, given by $L_f$ series inductor and $R_f$ internal resistance, is connected between the VSI and the grid to reduce the distortions of the injected current caused by the switching frequency.

Let us consider $i_{L,k}$, $i_{s,k}$, $v_{\text{inv},k}$, and $v_{s,k}$ denote the load current, source current, inverter output voltage, and the point of common coupling (PCC) voltage, respectively, where $k \in \{1,2,3\}$ represents the three phases. One can determine the injected current $i_{\text{inj},k}$ with respect to KCL as $i_{\text{inj},k} = i_{L,k} - i_{s,k}$ while its dynamic $i_{inj,k}$ is expressed as follows:

$$\dot{i}_{\text{inj},k} = \frac{1}{L_f}\left(v_{\text{inv},k} - v_{s,k}\right) - \frac{R_f}{L_f} i_{\text{inj},k}. \tag{13}$$

To describe the instantaneous model of the SAF, the power inverter of the SAF is composed of three legs, that is commanded by PWM to generate a three-phase voltage output $v_{\text{inv},k}$. The transistors in each leg ($S1/S2$, $S3/S4$, and $S5/S6$) operate in either an ON-state 1 or an OFF-state 0. The upper and lower transistors in each leg are operated complementary and phase shifted by 120°.

For simplicity, the upper and lower transistors are denoted as $S_{\text{up},k}$ and $S_{\text{down},k}$, respectively. According to this configuration, the output voltage of this power inverter can be calculated as follows [30]:

$$v_{\text{inv},k} = \left(S_{\text{up},k} - S_{\text{down},k}\right) V_{\text{dc}}. \tag{14}$$

By substituting (13) into (12), we find

$$\dot{i}_{\text{inj},k} = \frac{\left(S_{\text{up}} - S_{\text{down}}\right)}{L_f} v_{\text{inv},k} - \frac{1}{L_f} v_{s,k} - \frac{R_f}{L_f} \cdot i_{\text{inj},k}. \tag{15}$$

By neglecting the transistors switching losses, one can define the SAF capacitor current $I_{\text{dc}}$ based on the injected current and the associated transistors' states per leg, i.e., $I_{\text{dc}} = (S_{\text{up}} - S_{\text{down}}) i_{\text{inj},k}$.

Therefore, the voltage variations across the capacitor are expressed as follows:

$$\dot{v}_{\text{dc}} = \frac{1}{C_{\text{dc}}} \cdot I_c = \frac{\left(S_{\text{up}} - S_{\text{down}}\right)}{C_{\text{dc}}} \cdot i_{\text{inj},k}. \tag{16}$$

However, the instantaneous model of a classical SAF is expressed in the compact form as follows:

$$\begin{pmatrix} \dot{i}_{\text{inj},k} \\ \dot{v}_{\text{dc}} \end{pmatrix} = \begin{pmatrix} \frac{(S_{\text{up}} - S_{\text{down}})}{L_{f,k}} & -\frac{R_f}{L_f} \\ 0 & \frac{(S_{\text{up}} - S_{\text{down}})}{C_{\text{dc}}} \end{pmatrix} \cdot \begin{pmatrix} v_{\text{inv},k} \\ i_{\text{inj},k} \end{pmatrix} + \begin{pmatrix} -\frac{1}{L_f} \\ 0 \end{pmatrix} \cdot v_{s,k} \; k \in \{1, 2, 3\}. \tag{17}$$

To eliminate the load current perturbation, the SAF typically employs the instantaneous power method to identify the network perturbation current [31]. This method aims to determine the reference currents $I_{\text{ref},k}$ as input for the inner current control loop of the SAF. The identified current subtracted from the injected current is to define the current error, which is controlled using an appropriate controller. For this purpose, a proportional-integral (PI) controller can be utilized to control the injected current and track the desired reference current as follows:

$$v_{\text{inv},k} = k_{p,i}\left(i_{\text{ref},k} - i_{\text{inj},k}\right)$$

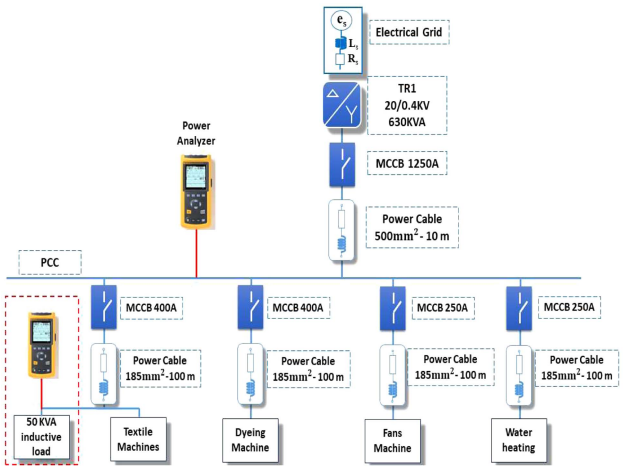


**FIGURE 9.** Power topology of the factory transformer TR1.

$$+ k_{i,i} \int \left(i_{\text{ref},k} - i_{\text{inj},k}\right).dt \tag{18}$$

where $k_{p,i}$,$k_{i,i} > 0$ are the PI gains. These gains are designed to ensure fast dynamics of the injected currents, as well as better performance tracking to the reference current $I_{\text{ref}}$. Furthermore, the SAF requires a voltage controller to eliminate the steady-state error of the capacitor voltage $V_{\text{dc}}$ and to maintain it constant around the desired reference voltage $V_{\text{dc}}^{*}$. In this article, a simple PI controller has two gains $k_{p,v}$ and $k_{i,v}$, which are suggested as follows:

$$I_{\text{dc}} = k_{P,v}\left(v_{\text{dc}}^{*} - v_{\text{dc}}\right) + k_{i,v}\int \left(v_{\text{dc}}^{*} - v_{\text{dc}}\right)\cdot dt. \tag{19}$$

## VI. EXPERIMENTAL RESULTS FOR REAL CASE STUDY

In this article, the proposed ac/dc/ac converter had been validated on a real industrial plant, a textile factory, located in the industrial city of Aleppo, Syria.

The electrical network of this factory is composed of three transformers (20/0.4 kV) fed by a 66/20 kV substation transformer. In this context, these transformers (TR$k$, $k$ = 1,2,3) have the following load types [32].

1) TR1: textile machine, ventilation fans, dyeing machine.
2) TR2: textile machine, ventilation fans, lighting system.
3) TR3: textile machine, ventilation fans.

The electrical loads of TR1 are considered the most important production line of this factory since any electrical failure in this line stops the production process of the remaining two production lines, powered by (TR2 and TR3). Therefore, special research is conducted on TR1, whose power topology is shown in Fig. 9.

Apparently, the TR1 network comprises four main parts: Grid, TR1, load power cable, and loads. The numerical implementation of these parts requires their electrical parameters. The parameters of the first three parts are determined by their nominal values, while real measurements are needed to determine the load characteristics and parameters. Let us consider

**TABLE 6.** Parameters of the Electrical Components

| *Electrical Network Parameters* | |
|---|---|
| $e_s, S_{cc}, R_{cc}, L_{cc}$ | 20 kV, 500 kVA, 0.253 Ω, 0.002415 H |
| Power Transformer TR1 | D11/Yn, 20/0.4 kV |
| $S_n, \Delta P_{cu}, \Delta P_{oc}, \mathrm{U}_{cc}, I_{oc}$ | 630 kVA, 6.5 kW, 1.3 kW, 4%, 1.6% |
| Main Power Cable | 3 x 500 mm2, L=10 meter |

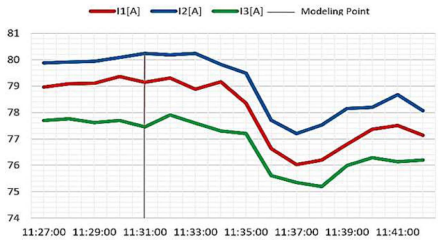


**FIGURE 10.** Currents at SL—50 kVA.

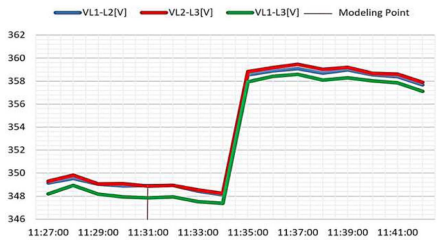


**FIGURE 11.** Line voltages at SL—50 kVA.

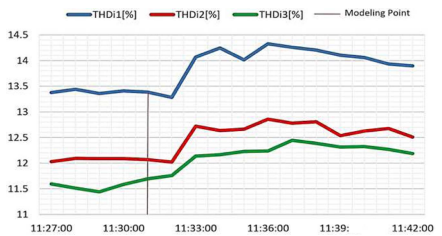


**FIGURE 12.** THD$_i$ at SL—50 kVA.

that $e_s$ denotes the grid line voltage, one can express the short-circuit grid model as $S_{cc}$, $R_{cc}$, and $L_{cc}$, which represents the apparent power, resistance, and inductance of the grid, respectively.

The TR1 primary/secondary windings' voltages are 20/0.4 kV, these windings are connected in delta/star (D11/Yn) and their parameters $S_n$, $\Delta P_{cu}$, $\Delta P_{oc}$, $U_{cc}$, and $I_{oc}$ denote the nominal apparent power, copper losses, iron losses, magnetic power losses, short-circuit voltage, and open-circuit current, respectively. The load power cable parameters are the cable section and length. Table 6 illustrates the nominal value of the grid, TR1, and load cable as follows.

Due to the high amount of TR1 loads, it is difficult to investigate their individual load parameters. However, a power analyzer instrument is used to precisely assign the TR1 load state. Two real measurements were executed. The first

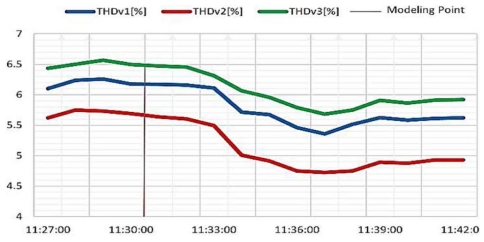


**FIGURE 13.** THD$_v$ at SL—0 kVA.

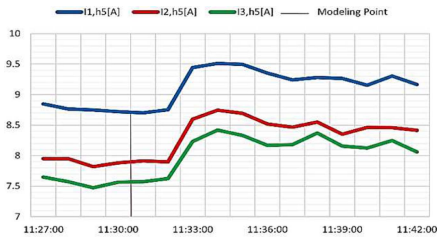


**FIGURE 14.** Fifth current component SL—50 kVA.

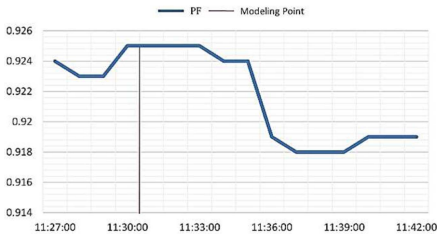


**FIGURE 15.** PF at SL—50 kVA.

measurement was conducted at the PCC, which reflects the full-load state of TR1, whereas the second was measured at the terminals of a sensitive textile machine with a nominal power rate of 50 kVA. The duration of the first and second measurements was taken from 4:19 A.M. to 11:28 A.M., and from 11:27 A.M. to 11:42 A.M., respectively. Figs. 10–15 show the electrical measurements at the SL terminals, including the line currents $I_k$, line voltages $V_{LL}$, THD of the current and the voltage (THD$_{ik}$ - THD$v_k$), power factor (PF), and fifth current components $I_{k,h5}$. It is important to note that the induction/asynchronous motor of the SL had already been fed by a classical ac/dc/ac converter.

These real measurements enable us to implement numerically the linear and nonlinear parts of loads. To evaluate the load performance, the most distorted operating point is considered, which is so-called the "modeling point." This point is selected to correspond to the maximum THD of the SL load voltage. Therefore, one can create the SL numerical model at measurement time 11:31 A.M., while the TR1 load can be modeled at 10:38 A.M. Table 6 summarizes the electrical quantities corresponding to these two measurement times.

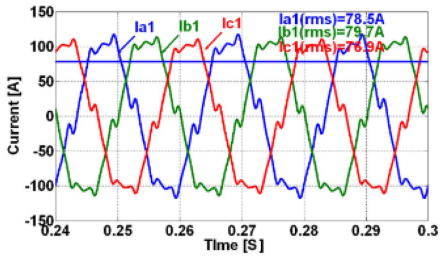


**FIGURE 16.** SL current $i_{SL,a,b,c}$.

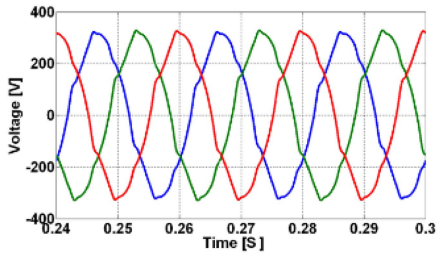


**FIGURE 17.** Phase voltage $v_{SL,a,b,c}$.

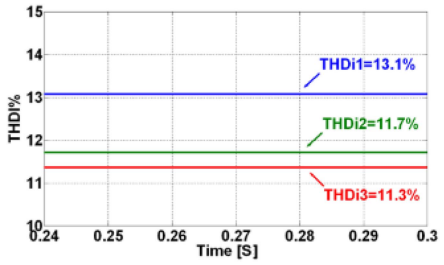


**FIGURE 18.** THD$i_{SL,a,b,c}$%.

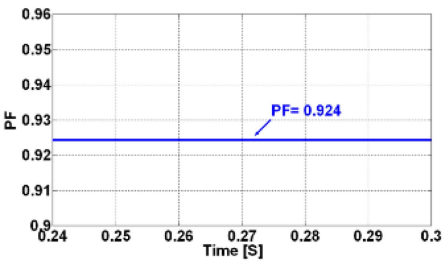


**FIGURE 19.** PF at SL.

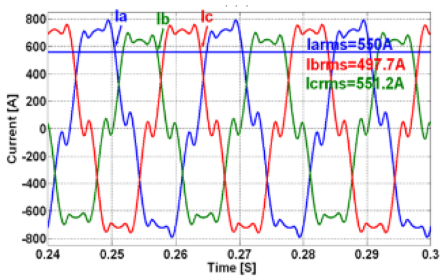


**FIGURE 20.** TR1 full-load currents.

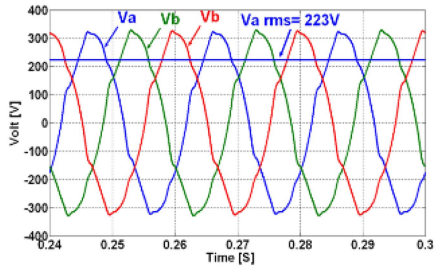


**FIGURE 21.** PCC phase voltages.

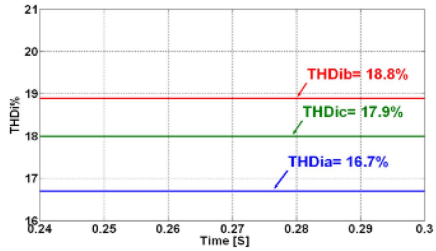


**FIGURE 22.** THD$i$% for the PCC.

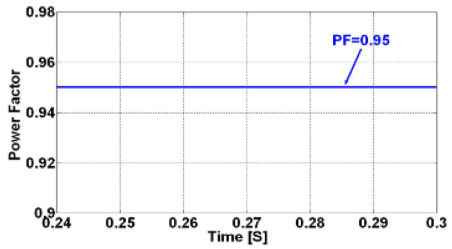


**FIGURE 23.** PF for the PCC.

After setting the parameters of the TR1 network, one can create its numerical model using MATLAB/Simscape Electrical. To set up the simulation parameters of this model, the Euler solver method is used at sampling time $T_s = 1\ \mu$s [33]. These results represent the time-domain analysis of the SL load, such as the phase voltages $v_{SL}$, line currents $i_{SL}$, the PF, and the THD$i_{SL}$, which are depicted in Figs. 16–19. However, the same analysis for the TR1 load at PCC is shown in Figs. 20–23. To address the accuracy of the TR1 model, a comparison is made between the results obtained using the suggested model and the real measurement at the corresponding measuring time in the effective values. One finds that the accuracy ratio of the PCC load model ranges from 92.2% to 100%, while it ranges for the SL load model from 91.1% to 99.3%.

### A. INTEGRATION OF THE PROPOSED AC/DC/AC STRUCTURE TO SUPPLY SL

This article investigates the performance of the proposed ac/dc/ac converter that employs three ACHB modules as a power MLI inverter for the SL within TR1 network. This converter structure is designed to reduce the THD of the output line voltage to less than 3% at the load side by employing the novel modulation approach SMT-SHE. The ac/dc part of the converter is accomplished by combining a simple ac/dc rectifier for each module and a multiwinding transformer. This combination provides the desired asymmetrical dc voltages for the inverter modules. Furthermore, an SAF is utilized to mitigate perturbing harmonics at the grid side. Fig. 24 illustrates the power plan for the TR1, which highlights the integration of the ac/dc/ac converter on the SL side. It is important to highlight that the SHE-SMT approach might be configured to change the rotation direction of the SL instead of switching two phases at the SL terminals. To address this phase changing by the SHE-SMT algorithm, the switching angles of ACHB modules of phase $A$ should be shifted 120°, while the switching angles of ACHB modules of phase $B$ are triggered with zero shifting.

**TABLE 7.** Triggering Angles for a 17-Level ACHB-MLI for SL Load

| $\alpha_1$ | $\alpha_2$ | $\alpha_3$ | $\alpha_4$ | $\alpha_5$ | $\alpha_6$ | $\alpha_7$ | $\alpha_8$=$\alpha_\mu$ |
|---|---|---|---|---|---|---|---|
| 2.726° | 11.206° | 11.206° | 19.175° | 25.177° | 31.879° | 42.246° | 58.566° |

### B. CONFIGURATION OF THE ACHB-MLI FOR SL

In this real case study, the three modules, ACHB-MLI will be commanded by SMT-SHE approach. The objectives of this modulation approach are to reduce the number of structure modules, voltage levels, the THD, and the harmonic content of the output voltage while limiting the dc-side capacitors' ratings. Therefore, taking into account the high power/current to be supplied to the SL, with the required high-power quality of the load voltage, the 3 modules, ACHB–MLI configured their dc voltages as {1:2:5} to generate 8 voltage steps per quarter cycle and 17 voltage levels at the SL terminal. This configuration can mitigate up to eight predefined low-order/specific harmonics. Therefore, the targeted harmonic ranks are $\mathcal{H}$ =[5th, 7th, 11th, 13th, 17th, 19th, 23rd, and 27th], which include those undesirables by such an asynchronous motor [19]. Since the SL is a three-phase balanced load, the triplen harmonics disappear at the voltage terminals.

The novel modulation approach (SHE-SMT) is used to mitigate the undesired harmonics by computing and optimizing the relevant switching angles that correspond to the selected harmonic rank.

These switching angles were limited to $\pi/3$ to prevent negative sequence as well as nonconventional harmonics from appearing on the SL side and to prevent the amplifications of the odd harmonics (see Section VI-C).

Table 7 summarizes the switching angles for the 17-level ACHB-MLI, with switching angle limitation to satisfy the ideal balanced three-phase system. It is important to note that one of the SHE-SMT advantages is its ability to calculate the switching angles offline using quarter-wave symmetry [38]. Therefore, one can calculate and equip the switching angles

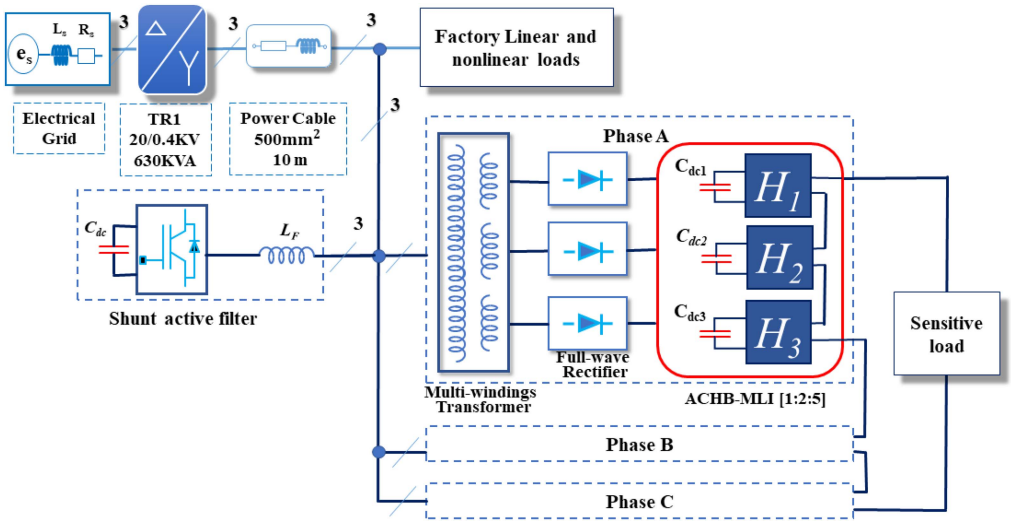


**FIGURE 24.** Power diagram for TR1 with the SL supplied through ac/dc/ac–ACHB-MLI converter.

for the ACHB-MLI at different harmonics' ranks and modulation index for the controlled SL.

### C. DC CAPACITORS RATING OF THE PROPOSED AC/DC/AC STRUCTURE

To determine the appropriate capacitor rating for each of the three modules, two main factors should be considered. First, the dc voltage $V_{\text{dc}}$ of each module's capacitor should correspond to the relevant dc configuration {1:2:5}. Second, the capacitors should be rated without degrading the power quality at the load side, as well as being applicable from an industrial point of view. The nominal phase voltage of the SL is $v_1 = 230$, which is ensured by a unity modulation index. Therefore, one can calculate the capacitance $C_{\text{dc}}$ needed for each module per phase using the following notation:

$$C_{\text{dc}} = \frac{\sqrt{2} \cdot I_{\max} \cdot r}{8 \cdot \pi \cdot f_{\text{grid}} \cdot \Delta V} = \frac{\sqrt{2} * \left(\sqrt{2} * 79.139\right) * 0.7}{8 * \pi * 50 * \left(230 * \sqrt{2} * 3\%\right)}$$

$$= \frac{110.79}{8174.9} = 9.035 \text{ mF}. \quad (20)$$

This capacitance is selected for SL load with a power rating of 47.306 kVA, as demonstrated in Table 6, and a voltage ripple of 3%. Clearly, this value is fulfilled with industrial requirements as compared with 10 mF with 15 voltage levels, 3 modules, which feed small load lower than 1.5 kW and voltage ripple of ±10% [11].

After assigning the dc capacitors, one can analyze the performance of the 17-level, 3 modules per phase, ACHB-MLI, which feeds within real factory environment. Figs. 25 and 26 show the SL line voltage $v_s$ in the time and frequency domains, and Fig. 27 shows the dc voltages across the capacitors of the three modules connected on phase $a$. However, Fig. 28 shows the grid current of SL in time domain.

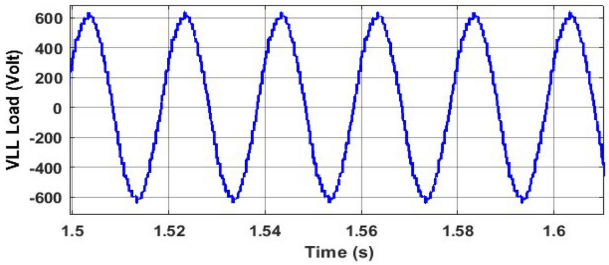


**FIGURE 25.** Line voltage $v_s$ of SL (in time domain).

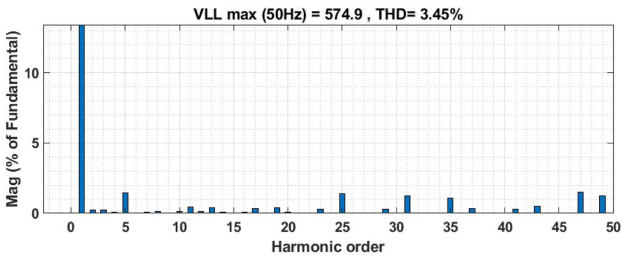


**FIGURE 26.** Line voltage $v_s$ of SL (in frequency domain).

We effectively noticed from the numerical simulation results that the predefined low harmonics' ranks [5th, 7th, 11th, 13th, 17th, 19th, 23rd, and 27th] of the output line voltage applied to SL are almost eliminated and the line voltage in the time domain is closer to the sinusoidal waveform.

Besides, the THD of the voltage is equal to $\text{THD}_v\% = 3.45\%$, which is complied with IEEE-519 norm below 5%. Moreover, the dc voltages across the capacitors track their references of $[V_{\text{dc},1}, V_{\text{dc},2}, V_{\text{dc},3}] = [200,80,40]$, which correspond the desired configuration {1:2:5} to satisfy the required voltage level and a ripple ratio less than 3%. This harmonic reduction to 3.45% under dc-voltage fluctuation of

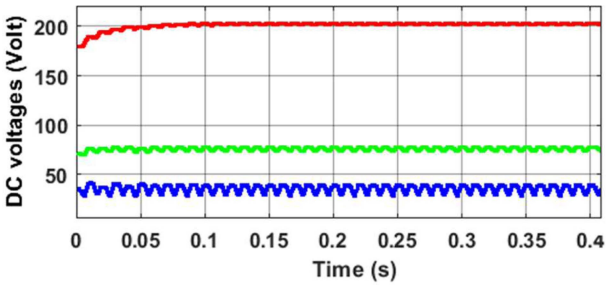


**FIGURE 27.** DC voltage across the three capacitors $V_{dc,1}$, $V_{dc,2}$, and $V_{dc,3}$.

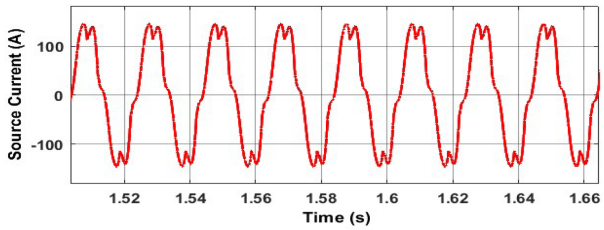


**FIGURE 28.** Source current at grid side is in time domain.

**TABLE 8.** Rated Element Values of the SAF

| | |
|---|---|
| Output filter: ($L_{f,1}$ -$R_{f,1}$),($L_{f,2}$ - $R_{f,2}$) | (0.4 mH -0.005 ohm), (0.8 mH-0.005 ohm) |
| Storage element: $V_{dc,AF}$ $C_{dc}$ | 840V, 0.9 mF |
| Switching frequency: $f_{sw}$ | 12.5 kHz |

3% proves a high filtration performance of the SHE-SMT algorithm for controlling the SL using the ACHB-MLI.

Finally, the SL grid-side current ($I_s$-SL) is quite far from a sinusoidal shape with THD$i_s$% of 13.58% (see Fig. 28 and Table 7). These perturbing current harmonics propagate to the mains and distort the voltage of other consumers supplied by the same grid. Therefore, the SAF is recommended here to cancel out these perturbations and improve the power quality on the grid side of TR1. It is worth noting that the SL can be completely isolated from the perturbing voltage and current of the grid using a series active filter, which is more complicated to design, install, and protect than an SAF, with an oversizing also [34], [35].

### D. DESIGNING AND INTEGRATING THE SAF

In this article, the SAF is added to eliminate, on the grid side, the harmonic currents and, consequently, harmonic voltage that are caused by the full-wave rectifiers. Indeed, the grid current of the proposed ac/dc/ac structure contains obvious harmonics that are produced due to the existence of the power electronics' devices and its THD is equal to 13.58%. Therefore, we suggested that the SAF eliminates its harmonic contents. Table 8 gives the element values of the employed SAF.

It is important to note that, in this real case study, the method of instantaneous real and imaginary powers is used to identify current perturbations, such as harmonics, unbalance, and reactive power [31]. In this context, a phase-locked loop

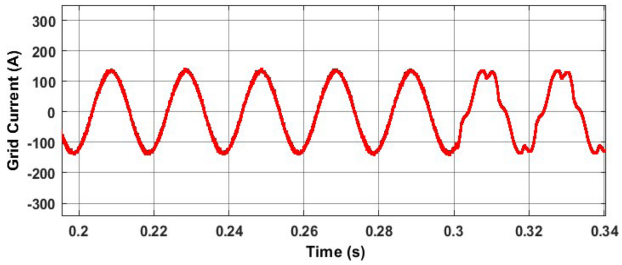


**FIGURE 29.** After and before integrating SAF—Lf,1.

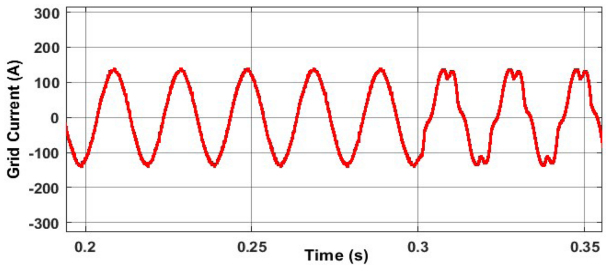


**FIGURE 30.** After and before integrating SAF—Lf,2.

is integrated into this method to obtain a reliable identification result, even in distorted PCC voltage conditions [29], as shown in Fig. 8. In addition, two PI-based control loops were used for the injected current control $I_{inj}$ and for dc-side voltage ($V_{dc}$) regulation and stabilization. PI controllers' parameters were carefully selected to provide robust, fast, and accurate tracking between $I_{inj}$ and $I_{ref}$ as well as $V_{dc,AF}$ and $V_{dc\text{-}ref}$ for current control and dc-voltage regulation loops, respectively [36].

The performance of this SAF was tested and validated using two different values of the coupling inductor, $L_{f,1} = 0.4$ mH and $L_{f,2} = 0.8$ mH. The purpose of using these inductors was to ensure that the switching components were significantly attenuated while maintaining good dynamics of the SAF. Figs. 29 and 30 show the time-domain grid current $i_s$ before and after the SAF activation for $L_{f,1}$ and $L_{f,2}$, respectively. The grid current becomes relatively sinusoidal for both inductor values, after SAF activation, indicating a significant improvement in the current waveform. This improvement contributed to the THD reduction from 13.38% without filtering to 2.38%–1.74% with filtering for $L_{f,1}$ and $L_{f,2}$, respectively, as shown in Figs. 31 and 32. In fact, this SAF satisfies high-power quality with respect to the IEEE-519 norm at the grid side, even with a relatively low inductance of the coupling filter. However, the proposed ac/dc/ac structure presents a high-power efficiency of 95.7% for feeding the SL of 50 kVA.

Finally, adding one or more SAFs to the ac/dc/ac structure implies additional cost, knowing that the overall cost and the filtering quality depend on the number and the layout emplacement of the SAFs installed in the industrial site. Indeed, Sheebi et al. [37] have shown that adding one active filter

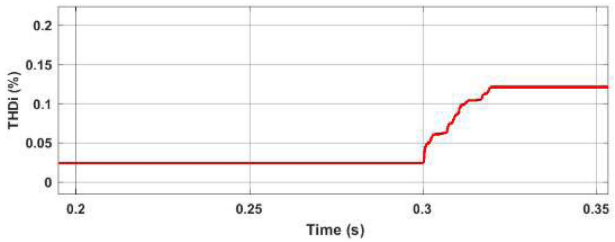


**FIGURE 31.** THD*is*% after and before integrating SAF—Lf,1.

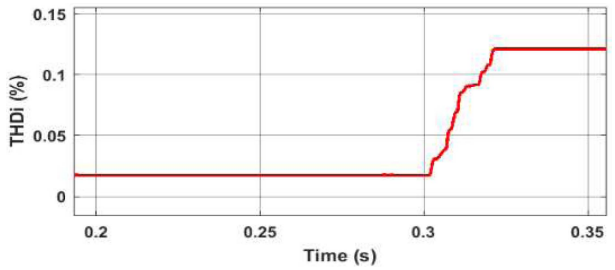


**FIGURE 32.** THD*is*% after and before integrating SAF—Lf,2.

for a set of polluting loads results in more economical with better filtration quality than coupling one active filter for each polluting load. It is worth noting that the rated power of an SAF is 30% of the polluting load.

### *F. POWER LOSSES CALCULATION USING MATLAB AND PLECS PROGRAMS*

The power losses of the ACHB-MLI structure controlled by SMT-SHE vary among the HB modules due to the various power contributions of each module. In the 3-module,17-level ACHB-MLI structure proposed for the factory network, we choose the IGBT device IKQ100N60TA with current and voltage rating of 160 A and 600 V, respectively; it corresponds to the 50 kVA protected load. Thus, the power loss calculation of the entire 17-level ACHB-MLI structure can be calculated based on the conduction and switching losses. It is worth noting that the conduction losses are mainly caused by the conduction resistance of both IGBT and its antiparallel diode, while the switching losses depend on the thermal characteristics of the IGBT device, as demonstrated in [39]. Based on the specifications given by IGBT datasheet, the conduction loss of the studied structure, using the MATLAB program, is 711.3 W; this value only represents the conduction losses and does not include the switching losses.

In order to calculate both losses, this article proceeded to model the dc/ac part of the overall structure using PLECS program, which can be installed within MATLAB. The advantage of PLECS software is the ability to calculate both power losses, including the switching one, even for real power electronics' components. As a result, conduction and switching losses, given by PLECS, are 713 W and 4.7 W, respectively. This result is in concordance with this obtained by MATLAB program, with an error ratio of 0.23%. Besides, one can observe the relatively low switching losses caused by switching frequency corresponding to the fundamental frequency of the grid.

It is important to emphasize that the maximum voltage stress experienced by an IGBT device of the proposed structure is, in our case study, 200 V. Indeed, the applied voltage levels on the first, second, and third HB modules are 200 V, 80 V, and 40 V, respectively, for each phase. Additionally, the IGBTs' devices of the three HB modules experience identical current stresses of 105.5 A, which represents the maximum value of the load current [2].

## VII. CONCLUSION

In this article, an advanced ac/dc/ac converter is proposed for harmonic reduction at both ac sides. The ac load side was conducted based on $n$ modules of ACHB-MLI that are commanded through a novel modulation approach called SMT-SHE, whereas the ac-side structure was built using simple conventional rectifiers combined with only one SAF.

The proposed SMT-SHE modulation approach aims to reduce the THD ratio of voltage, eliminate wide specific/predominant harmonic band at the load side, and command the output voltage amplitude, using a minimum number of CHB modules with appropriate output voltage level and lower industrial rating of the dc-side capacitors. The principle and the mathematical algorithm of SMT-SHE were explained in detail. First, for single-phase application, this combined approach exhibits its effectiveness to provide an output/load voltage closer to sinusoidal using the SMT technique, calculate the suitable switching angles of the SHE algorithm, eliminate the predefined harmonic rank, and control the fundamental component of the output inverter voltage using the modulation index. Second, this algorithm was extended to include the three-phase applications; the SMT-SHE approach with switching angle limitation was defined to prevent the simultaneous activation of two sequenced phases. This *L–L* simultaneous command leads to generating negative and dc components as well as even and zero harmonic ranks while amplifying the conventional odd harmonics.

In this context, the simulation results of the SMT-SHE-based ACHB-MLI showed a voltage harmonic distortion reduction to 3.4514%, while minimizing the CHB module number to 3, for an appropriate voltage level equal to 17.

Another challenge is to energize such an MLI structure from the grid using a simple/conventional ac/dc rectifier structure free of harmonics at the grid side. Therefore, a combination of multiwinding transformers associated with the conventional diode rectifier for each module per phase is set up. In addition, to mitigate the harmonic impact of these rectifiers on the grid, the SAF solution was introduced.

Furthermore, the proposed ac/dc/ac structure was tested and validated within a real industrial network, where real measurements were taken for the textile factory whose electrical network model was proposed and validated. Then, the proposed SMT-SHE-based ACHB-MLI, including the SAF, was

applied to an SL (textile machine: asynchronous motor drive) with a nominal power rate of 50 kVA. In fact, any power interruption of this load results in stopping the entire production line. The real simulation results proved the effectiveness and reliability of the proposed structure to significantly mitigate the harmonic components at both ac sides with a minimum number of load-side inverter modules and a noncomplicated ac/dc structure, while guaranteeing industrial values of dc bus capacitors. In this context, only 3 CHBs and 17 voltage levels using the proposed SMT-SHE combined approach with switching angle limitation allowed sinusoidal load voltage with 3.45% of THD. Also, an almost total elimination of the predominant/specific harmonics' ranks [5th, 7th, 11th, 13th, 17th, 19th, 23rd, and 27th], including the undesired ones of the SL, was achieved while limiting the dc bus capacitors' values to 9.035 mF.

Finally, using a conventional full-bridge diode rectifier combined with a three-phase SAF on the grid side, the THD of the grid current was reduced from 13.58% to 2.38%–1.74%, which corresponds to two suggested values of the coupling/output filter of $L_{f,1} = 0.4$ mH and $L_{f,2} = 0.8$ mH, respectively.

## REFERENCES


[1] A. H. Bonnett, "Analysis of the impact of pulse-width modulated inverter voltage waveforms on AC induction motors," *IEEE Trans. Ind. Appl.*, vol. 32, no. 2, pp. 386–392, Mar./Apr. 1996, doi: 10.1109/28.491488.

[2] H. Akagi, S. Inoue, and T. Yoshii, "Control and performance of a transformerless cascade PWM STATCOM with star configuration," *IEEE Trans. Ind. Appl.*, vol. 43, no. 4, pp. 1041–1049, Jul./Aug. 2007, doi: 10.1109/TIA.2007.900487.

[3] H. S. Patel and R. G. Hoft, "Generalized techniques of harmonic elimination and voltage control in thyristor inverters: Part I—Harmonic elimination," *IEEE Trans. Ind. Appl.*, vol. IA-9, no. 3, pp. 310–317, May 1973, doi: 10.1109/TIA.1973.349908.

[4] C. Buccella, C. Cecati, M. G. Cimoroni, and K. Razi, "Analytical method for pattern generation in five-level cascaded H-bridge inverter using selective harmonic elimination," *IEEE Trans. Ind. Electron.*, vol. 61, no. 11, pp. 5811–5819, Nov. 2014, doi: 10.1109/TIE.2014.2308163.

[5] C. Buccella, M. G. Cimoroni, and C. Cecati, "Selective harmonics elimination for nine level inverter based on linear system solution," in *Proc. 2nd IEEE Int. Conf. Ind. Electron. Sustain. Energy Syst.*, 2020, pp. 137–141, doi: 10.1109/IESES45645.2020.9210691.

[6] M. T. Hagh, H. Taghizadeh, and K. Razi, "Harmonic minimization in multilevel inverters using modified species-based particle swarm optimization," *IEEE Trans. Power Electron.*, vol. 24, no. 10, pp. 2259–2267, Oct. 2009, doi: 10.1109/TPEL.2009.2022166.

[7] B. Ozpineci, L. M. Tolbert, and J. N. Chiasson, "Harmonic optimization of multilevel converters using genetic algorithms," *IEEE Power Electron. Lett.*, vol. 3, no. 3, pp. 92–95, Sep. 2005, doi: 10.1109/LPEL.2005.856713.

[8] C. Buccella, M. G. Cimoroni, M. Tinari, and C. Cecati, "A new pulse active width modulation for multilevel converters," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7221–7229, Aug. 2019, doi: 10.1109/TPEL.2018.2878967.

[9] M. Sharifzadeh, H. Vahedi, R. Portillo, L. G. Franquelo, and K. Al-Haddad, "Selective harmonic mitigation based self-elimination of triplen harmonics for single-phase five-level inverters," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 86–96, Jan. 2019.

[10] T. D. C. Busarello, A. L. de Sousa Marcondes Reuter, A. Peres, and M. G. Simões, "Understanding the staircase modulation strategy and its application in both isolated and grid-connected asymmetric cascaded H-bridge multilevel inverters," *IEEE Trans. Ind. Appl.*, vol. 55, no. 5, pp. 5371–5382, Sep./Oct. 2019, doi: 10.1109/TIA.2019.2927189.

[11] R. Vasu, S. K. Chattopadhyay, and C. Chakraborty, "Asymmetric cascaded H-bridge multilevel inverter with single DC source per phase," *IEEE Trans. Ind. Electron.*, vol. 67, no. 7, pp. 5398–5409, Jul. 2020, doi: 10.1109/TIE.2019.2934080.

[12] Z. Ni et al., "A new approach to input filter design for regenerative cascaded H-bridge drives," *IEEE Trans. Ind. Electron.*, vol. 69, no. 4, pp. 3266–3277, Apr. 2022, doi: 10.1109/TIE.2021.3071694.

[13] J.-M. Yoo, H.-S. Jung, and S.-K. Sul, "Control strategy of DC-link voltage for single-phase back-to-back cascaded H-bridge inverter for MV drive with interfacing transformer having tertiary winding," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 8190–8200, Aug. 2019.

[14] F. Khoucha, S. M. Lagoun, K. Marouani, A. Kheloui, and M. E. H. Benbouzid, "Hybrid cascaded H-bridge multilevel-inverter induction-motor-drive direct torque control for automotive applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 3, pp. 892–899, Mar. 2010.

[15] M. A. E. Alali, Y. B. Shtessel, J.-P. Barbot, and S. Di Gennaro, "Sensor effects in LCL-type grid-connected shunt active filters control using higher-order sliding mode control techniques," *Sensors*, vol. 22, no. 19, 2022, Art. no. 7516. [Online]. Available: https://www.mdpi.com/1424-8220/22/19/7516

[16] P. Lezana, J. Rodriguez, and D. A. Oyarzun, "Cascaded multilevel inverter with regeneration capability and reduced number of switches," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1059–1066, Mar. 2008.

[17] S. D. T. Robertson and K. M. Hebbar, "Torque pulsations in induction motors with inverter drives," *IEEE Trans. Ind. Gen. Appl.*, vol. IGA-7, no. 2, pp. 318–323, Mar. 1971, doi: 10.1109/TIGA.1971.4181297.

[18] A. Madani, J. P. Barbot, F. Colamartino, and C. Marchand, "Reduction of torque pulsations by inductance harmonics identification of a permanent-magnet synchronous machine," in *Proc. Int. Conf. Control Appl.*, 1995, pp. 787–792.

[19] A. Tripathi and G. Narayanan, "Evaluation and minimization of low-order harmonic torque in low-switching-frequency inverter-fed induction motor drives," *IEEE Trans. Ind. Appl.*, vol. 52, no. 2, pp. 1477–1488, Mar./Apr. 2016, doi: 10.1109/TIA.2015.2487447.

[20] T. D. C. Busarello, A. Mortezaei, H. K. M. Paredes, A. Al-Durra, J. A. Pomilio, and M. G. Simões, "Simplified small-signal model for output voltage control of asymmetric cascaded H-bridge multilevel inverter," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 3509–3519, Apr. 2018, doi: 10.1109/TPEL.2017.2704919.

[21] S. K. Chattopadhyay and C. Chakraborty, "Performance of three-phase asymmetric cascaded bridge (16: 4: 1) multilevel inverter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 10, pp. 5983–5992, Oct. 2015, doi: 10.1109/TIE.2015.2424191.

[22] M. Ahmed, A. Sheir, and M. Orabi, "Real-time solution and implementation of selective harmonic elimination of seven-level multilevel inverter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 4, pp. 1700–1709, Dec. 2017.

[23] R. Vasu, S. K. Chattopadhyay, and C. Chakraborty, "Three-phase trinary asymmetric multilevel inverter with single DC source and open-loop control," *IEEE Open J. Ind. Appl.*, vol. 2, pp. 259–277, Aug. 2021, doi: 10.1109/OJIA.2021.3105605.

[24] M. A. E. Alali, Z. Sabiri, Y. B. Shtessel, and J.-P. Barbot, "Study of a common control strategy for grid-connected shunt active photovoltaic filter without DC/DC converter," *Sustain. Energy Technol. Assessments*, vol. 45, 2021, Art. no. 101149, doi: 10.1016/j.seta.2021.101149.

[25] M. A. E. Alali, Y. B. Shtessel, and J.-P. Barbot, "Grid-connected shunt active LCL control via continuous sliding modes," *IEEE/ASME Trans. Mechatronics*, vol. 24, no. 2, pp. 729–740, Apr. 2019, doi: 10.1109/TMECH.2019.2896140.

[26] M. Machmoum, N. Bruyant, S. Saadate, and M. A. E. Alali, "Stratégies de dépollution active des réseaux electriques Partie I : Commande généralisée et analyse de performances d'un compensateur actif parallèle," *Revue Internationale de Génie Electrique*, vol. 4, no. 3/4, pp. 293–316, 2001, doi: 10.3166/rige.4.293-316.

[27] M. A. E. Alali and J.-P. Barbot, "A first order sliding mode controller for grid connected shunt active filter with a LCL filter," *IFAC-PapersOnLine*, vol. 50, pp. 14812–14817, 2017, doi: 10.1016/j.ifacol.2017.08.2563.

[28] M. A. E. Alali, S. Saadate, Y.-A. Chapuis, and F. Braun, "Energetic study of a shunt active conditioner compensating current harmonics, power factor and unbalanced current," in *Proc. EPE-PEMC*, Kosic, Slovak Republic, 2000, pp. 211–216.

[29] H. Akagi, "New trends in active filters for power conditioning," *IEEE Trans. Ind. Appl.*, vol. 32, no. 6, pp. 1312–1322, Nov./Dec. 1996.
[30] S. Rahmani, A. Hamadi, and K. Al-Haddad, "A Lyapunov-function-based control for a three-phase shunt hybrid active filter," *IEEE Trans. Ind. Electron.*, vol. 59, no. 3, pp. 1418–1429, Mar. 2012, doi: 10.1109/TIE.2011.2163370.
[31] H. Akagi, Y. Kanazawa, and A. Nabae, "Generalized theory of the instantaneous reactive power in three-phase circuits," in *Proc. Int. Power Electron. Conf.*, 1983, pp. 1375–1386.
[32] G. Mokl and M. A. E. Alali, "Modeling and simulation of a universal series active filter to eliminate all voltage disturbances in electrical networks (case study in industrial site)," *Res. J. Aleppo Univ., Eng. Sci. Ser.*, vol. 109, 2013, Art. no. 637.
[33] N. Karania and M. A. E. Alali, "Nonlinear control by hysteresis of the parallel active filters (optimization, comparative study with PWM, case study in industrial site)," *Res. J. Aleppo Univ., Eng. Sci. Ser.*, vol. 84, pp. 275–296, 2010.
[34] M. A. E. Alali, S. Saadate, M. Machmoum, and N. Bruyant, "Stratégies de dépollution active des réseaux electriques—Partie II: Compensateur actif série d'harmoniques, de déséquilibre et de creux de tension des réseaux electriques," *Revue Internationale de Génie Electrique*, vol. 4, no. 3/4, pp. 317–332, 2001.
[35] M. A. E. Alali, S. Saadate, Y. A. Chapuis, and F. Braun, "Energetic study of a series active conditioner compensating voltage dips, unbalanced voltage and voltage harmonics," in *Proc. IEEE 7th Int. Power Electron. Congr. Tech.*, Acapulco, Mexico, 2000, pp. 80–86.
[36] S. Rahmani, A. Hamadi, K. Al-Haddad, and L. A. Dessaint, "A combination of shunt hybrid power filter and thyristor-controlled reactor for power quality," *IEEE Trans. Ind. Electron.*, vol. 61, no. 5, pp. 2152–2164, May 2014.
[37] K. Sheebi, M. A. E. Alali, O. A. Hamandouch, and S. Saadate, "Shunt active filters control aiming to limiting the spreading of the harmonic currents resulting from an industrial facility onto the medium voltage networks (case study in industrial site)," *Egyptian J. Appl. Sci.*, vol. 27, no. 7, pp. 181–192, Jul. 2012.
[38] A. Bourgeade, M. Ghanes, J.-P. Barbot, B. Abdelkader, F. Maurice, and B. Robert, "New PWM inverter control based on optimal pulse pattern computation without phases symmetry constraints," *Control Eng. Pract.*, vol. 132, 2023, Art. no. 105390, doi: https://doi.org/10.1016/j.conengprac.2022.105390.
[39] M. H. Ahmed, M. Wang, M. A. S. Hassan, and I. Ullah, "Power loss model and efficiency analysis of three-phase inverter based on SiC MOSFETs for PV applications," *IEEE Access*, vol. 7, pp. 75768–75781, 2019.

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