IEEE Open Journal of the
Industrial Electronics Society

Received 7 August 2023; accepted 16 October 2023. Date of publication 20 October 2023;
date of current version 20 November 2023. The review of this paper was arranged by Associate Editor H. Li.

*Digital Object Identifier 10.1109/OJIES.2023.3326380*

# Wireless Control of Active Gate Drivers for Silicon Carbide Power MOSFETs

**DANIEL A. PHILIPPS (Student Member, IEEE), AND DIMOSTHENIS PEFTITSIS (Senior Member, IEEE)**

Department of Electric Energy, Norwegian University of Science and Technology, 7034 Trondheim, Norway

CORRESPONDING AUTHOR: DANIEL A. PHILIPPS (e-mail: daniel.a.philipps@ntnu.no).

This work was supported by the Research Council of Norway under the FRIPRO Grant 287820 "Adaptive Silicon Carbide Electrical Energy Conversion Technologies for Medium Voltage Direct Current Grids (ASiCC)."

**ABSTRACT** Active gate drivers (AGDs) enhance the controllability and monitoring of switching devices, especially for fast switching silicon carbide (SiC) power metal–oxide–semiconductor field-effect transistors (MOSFETs). To support information flow between gate driver, converter, and grid control units, high-performance digital infrastructure is required. This article proposes a practical strategy of assessing the benefits of using wireless communication technologies (WCTs) in power electronics systems (PESs) employing AGDs. First, information transmission routes (ITRs) are identified and located within a PES. Second, an ITR taxonomy is proposed, classifying ITRs and describing both application scenarios and requirements for every class. After presenting general advantages of WCTs over wired alternatives, seven specific WCTs are individually characterized. Subsequently, the benefits of using WCTs are evaluated for each ITR class, resulting in a specific recommendation for or against the use of WCTs, and at least one appropriate WCT for each ITR. Experimental results demonstrate that the wireless control of AGDs for SiC power MOSFETs is feasible using Bluetooth low energy. It is shown that an exemplary AGD can be effectively controlled with an information transmission delay of less than 45 ms, which is sufficient for the intended target applications.

**INDEX TERMS** Active gate driving, Bluetooth low energy (BLE), control, MOSFET, silicon carbide (SiC), wireless.

## NOMENCLATURE

| | |
|---|---|
| AGD | Active gate driver. |
| BLE | Bluetooth low energy. |
| CW | Continuous wave. |
| DPT | Double pulse test. |
| EHF | Extremely high frequency. |
| EMI | Electromagnetic interference. |
| FPGA | Field-programmable gate array. |
| HF | High frequency. |
| IDVL | Intermediate driving voltage level. |
| ITR | Information transmission route. |
| ITU | International Telecommunication Union. |
| MCU | Microcontroller unit. |
| MLVSGD | Multilevel voltage-source gate driver. |
| MOSFET | Metal–oxide–semiconductor field-effect transistor. |
| PCB | Printed circuit board. |
| PES | Power electronics system. |
| PSK | Phase-shift keying. |
| PWM | Pulsewidth modulation. |
| RF | Radio frequency. |
| SCPI | Standard Commands for Programmable Instruments. |
| SHF | Super high frequency. |
| SiC | Silicon carbide. |
| UHF | Ultrahigh frequency. |
| WCT | Wireless communication technology. |

## I. INTRODUCTION

Wide-bandgap switching devices have gained popularity in the past few years. Properly harnessed, their technological advantages allow high-efficiency, high-power-density, and high-temperature converter designs, even under varying load conditions [1], [2], [3], [4], [5], [6], [7]. To exploit the low

switching loss potential of SiC MOSFETs, a powerful gate driver is required.

As opposed to conventional gate drivers, AGDs are online-reconfigurable circuits that can manipulate the gate charging process [2], [3], [4], [5], [6], [8], [9], [10], [11]. AGDs have successfully activated the technological advantages of SiC MOSFETs by providing effective, yet fine-grained control of switching transitions [2], [3], [4], [5], [6], [8], [9], [10], [11]. In addition, many AGDs incorporate sensors that enable monitoring key parameters of switching devices. AGDs support fast switching and low switching losses, but also alleviate negative side effects of fast switching, mainly EMI [5], [7], [9], [10], [12] and elevated device stress due to overshoot voltages and currents compared to conventional gate drivers at the same operating points [5], [7], [10], [12], [13]. Furthermore, AGDs have been used to slow down voltage slopes [4], [5], [10] to lower the associated risks for the health of coil windings [14] in electrical machines or transformers. AGD topologies vary in the physical principles, i.e., circuitry and operating principles, employed to achieve switching transient control. The majority of AGDs require timed multichannel digital signals [4], [9], [13], [15], [16], and in addition to that, some need another digital or analog configuration signal [8], [10], [17].

Today's localized, reaction-driven, and often maximum-power-oriented approach of converter control will evolve into an intelligent and grid- and demand-optimized solution that features self-monitoring in the future. Numerous digital AGD concepts include various sensors [15], [16], [18], [19]. Collecting operational data with these sensors enables monitoring the health of switching devices. With their ability to monitor and manipulate switching device behavior, AGDs will play a key role in the transformation of converters to intelligent, partly autonomous units, supporting energy availability and security [2].

To make this future a reality, however, high-performance information technology is needed. Recent advances in both high-bandwidth wireless communication and data processing technology reveal great potential for converter and grid control. To make informed decisions about the usage of WCTs and system component autonomy, new approaches to classify information transmission in the context of PESs are required.

The most important advantages of wireless AGD control are as follows.

1) The benefits of using AGDs are enabled, while, at the same time, common-mode interference is reduced to a minimum because conductive and/or capacitive paths to the converter control are effectively eliminated.
2) As will be shown later, the integration of certain WCTs requires a higher degree of autonomy in converter subsystems. This can improve the system reliability and be used to implement advanced protection features.
3) Flexibility is added to the system, for example, regarding the placement of components.
4) Converters are made more modular using WCTs, as the different functional units are both electrically and mechanically separated.

These advantages are especially relevant in high-power PES employing SiC power MOSFETs, where AGDs can enhance the power MOSFET behavior significantly, and modular systems are especially worth considering. This is the case in applications with significant load and source variations, such as converters for large renewable energy sources.

Several WCT-enabled gate drivers have been presented recently [20], [21], [22], [23], [24]. These gate drivers predominantly rely on a binary transmission mode to control the state of a single gate driver switch per wireless signal [20], [21], [22], [24]. They mainly differ in the RF located either in the HF [21], [22], [24], the UHF [25], [26], or the EHF [20] ITU band. In case of receiver or transmitter failure, these binary transmission modes will not ensure system stability, but rely on additional safety measures to avoid shoot-through conditions. Furthermore, as SiC MOSFETs switch very fast, disturbances and EMI can be expected in the HF band. The UHF and EHF bands are located significantly above the expected EMI frequencies (below approximately 250 MHz [27], [28]) and are, therefore, not susceptible to disturbances from the converter. However, the hardware needed to broadcast and receive EHF signals requires careful RF design and restricts the placement of components in a converter, especially, if directional antennas are required. A wireless gate driver control using EHF frequency and digital signals [23] improves both wireless communication efficiency and reliability by using digital information encoding. Furthermore, it enables simple error correction. However, each switching action requires the transmission of one message. As a consequence, system stability cannot be guaranteed in case of receiver or transmitter failure. In addition, the encoding and decoding of the wireless signal require bulky and costly hardware using FPGAs or application-specific integrated circuits.

The aim of this work is to facilitate the decision process of WCT adaptation in a high-power converter design, addressing the following objectives.

1) Determine where in a converter system the abovementioned advantages of wireless information transmission can be utilized most effectively.
2) Identify suitable WCTs for these locations.
3) Demonstrate wireless AGD control in an experimental setup.

The contributions of this work are as follows:

1) a hierarchical model of information transmission in PES, the ITR taxonomy, defining the requirements of these ITRs on suitable communication technologies;
2) a systematic method to assess the suitability of WCTs for the realization of the various ITRs;
3) the demonstration of validity of both ITR taxonomy and WCT suitability assessment by the example of wireless AGD control using BLE.

Moreover, a recommendation for or against the usage of WCT in each of the ITR classes will be given, and related

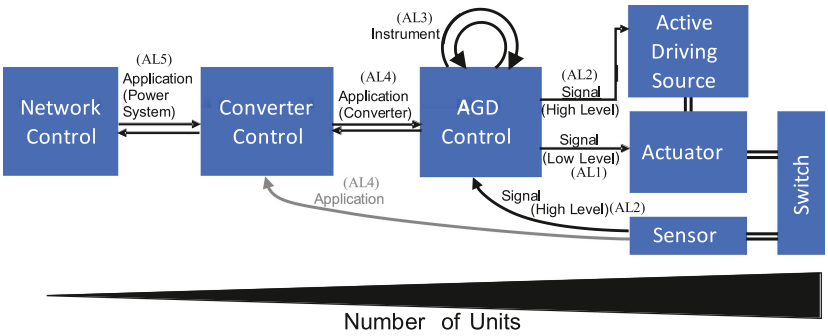


**FIGURE 1.** PES layout employing AGDs.

consequences for system safety will be laid out. The proposed suitability assessment methodology enables weighing benefits and challenges of using WCTs against each other on a conceptual level, leading to a multifaceted conclusion about whether and where WCTs constitute a valuable part in a converter design. Experimental results demonstrate the successful wireless control of an MLVSGD for SiC power MOSFETs using BLE as WCT.

The rest of this article is organized as follows. Section II examines the flow of information within a PES. The information structure of a PES employing AGDs is presented and ITRs are identified. Subsequently, a taxonomy for classifying these ITRs is proposed. Section III first elaborates on the advantages of WCTs over alternative wired technologies. Seven exemplary WCTs are introduced with their specific characteristics. Then, the process of assessing the suitability of WCTs for realizing an ITR is introduced and demonstrated for all previously defined ITRs. Section III closes with an analysis of the safety implications of using wireless control of AGDs. Experimental results that demonstrate the successful application of UART over BLE for controlling an MLVSGD for SiC power MOSFETs are presented in Section IV. Finally, Section V concludes this article.

## II. INFORMATION TRANSMISSION IN PES

### A. PES INFORMATION STRUCTURE

To facilitate evaluating the use of WCTs in a PES employing AGDs, the ITRs within this system are identified and classified in the following. Fig. 1 shows the structure of a PES incorporating AGDs. It consists of the following:

1) system components, conceptual units, symbolized by labeled rectangles;
2) physical, i.e., electrically conductive, links shown as thick lines;
3) directed ITRs as arrows.

A tree structure with a single network control at the root and several branches for each new instance would describe an actual PES better, as it does not consist of only one of the depicted structures. To avoid redundancy, this is represented by the black triangle on the bottom of Fig. 1. The width of this triangle indicates the number of involved components and information links.

The network control represents the grid operator control instances, which can be manifold and, depending on the network structure, more or less complex. The converter control symbolizes the local control units, ensuring compliance with the network control directive, for example, real and reactive power output. At the same time, the converter control governs the converter state. The converter state includes the system temperature, power-sharing among modular converter subsystems, health monitoring, predictive maintenance functionality, and potentially more, depending on the specific system. The AGD control translates abstract commands given by the converter control into suitable command and PWM switching signals for the downstream active driving source and AGD actuator. As mentioned above, the system structure visualized in Fig. 1 appears linear for simpler illustration. In fact, the number of components further toward the right of the schematic diagram is larger than to the left. One AGD control unit, therefore, can provide commands and PWM switching signals for multiple active driving sources and AGD actuators and, therefore, be in control of multiple switches. An AGD control unit, like the one used in this work, can be in control of up to four switches that are required for a full-bridge circuit. This means that an accordingly powerful microcontroller must be installed to provide the required amount of PWM signals and implement simple control functions. In this work, a similar microcontroller as the TI TMS320F280049C microcontroller is assumed as the AGD control unit. The output signals of the AGD control unit are directed toward the actuator, i.e., the gate driver switches, and the active driving source, i.e., the part of the AGD that makes it online-configurable. To make this structure more clear, Fig. 2 shows the schematic diagram of a four-level MLVSGD connected to the device under test (DUT) in a test setup. The AGD consists of three parts, the AGD control unit that generates PWM switching signals and control signals for the other two parts, the active driving source that provides the reconfigurable voltage levels, and the actuator containing the switch array that delivers these voltage levels to the gate.

The sensor block in Fig. 1 symbolizes one or multiple sensors of any type. To name examples, this could be a current sensor, a voltage or current slope ($dv/dt$ or $di/dt$) sensor, a temperature sensor, etc. The sensor block is an optional part

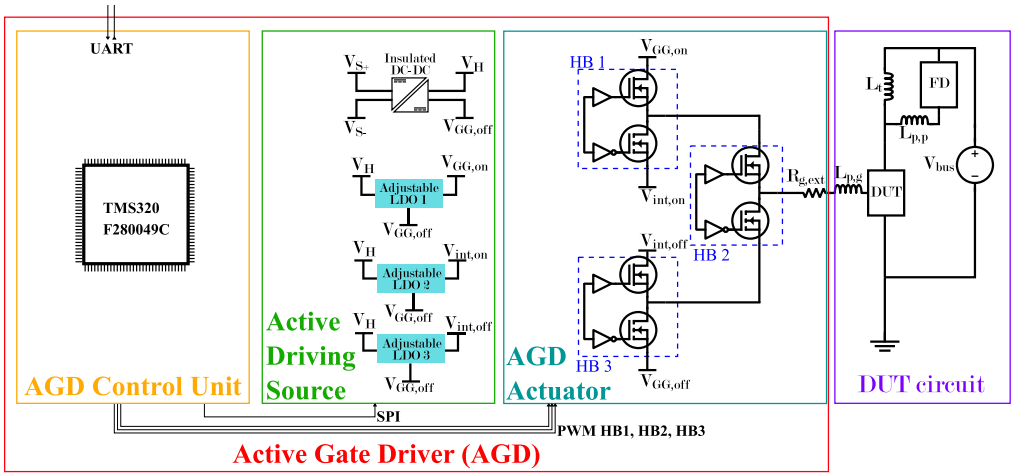


**FIGURE 2.** Schematic diagram of an exemplary AGD, a four-level MLVSGD, and its components, connected to a test circuit.

**TABLE 1.** ITR Classification

| Abstraction Level (AL) | Exemplary Information Content | Data Rate Requirement | Latency Requirement |
|---|---|---|---|
| Application (Power System) (AL5) | Power Flow control (P/Q), Digital Filtering | Low/Mediocre | Low ($<$ 10 s) |
| Application (Converter) (AL4) | EMI control, Active Temperature Control | Low/Mediocre | Low ($<$ 100 ms) |
| Instrument (AL3) | $\frac{dv}{dt}$, $\frac{di}{dt}$, $\frac{d\theta}{dt}$ | High | Mediocre ($<$ 1 ms) |
| Signal (High Level) (AL2) | AGD Source Configuration (Voltage/ Current/Resistance) | Very High / High | Very High ($<<$ 100 µs) |
| Signal (Low Level) (AL1) | Gate Driver Timing, Gate Signal | Extremely High | Extremely High ($<<$ 100 ns) |

of the AGD, and it will in most cases communicate back to the AGD control. In safety-critical sensor applications, or for control purposes implemented on a higher level like, for example, active temperature control, the communication might also be established with the converter control unit directly.

### B. ITR TAXONOMY

Each ITR within this PES structure is assigned a level of abstraction describing the physical distance of that ITR to the switching devices it has an impact on. With increasing level of abstraction, an ITR is located at a larger distance from the switching devices it impacts, and it has an impact on more switching devices. In this work, an ITR is not distinguished from the information or signal passed through this ITR, and these are, therefore, classified identically, and as one unit. In the case of the PES structure presented in Section II-A, the proposed taxonomy yields six classes, i.e., abstraction levels. A summary of the ITR Taxonomy can be found in Table 1.

#### 1) ABSTRACTION LEVEL 1 (AL1) BETWEEN THE AGD CONTROL AND THE ACTUATOR

This ITR is assigned the lowest abstraction level, named "Signal (Low Level)" as it has an immediate effect on the gate–source voltage of a single power switch or potentially few parallel connected power switches. Therefore, the ITR has a distance of at most few centimeters to the switching device it controls. This results in a low level of abstraction, the lowest in the context of this work, AL1. The signals of this ITR must have a very high resolution in time. Depending on the AGD architecture, only very short delays are acceptable, down to the range of 500 ps and even below. Some AGDs require multiple channels of this signal type. Although only binary information is required on this route and the average information entropy is low as the information is highly repetitive, the high time resolution, possibly required on multiple channels simultaneously, leads to an extremely high data rate.

#### 2) ABSTRACTION LEVEL 2 (AL2) BETWEEN AGD CONTROL AND ACTIVE DRIVING SOURCE

All AGDs are realized with a configurable unit that is separate from the gate driver switches (Actuator) and, in the context of this work, is referred to as active driving source. In current and multilevel voltage-source AGDs, this is the configurable power supply, and in the case of variable external resistor AGDs, this is the resistor configuration, for example. The distance to the switch is increased compared to AL1, as the active

driving source is located "behind" the actuator seen from the switching device(s). The required data rate depends on the controllability requirement. A fast response is desired because control loops utilizing AGD functionality could be potentially limited by the latency introduced in this path. However, the active driving source itself has a minimum reaction time tied to its digital (digital isolators, digital potentiometers, microcontrollers, etc.) and analog components that determine its dynamics, for instance, the output response of a variable voltage source in the case of an MLVSGD. In addition, as opposed to the actuator signals, it is not necessary to transmit at every switching instance. The data rate is, therefore, significantly lower than in the case of AL1, but still significantly higher than in higher abstraction levels. Reaction times range below 100 µs.

#### 3) ABSTRACTION LEVEL 3 (AL3) WITHIN AN AGD CONTROL

With the PES layout in Fig. 1, the AGD control block can have multiple responsibilities. The converter control will provide abstract information about, for example, the allowed voltage overshoot and maximum slope in the context of an EMI control. The AGD control unit has the following four responsibilities.

1) Given the command received from the converter control, and with the knowledge of the current AGD state, check for deviance from the converter control command.
2) Then, determine the necessary sequence of switching condition commands that bring the state of the switch into compliance with the converter control command immediately or over a period of time. These switching condition commands are, for example, the voltage slope during switching $dv/dt$, the current slope during switching $di/dt$, the desired temperature gradient $d\theta/dt$, etc.
3) With the knowledge of how switching device and AGD together behave, translate the sequence of switching condition commands into a sequence of AGD configurations.
4) Send this sequence of AGD configurations to the active driving source and the actuator via ITRs on AL2 and AL1.

The computational power of one MCU might not be sufficient to realize all of these tasks. Therefore, tasks 1 and 2 might be implemented in two separate MCUs, which communicate over an ITR on AL3. The amount of information exchanged on this ITR is again significantly lower than on AL2, as only single numerical values need to be transmitted, but because a high degree of repetition is required, the data rate qualifies as "High." To achieve fast control, the latency introduced by this ITR should not surpass 1 ms. The two ends of this ITR are located within the AGD control unit. As has been mentioned earlier, this ITR can, therefore, be regarded internal to the AGD control block. In the AGD example presented in the experimental part of this work (see Section IV), this ITR does not exist separately because the associated information is handled within the MCU. Besides, the information transmitted on AL3 is highly specific to the AGD type. Encapsulating this information within one MCU enables easier abstraction.

#### 4) ABSTRACTION LEVEL 4 (AL4) BETWEEN CONVERTER CONTROL AND AGD CONTROL

This ITR transmits application-specific information. In the context of EMI control, for example, boundary values of the voltage and current overshoot and slope could be transmitted, or a desired junction temperature or temperature range in the case of active temperature control. Thermal systems exhibit slow dynamics in the range of many seconds. Therefore, for this application, a reaction time below 100 ms is regarded sufficient. The very fast switching speeds observed with SiC pose challenges in the health of inductor and especially electrical machine windings [14]. By limiting the maximum voltage slope steepness through EMI control, this issue can be softened and the lifetime of windings prolonged, comparing winding lifetime tests with five- and two-level inverters [29]. With a maximum failure rate of 2%, a twisted-pair lifetime of approximately 3000 s has been observed in a two-level converter test with voltage rise times of 60 ns [29]. When detecting a high $dv/dt$ condition that might deteriorate the lifetime of the winding insulation material, taking action by reconfiguring the AGD within 100 ms is, therefore, regarded sufficiently fast to achieve major lifetime improvements.

#### 5) ABSTRACTION LEVEL 5 (AL5) BETWEEN NETWORK CONTROL AND CONVERTER CONTROL

This signal can, for example, contain (active and reactive) output power commands, (active and reactive) output power slope commands, etc. It affects all switches in a converter or even multiple converters and can be located at a distance of multiple meters or even kilometers from the switches it affects. It is, therefore, assigned the highest abstraction level in the context of this work, AL5. Delay requirements for this information type are far more relaxed, as the power system reserves buffer short-term misalignment. Moreover, electric energy market planning may allow converter preconfiguration in the future, so that the continuous time-critical information flow can be optimized. Altogether, this results in only mediocre or even low average rate of data transmission.

## III. WCTS FOR PES

### A. ADVANTAGES OF WCTS OVER WIRED ALTERNATIVES

WCTs exhibit major advantages over wired alternatives such as digital signal isolators and fiber-optic cables. SiC MOSFETs accelerate the trend toward faster switching speeds to reduce associated losses and filter size. This leads to steadily increasing requirements in regard to high voltage isolation, $dv/dt$ immunity, and common-mode rejection. While this is a major issue for the use of digital isolators, these requirements are

**TABLE 2. WCTs by Example**

| Wireless Technology | Data Rate Limit | Latency (excl. Propagation Delay) | Spatial Range | Advantages | Disadvantages |
|---|---|---|---|---|---|
| SHF/EHF CW | Spectral Bandwidth and Sampling Frequency Dependent, $>>$ 2 Gbps | $\leq$ 100 ns | Implementation Specific | Noise Immunity | Efficiency, Hardware Cost and Complexity (RF) No Error Correction |
| SHF/EHF PSK | Spectral Bandwidth and Sampling Frequency Dependent, $\leq$ 1 Gbps | $\leq$ 1 µs | Implementation Specific | Noise Immunity | Hardware Cost and Complexity (De-/Modulation + RF) No Error Correction |
| BLE | Hardware and Service Dependent, $\leq$ 1 Gbps | $\leq$ 100 ms | $\leq$ 10 m | Hardware Cost, Availability | Latency, Data Rate |
| WiFi | Hardware Dependent, $\approx$ 1 Gbps | $\leq$ 10 ms | $\leq$ 1000 m | Hardware Cost, Availability, Security | Latency |
| WWAN (e.g.4G) | Location Dependent, $\leq$ 100 Mbps | Location Dependent, $\geq$ 100 ms | | Hardware Cost, Network Integration, Availability, Security | Latency, Operating Cost, Dependence on Telecom. OPs |

easily fulfilled by WCTs and fiber-optic cables. In addition, both fiber-optic cables and WCTs operating in the UHF band or at even higher frequencies are not equally affected by EMI as wired solutions because less conductive cables are required. EMI frequencies are usually limited to 250 MHz [27], [28], and WCTs, e.g., BLE or Wi-Fi, commonly operate at frequencies well above 2 GHz.

In comparison to both digital isolators and fiber-optic cables, WCTs significantly enhance the modularity of PES. This modularity facilitates the mechanical placement of subsystems, allowing for optimal filter locations and thereby improved electrical behavior. Apart from that, the increased modularity simplifies maintenance procedures as subsystems are more easily connected and disconnected and made more accessible. In addition, WCT-enhanced converters can be scaled more easily, for example, by adding converter building blocks to increase the converter power rating. Finally, WCTs on high abstraction level ITRs, such as BLE or Wi-Fi, inherently enable two-way communication. Bidirectional digital isolators are widely available. Enabling two-way information transmission with fiber-optic cables requires twice as many cables and a significant amount of available power on the secondary side, which would be the AGD or AGD control unit for example. However, AGDs are limited in the power available for this purpose. Increasing the AGD power supply would lead to increasing the coupling capacitance and thereby degrade the common-mode interference rejection. These factors discourage enabling bidirectional information transmission with fiber-optic cables. However, as was mentioned in Section I, integrating sensors into AGDs constitutes an important motivation for their usage and a significant advantage over conventional gate driver systems. Therefore, utilizing WCTs for AL4 ITRs is regarded particularly valuable for future integration of AGDs.

To summarize, WCTs are superior to digital isolators in regard to high-voltage isolation and $dv/dt$ ruggedness while being significantly less expensive than fiber-optic solutions (cost aspects will be discussed more below). Furthermore, in comparison to both digital isolators and fiber-optic solutions, WCTs provide more flexibility and simpler scalability as mechanically fixed links are reduced. These advantages are best utilized in high-power PES where the distance between subsystems can be significant and modular systems are the solution of choice to provide the required power rating.

### *B. CHARACTERISTICS OF EXEMPLARY WCTS*

The three main characteristics of WCTs are data rate, latency, and range. Data rate describes the amount of information that can be transmitted in a fixed time interval, latency is the delay caused by preparation, transmission, reception, and interpretation of information, and range refers to the distance over which information transmission is reliable at the specified data rate and latency. Table 2 contains these characteristics for seven exemplary WCTs. Moreover, the greatest advantages and disadvantages of each WCT are mentioned. These exemplary WCTs were chosen because they are either commonly available (Wi-Fi, BLE, 4G), have been demonstrated in literature (EHF CW), or present an interesting alternative to what has been studied in literature (SHF/EHF PSK and SHF CW).

These technologies can be divided into two groups: low-level WCTs (SHF/EHF CW/PSK) that transmit information in the form of single bits; and higher level WCTs that provide abstracted transmitted information (Wi-Fi, BLE, 4G). Low-level WCTs can be seen as a direct substitute for wired signal lines and the associated line drivers because both transmit binary signals. Just as wired signal lines, low-level WCTs do not have an inherent error correction ability. Higher level WCTs are a substitute for wired signal lines, line drivers, and the integrated circuits implementing a communication protocol (e.g., UART). Instead of information in the form of bits, these WCTs deliver aggregated information packages, encapsulating and abstracting the wireless hardware. Higher level WCTs typically implement error correction. However, this comes at

the cost of processing time and demand for control information, which result in a significantly larger latency and reduced maximum data rate.

### C. WCT SUITABILITY ASSESSMENT

Table 2 shows that wireless solutions exist to support all previously introduced ITR classes. To help deciding on the use of WCTs for a given ITR, three aspects must be considered.

1) The WCT must fit the application requirements under nominal operating conditions.
2) In a worst case scenario, the failure of the WCT in question must have deterministic consequences that are acceptable from the perspective of system safety and security.
3) The implementation of a WCT must be worthwhile considering wired alternatives with regard to cost, complexity, operation safety, and reliability.

These questions have to be answered individually for every abstraction level as the WCTs take different roles, and different WCTs come into question. This decision process is described hereafter for all abstraction levels. Whenever prices are stated in the following, these prices refer to 2023 prices from a well-known European distributor of electronic components.

#### 1) ABSTRACTION LEVEL 1

As already mentioned, wireless gate drivers have been proposed for controlling PWM switching signals that are passed through AL1 and AL2 ITRs [20], [21], [22], [24]. However, potentially unstable converter states in case of transmitter or receiver failure raise safety concerns when using CW that does not support inherent error correction or digital modes that require one signal per switching event. PSK has a slight advantage over CW in this regard, as it requires a constant carrier signal. Losing RF contact or transmitter failure could be easily detected by a missing or faulty carrier signal. However, digital isolators and wired signal lines do not have the same disadvantages: Using WCTs on this ITR abstraction level requires more complex hardware that is more cost intensive and less flexible. In addition, this hardware occupies more space and thereby adds considerable parasitic coupling capacitance. These aspects will be discussed in more detail in the following.

The proposed wireless gate drivers presented in literature operate in the EHF band and an FPGA on the transmitter side [20] or on both the transmitter and receiver sides [23]. Moreover, (partly) directional antenna systems are required for these systems. Wireless gate drivers in the HF band do not require directional antennas, but the antenna size is significant [22]. Digital isolators do not require complex antenna systems and also no FPGA to transmit signals.

A major challenge in fast-switching converters is capacitive current injection caused by steep voltage slopes. This type of disturbance is caused by capacitive coupling of jumping potentials to a fixed potential within the converter through the gate driver. With voltage slopes of 20 kV/µs, a current of 20 mA per 1 pF of coupling capacitance has to be expected.

The coupling capacitance can be divided into a component added by the power supply and another component added by the signal lines. A power supply is required irrespective of using wired signal connections (digital isolator/fiber optics) or WCTs, so this path cannot be eliminated. Power supplies introduce a significant amount of coupling capacitance, that is of the order of 10 pF in state-of-the-art isolated dc–dc converters. The coupling capacitance typically increases with increasing power rating. While digital isolators practically do not increase the demand for power, fiber-optic transmitter LEDs and the digital components of WCTs capable of realizing AL1 ITRs increase the power demand, which leads to an increase of this capacitance.

The two main contributors to the coupling capacitance of signal lines are the so-called self-capacitance of conductive materials and the added capacitance due to the signal lines. Intrinsically, volumes of conductive material have a finite self-capacitance. This capacitance occurs with ground potential located at a far distance, "far" meaning multiple times the largest dimension of the respective volume. This capacitance strongly depends on the geometry of the respective conductive volume and can be approximated using finite-element method (FEM) simulations or applying Gauss's law to an approximate simplified conductor structure. For a thin conductive disc, the self-capacitance is proportional to the radius and, thereby, to its circumference [30]. Therefore, the self-capacitance of a conductive volume can be expected to increase proportionally with its circumference. FEM simulations of a square copper sheet with 1-cm side length and 35-µm thickness, located at the center of a 50-cm hollow cubic copper block at ground potential, result in a capacitance of approximately 0.5 pF. For fiber-optic solutions, this is a fair approximation of the added capacitance in the signal transmission path, as the required PCB area for signal conditioning will not exceed 1 $cm^2$.

For WCTs, the self-capacitance depends strongly on the WCT in question. WCTs suitable for AL1 ITRs require significantly more space. One proposed SHF/EHF solution demonstrated in the literature [23] requires a 5.75-$cm^2$ wireless module with a circumference of 9.6 cm. Therefore, a capacitance of approximately 1.2 pF can be expected from the wireless module alone, not including the FPGA for signal evaluation.

In comparison to this, the capacitance introduced by conducting wires near the converter enclosure can reach approximately 27.2 pF/m assuming a 0.75-$mm^2$ wire that lies in an edge of the converter enclosure such that roughly half of the outer perimeter couples ideally to ground through 500 µm of insulation material with a relative permittivity of $\epsilon_r = 2$. The resulting capacitance is much larger than that of the digital isolator IC, which is approximately 1 pF for state-of-the-art digital isolators. Hence, the coupling capacitance of digital isolators is dominated by the coupling capacitance of the integrated circuit itself and the self-capacitance of the integrated

circuit and its surrounding circuitry, approximately 0.5 pF, adding up to 1.5 pF.

The disadvantages of WCTs suitable for AL1 ITRs are not counterbalanced by the advantage of inherent high voltage isolation. When available, digital isolators are the best solution here, as they operate with a comparable $dv/dt$ ruggedness, and are significantly less complex and costly (USD 2.40 per bidirectional, 10-kV, 180-kV/µs digital isolator as compared to USD 23.41 per set of fiber-optic components, and an unknown cost of the abovementioned wireless module that contains 60-GHz RF technology that is not available off-the-shelf from said distributor). Hence, the usage of WCTs for AL1 ITRs is not recommended.

#### 2) ABSTRACTION LEVEL 2

The considerations for AL1 ITRs are valid for AL2 ITRs as well. Since the requirements in regard to data rate and latency are lower though, less complex WCTs could be used. However, none of the previously considered WCTs fits this purpose, except for those that can support AL1 ITRs but were ruled out because of the disadvantages listed above. Therefore, the use of WCTs for ITRs on AL2 is not recommended.

#### 3) ABSTRACTION LEVEL 3

With the yet reduced requirements of ITRs on AL3, more WCTs, that lie outside the scope of this work, come into question for the realization of information transmission. As mentioned before, AL3 ITRs are located within the AGD control block. Using WCTs adds unnecessary cost and complexity where either the use of a more capable MCU as AGD control unit or a wired connection accelerates control, reduces system complexity, and increases reliability. Therefore, it is recommended not to use WCTs as ITR implementation on AL3.

#### 4) ABSTRACTION LEVEL 4

The further reduced latency requirement to 100 ms for ITRs on AL4 makes BLE and Wi-Fi viable WCT candidates that are widespread, well documented, and cheaply available. Both BLE and Wi-Fi support the required data rate at the range required for the communication within a converter.

Moreover, the voltage blocking capability is provided by distance in air. The advantage of this is that the clearance requirements that have to be considered for the converter to run safely are sufficient for safe WCT operation, without checking additional ratings as it is the case for digital isolators. The PCB area required for BLE or Wi-Fi solutions does not exceed 1 $cm^2$. Therefore, these WCTs only add a coupling capacitance of approximately 0.5 pF according to the abovementioned FEM simulation, taking into account that the power required by BLE and Wi-Fi solutions usually does not require an increased isolated dc–dc supply rating with a higher coupling capacitance.

Apart from that, adding WCTs to support AL4 ITRs has more positive effects. Depending on the individual implementation, AGD control units can control entire half-bridge or full-bridge circuits. The AGD control units generate PWM switching signals for the AGD actuator and configuration signals for the active driving source. Half- and full-bridge circuits are fundamental converter subsystems. When realizing AL4 ITRs with WCTs, these fundamental subsystems are made electrically and mechanically separable from each other. This enhances modularity, adaptability, and flexibility by increasing subsystem autonomy, without introducing higher cost or complexity as it would be the case on lower abstraction levels. For example, using an ESP32 RF system on chip (RFSoC), all that is needed for using BLE or Wi-Fi for the task is to include this cheap (USD 1.11 per piece) and widespread microcontroller to the AGD and the converter control with a simple PCB antenna for 2.4 GHz. The main challenge for wireless technology integration in this communication path is to ensure safe, secure, and reliable communication in the presence of fast switching slopes. More information on these aspects will be given in Section III-E. Apart from that, synchronization of series- and parallel-connected switches will become a challenge depending on the converter architecture.

Overall, the use of WCTs for AL4 ITRs is recommended. An example for AGD control using BLE will be demonstrated experimentally in Section IV.

#### 5) ABSTRACTION LEVEL 5

As mentioned earlier, today's power system does not yet have the structure laid out in Fig. 1, so there is no wired infrastructure present. For economic reasons, the installation of a direct wired connection over several kilometers of distance and to multiple reception points is not realistic, while connecting to a wireless wide area network (WWAN) either directly or via an Internet connection is simple and associated with a significantly lower investment cost. Considering that viable options fulfilling the requirements exist without detrimental disadvantages, using WCTs for this ITR is recommended. All recommendations are summarized in Table 3.

### D. WCT DECISION CRITERIA

Especially, when transmitting information on a high abstraction level, multiple WCTs might be able to realize a specific ITR from the perspective of data rate, latency, and range. The system designer can base their choice between them on multiple factors.

1) *Operability:* Switching devices emit electromagnetic radiation. Choosing between viable solutions in regard to data transmission must include a consideration of possible interference. For that, the datasheet of WCT hardware includes signal-to-noise ratio (SNR) requirements. With a suitable software-defined radio, the SNR value can be determined directly. Furthermore, the signal level can be estimated by the RF transmitter power and the line-of-sight distance to the AGD control unit.

**TABLE 3. ITR Abstraction Levels and WCT Usage Recommendations**

| Abstraction Level (AL) | Suitable WCT | Wired Alternative | Recommendation |
|---|---|---|---|
| Application (Power System) (AL5) | Wireless Wide Area Network (WWAN), e.g. 4G | Wired Internet Connection (fiber optic, coaxial, etc.) | WCT |
| Application (Converter) (AL4) | WiFi, Bluetooth LE | Bi-directional Digital Isolators | WCT |
| Instrument (AL3) | SHF/EHF PSK | Bi-directional Digital Isolators | Wired Alternative |
| Signal (High Level) (AL2) | SHF/EHF PSK | Uni-directional Digital Isolators | Wired Alternative |
| Signal (Low Level) (AL1) | SHF/EHF PSK, SHF/EHF CW | Uni-directional Digital Isolators | Wired Alternative |

These two estimates can be used for assessing the operability of a WCT. The demonstration of these techniques, however, lies outside the scope of this work. A practical approach to determine operability is to measure the delay time that is introduced by the information transmission with the given WCT. This will be demonstrated in Section IV.

2) *Structural integrity:* Depending on the desired hierarchy of transmitters and receivers (e.g., mesh versus radial networks), certain WCTs are more desirable than others (e.g., BLE for mesh versus Wi-Fi for radial networks).
3) *Development time:* Another difference between the WCTs is availability. To name an example, for BLE, both hardware and software already exist that can encapsulate the wireless information transmission and interface it to a control MCU with little additional effort. The experimental part of this work presented in Section IV demonstrates that with suitable hardware and a compatible software implementation, adding a wireless interface is simple and convenient.
4) *Hardware cost:* Hardware prices vary greatly by manufacturer and change quickly and continuously; thus, no numbers are given in this work. However, numerous MCUs have integrated Wi-Fi and BLE modules (such as the ESP32). Such integrated solutions are usually cheap and easily integrated with the AGD control MCU. Choosing between the different WCTs that are available simultaneously must then be decided on by other factors as laid out before.

### E. SAFETY IMPLICATIONS OF USING WIRELESS AGD CONTROL

As mentioned above, realizing wireless AGD control on AL4 requires carefully considering the safety, security, and reliability of the wireless connection. Abstract information is transmitted through this ITR, and not PWM switching signals. Applications that can be supported by this information include efficiency optimization, EMI management, and active thermal control. A possible interruption in this ITR is, therefore, not detrimental for the immediate stability of the converter, as switching signals continue to be generated (or safely shut down) by the AGD control unit.

Using an independent MCU as AGD control unit as proposed in this work effectively increases the gate driver autonomy. This added autonomy can enhance system safety, since the free computational power of the AGD control unit microcontroller can be used to perform system monitoring tasks, and integrate safety features. This includes classic protection features like desaturation detection, but also advanced monitoring and protection features like EMI or parameter drift detection are feasible. The choice of the MCU as AGD control unit is especially important in this regard. It is recommended to use functional safety certified MCUs that are available from the major MCU manufacturers, and the recommendations of the IEC 61508 standard have to be followed for adequate functional safety of the PES.

In regard to cybersecurity, BLE has been shown to have exploitable pairing procedures. A way to tackle this problem is the usage of encrypted information exchange instead of human-readable messages. By using suitable encryption technology, the injection of false information into the AGD control MCU can be detected. For example, an ESP32 RFSoC could act as a BLE adapter. Handling the BLE connection is a simple task. The free resources can be used for implementing cryptographic processes to encrypt the critical data. Since the information routes are assumed to be bidirectional, a warning about possible interception attempts can further enhance awareness of this issue.

## IV. WIRELESS AGD CONTROL VALIDATION EXPERIMENTS

In Section III, it was determined that in a PES structure as the one presented in Section II, BLE is suitable for wireless control of AGDs. To demonstrate that the information transmission delay of BLE fits the requirements for AL4 ITRs (as defined in Section II-B), experiments were conducted. In the following, an exemplary AGD will be discussed first. This AGD forms the basis on which wireless AGD control was investigated. Subsequently, the experimental test setup and the experimental results will be presented.

### A. WIRELESS-CONTROLLED AGD

A four-level MLVSGD was used for demonstrating the application of BLE for wireless AGD control. This specific AGD was chosen for practical reasons, as it was studied in earlier work [8]. However, other AGDs like active current source,

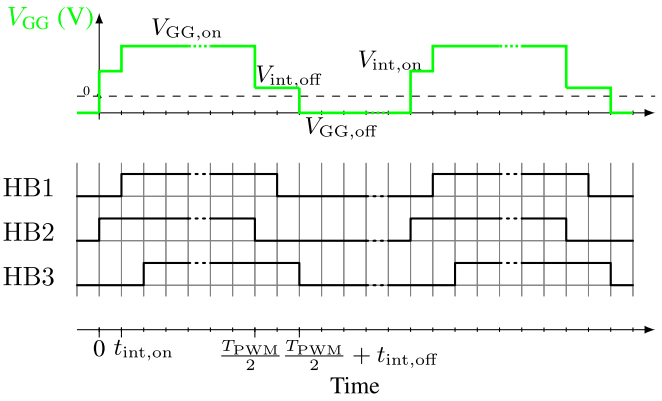


**FIGURE 3. Four-level MLVSGD [8]: Idealized gate driver output voltage $V_{GG}$ and corresponding control signals for the half-bridge circuits HB1, HB2, and HB3 of the AGD.**

variable resistor, and other multilevel voltage gate drivers [2], [3], [4], [5], [6], [9], [10], [15], [16], [17], [18], [20] could be used with the proposed wireless AGD control, if they implement control over a UART interface that can be connected to a BLE UART bridge, as will be explained below.

The MLVSGD applies a configurable IDVL to the gate at turn-ON ($V_{int,on}$) and another configurable IDVL at turn-OFF ($V_{int,off}$). The IDVLs are each provided by a digitally adjustable linear regulator (active driving source in Fig. 2) that is controlled by the TMS320F280049C MCU (AGD control unit in Fig. 2) using the serial peripheral interface (SPI). The high driving voltage $V_{GG,on}$ is configurable as well. The low driving voltage $V_{GG,off}$ is fixed at $-5$ V. Besides controlling these voltage levels, the AGD control MCU generates a timed pulse pattern consisting of three PWM channels, one for each half-bridge circuit of the gate driver, denoted as HB1, HB2, and HB3 in Fig. 2. These half-bridge circuits are referred to as the AGD Actuator (see Fig. 2). The delay between the PWM signals of HB1 and HB2 determines the IDVL duration at turn-ON ($t_{int,on}$), and the delay between the PWM signals of HB3 and HB2 determines the IDVL duration at turn-OFF ($t_{int,off}$). Note that this duration is not the same as the turn-ON and turn-OFF times (often denoted as $t_{on}$ and $t_{off}$) that describe the duration of the drain–source voltage transition. $t_{int,on}$ and $t_{int,off}$, on the other hand, are AGD parameters that have an impact on the entire switching trajectory. Fig. 3 depicts the idealized gate driver output voltage $V_{GG}$ and half bridge circuit (AGD actuator) PWM signals required to generate this output voltage. In the following, only the turn-ON switching transition will be considered.

To demonstrate the ability of the MLVSGD to control the SiC power MOSFET switching behavior, Fig. 4 depicts hard-switching DPT measurements at turn-ON in two scenarios. The parameters of these two DPT experiments are listed in Table 4. Fig. 4(a) shows the control signals of half-bridges HB1 and HB2, Fig. 4(c) shows the gate–source voltage, and Fig. 4(e) shows the drain–source voltage, the drain current, and the instantaneous loss power during switching with an

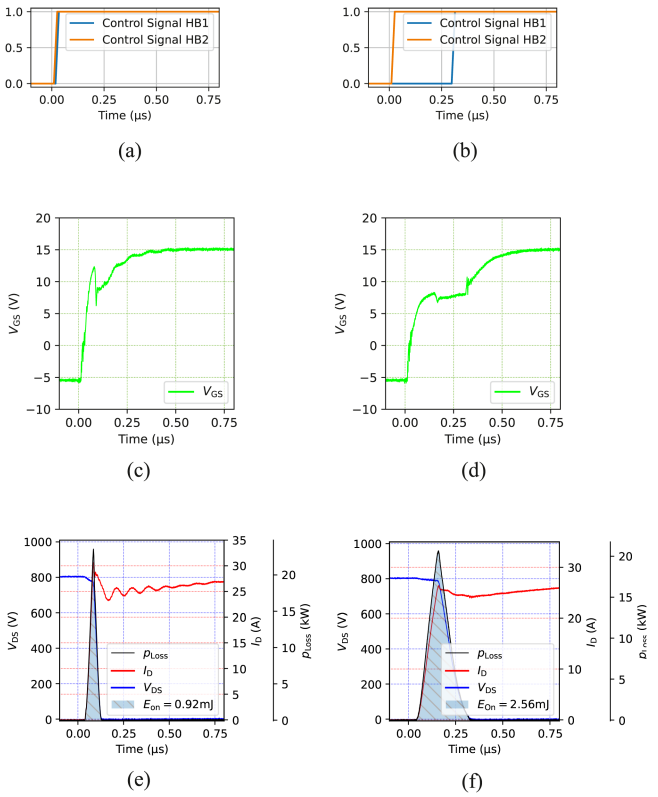


**FIGURE 4. DPT results using the control signal configuration shown (a) and (b). Gate–source voltage measurements (c) and (d), as well as drain–source voltage, drain current, and loss power as well as energy (e) and (f) before and after command transmission. (a) Half-bridge control signals at turn-ON before command ($t_{int,on}$ = 20 ns). (b) Half-bridge control signals at turn-ON after command ($t_{int,on}$ = 300 ns). (c) Gate–source voltage at turn-ON before command ($t_{int,on}$ = 20 ns). (d) Gate–source voltage at turn-ON after command ($t_{int,on}$ = 300 ns). (e) Drain–source voltage, drain current, and instantaneous loss power at turn-ON before command ($t_{int,on}$ = 20 ns). (f) Drain–source voltage, drain current, and instantaneous loss power at turn-ON after command ($t_{int,on}$ = 300 ns).**

**TABLE 4. DPT Conditions**

| Parameter | Value |
|---|---|
| SiC Power MOSFET Model | C3M0075120D (1200 V, 30 A) |
| $V_{test}$ | 800 V |
| $I_{test}$ | 25 A |
| $R_{g,ext}$ | 25 Ω |
| $V_{int,on}$ | 8.2 V |
| $t_{int,on}$ | 20 ns \| 300 ns |

intermediate voltage duration of $t_{int,on}$ = 20 ns. Moreover, the switching loss is given. Fig. 4(b), (d), and (f) shows the same measurements for an intermediate voltage duration of $t_{int,on}$ = 300 ns.

Changing $t_{int,on}$ from 20 to 300 ns results in an increase in switching losses at turn-ON from 0.92 to 2.56 mJ. Switching loss manipulation is a way to control the junction temperature of the power MOSFET, which can be used as part of an active temperature control directive [8]. Furthermore, the current slope is reduced from 0.673 to 0.328 A/ns, and the voltage

slope from 21 to 7.37 kV/µs, demonstrating the capability of adjusting the SiC power MOSFET switching dynamics. Finally, the drain current oscillation intensity and reverse recovery current peak is decreased significantly, as can be seen in Fig. 4(e) and (f). These results prove the capability of the MLVSGD to significantly manipulate the switching behavior of SiC power MOSFETs.

The TMS320F280049C MCU supports serial communication over UART, and the custom AGD control firmware is equipped with an SCPI command interpreter accepting inputs from the UART interface. Sending commands over this serial interface, the parameters mentioned above can be set either manually or automatically using suitable software. For example, to set the duration of the IDVL at turn-ON, $t_{\mathrm{int,on}}$, to 300 ns, requires transmitting the message ":TEST:TDON 300\r\n" to the UART input of the AGD control unit. The AGD control unit will then react to this command by setting the delay between the HB1 and HB2 PWM signals to 300 ns. Connecting the BLE UART bridge to the respective UART terminals of the AGD control unit makes the interface available over BLE and thereby enables wireless control over the MLVSGD.

### B. TEST SETUP

To measure the delay time that is introduced by the information transmission over BLE, a test setup was assembled. Fig. 5 shows a schematic diagram of this test setup. To simplify measurements, the test setup is divided into two parts: a signal part and a power part.

In the signal part of the experimental setup, an ESP32 MCU acts as a BLE central device and transmits messages to the BLE peripheral device, an Adafruit Bluefruit LE Friend, using the Nordic UART Service (UUID 6E400001-B5A3-F393-E0A9-E50E24DCCA9E). The messages are forwarded to the TMS320F280049 C MCU that acts upon the received command and changes the PWM control signals of the four-level MLVSGD actuator (HB1, HB2, and HB3). In addition, the TMS320F280049C MCU generates a PWM signal with a duty cycle of 50% at a frequency of $f_{\mathrm{PWM}} = 50$ kHz, which is forwarded to the power part of the test setup. This PWM signal is not changed during the experiments.

The power part of the test setup consists of a half-bridge circuit of two C3M0075120D discrete SiC power MOSFETs on a low-inductive test platform (LITP). A schematic circuit diagram of the LITP, that was introduced in an earlier work [31], [32], is shown in Fig. 6. In this work, the current sensor pad is shorted to minimize the path inductance. A 100-µH inductor is connected between the ac and the VDC/2 terminals. $C_1$ and $C_2$ are buffer capacitors that supply the energy for the inductor magnetization, $C_1 = C_2 = 3.85$ µF. $R_1$ and $R_2$ are discharging resistors that also have a balancing influence on the voltage distribution when energizing the circuit, $R_1 = R_2 = 1$ MΩ. $L_\sigma$ symbolize parasitic path inductances on the PCB. As can be seen in Fig. 7, the voltage at the ac terminal is measured along with the inductor current $I_{\mathrm{L}}$, and the gate–source voltage

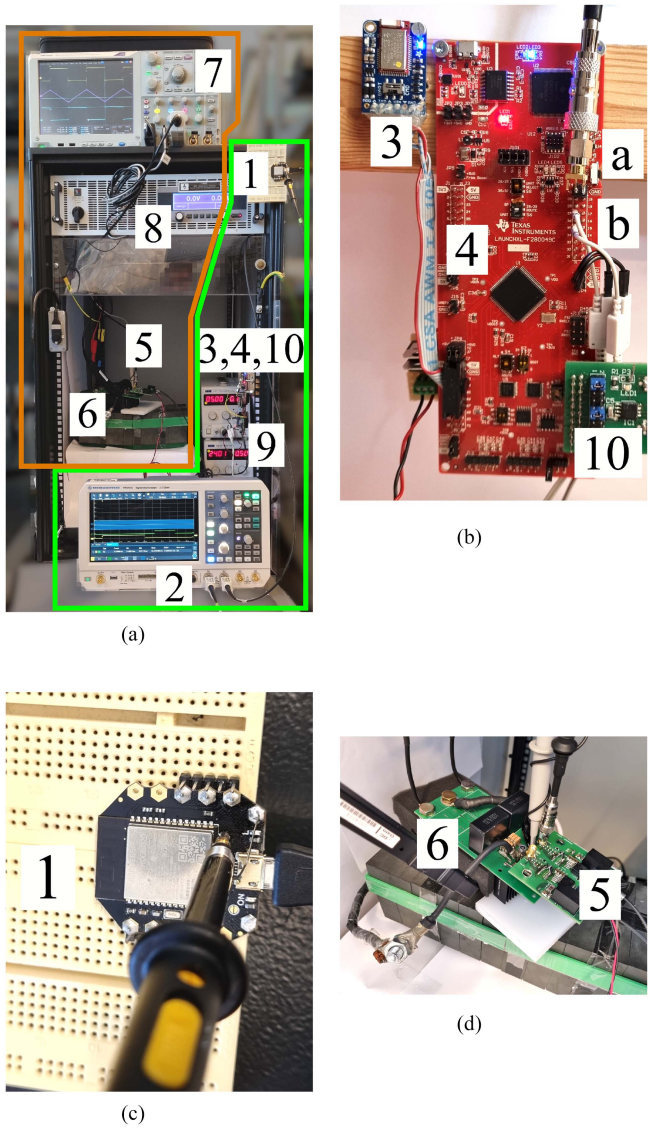


**FIGURE 5.** Wireless AGD control demonstration test setup. 1: ESP32 BLE central, 2: signal oscilloscope, 3: Adafruit BLE Friend BLE peripheral, 4: TMS320F280049C microcontroller board, 5: two-level voltage-source gate driver, 6: LITP with C3M0075120D SiC power MOSFETs on bottom side; inductor, 7: power oscilloscope, 8: dc power supply, 9: auxiliary power supplies for microcontroller board and two-level voltage-source gate driver, and 10: two-level voltage-source gate driver signal interface board. (a) Test setup overview: Signal part in green, power part in orange. (b) Adafruit Bluefruit LE Friend (3) and TMS320F280049C microcontroller board (4) with probes for (a) "ACK" and (b) HB1/HB2 PWM signals. Two-level voltage-source gate driver signal interface board (10). (c) ESP32 microcontroller board with "INIT" signal probe. (d) Two-level voltage-source gate driver (5), LITP with MOSFETs, and inductor underneath (6).

of the low-side MOSFET (DUT in Fig. 6). Both SiC power MOSFETs (DUT and FD in Fig. 6) are controlled by a conventional two-level voltage-source gate driver (IXDN609YI) that provides a high driving voltage of $V_{\mathrm{GG,on,p}} = 15$ V, a low driving voltage of $V_{\mathrm{GG,off,p}} = -5$ V, and a maximum gate current of $I_{\mathrm{g,max,p}} = 9$ A. An external gate resistor of

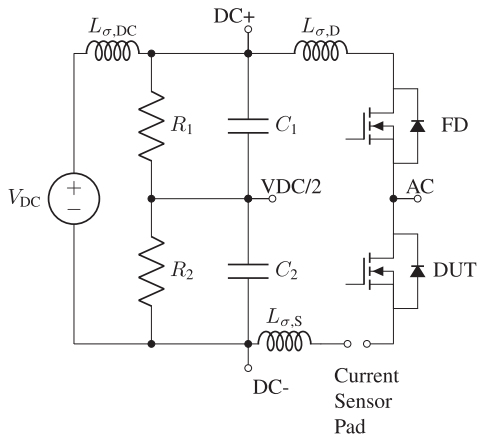


**FIGURE 6.** Idealized schematic diagram of the LITP.

$R_{G,ext,p} = 5.4\ \Omega$ was chosen to keep switching losses low and enable fast switching transitions.

### C. EXPERIMENT PROCEDURE

The following experiment was repeatedly executed to determine the properties of the delay caused by signal transmission by means of UART over BLE. The TMS320F280049C MCU is initialized as the AGD control unit. It sends the three AGD actuator PWM signals continuously at a frequency of $f_{PWM} = 50$ kHz. A BLE connection is established between the ESP32 MCU and the Bluefruit LE Friend.

The ESP32 MCU then first pulls up an output, hereafter referred to as "INIT." Next, the ESP32 MCU immediately proceeds to send out the SCPI message ":TEST:TDON 300\r\n" to the Bluefruit LE Friend, commanding to set $t_{int,on}$ to 300 ns. The message reaches the TMS320F280049C MCU through a gray ribbon cable, which reacts by interpreting and processing the message, choosing the correct action to take, and pulling up an output, hereafter referred to as "ACK." Immediately after that, the TMS320F280049C MCU enacts the requested change in PWM output signals according to the received command. The delay between the rising edges of the "INIT" and "ACK" signals is, in very good approximation, the information transmission delay including information preparation, transmission, reception, and interpretation, as it was defined earlier.

Two variants of this experimental procedure are followed. In the first variant, the power part is de-energized ($V_{DC} = 0$ V), so that no current is flowing in the inductor, and no fast switching slopes are present. In the second variant, the power part is energized ($V_{DC} = 800$ V), which results in a triangular inductor current with an amplitude of 20 A, i.e., 12 Arms. An exemplary measurement obtained from the oscilloscope in the power part of the test setup is shown in Fig. 8. The depicted waveforms comprise the gate–source voltage of the low-side MOSFET installed on the LITP ($V_{gs}$), its drain–source voltage, that is equal to the ac terminal voltage ($V_{ds} = V_{AC}$), as well as the inductor current ($I_L$), while the power part is energized at a voltage of $V_{DC} = 800$ V. The voltage transitions are very fast, with manually determined transition rates of 52.2 kV/µs averaged between 10% and 90% of $V_{DC}$. When the power part of the test setup is energized, this switching pattern continuously repeats in direct vicinity (less than 20 cm) of the Bluefruit LE Friend and TMS320F280049C microcontroller.

### D. EXPERIMENTAL RESULTS

An exemplary measurement result obtained from the oscilloscope in the signal part of the test setup, while conducting a single experiment following the procedure described above, is shown in Fig. 9. It depicts the AGD actuator control signals with a PWM frequency of $f_{PWM} = 50$ kHz provided to the half-bridge circuits HB1 and HB2 of the AGD, and the "INIT" and "ACK" signals that indicate the information transmission initiation and completion. The control signal periods are not visible, as one period of the PWM signals is very short compared to the delay introduced by the information transmission. To illustrate the influence of the transmitted command on the PWM signals, two zoomed-in views of the control signals directed to HB1 and HB2 are shown in addition. It is clearly visible that the delay between the control signals for HB1 and HB2 increases from an almost invisible 20 ns before the transmission (shown in the red rectangle in Fig. 9) to 300 ns after the transmission (shown in the green rectangle in Fig. 9). This particular experimental result exhibits an information transmission delay of 23.1 ms.

As explained above, wireless control of the AGD is used to provide high-level control signals to the AGD, such as the change of $t_{int,on}$ in the given example. Thereby, the control of switching performance in regard to, for example, the switching loss energies, can be achieved. In particular, increasing $t_{int,on}$ for a constant $V_{int,on}$ will result in increased switching energy during turn-ON process and, simultaneously, a decrease of voltage slope steepness of a SiC power MOSFET controlled by the AGD, as discussed in Section IV-A.

The experiment described above demonstrates the general possibility of using BLE for wireless AGD control. However, only a large number of experiments can serve as evidence showing that the delay introduced by BLE is acceptable for the intended applications. Therefore, the information transmission delay measurement experiment was repeated 10 000 times, so that a statistical delay characteristic could be derived. As mentioned before, the experiments were conducted with the power part of the test setup de-energized first and then again with the power part energized. The delays measured throughout all these experiments are visualized in Fig. 10. The bottom part of Fig. 10 shows a histogram of the measured delay times in both experiment variants: "signal" denoting the variant without the power part de-energized and "power" with the power part of the test setup energized. The histograms of these two experiment variants overlap in large parts. To improve visibility, a third color was used to indicate this overlap. The upper two diagrams give a statistical interpretation of the measured data in the form of a boxplot diagram, indicating the minimum and maximum values with caps (vertical lines),

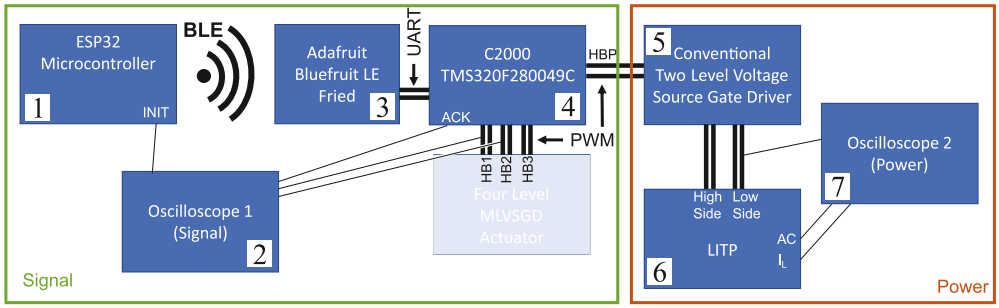


**FIGURE 7.** Schematic diagram of the experimental test setup.

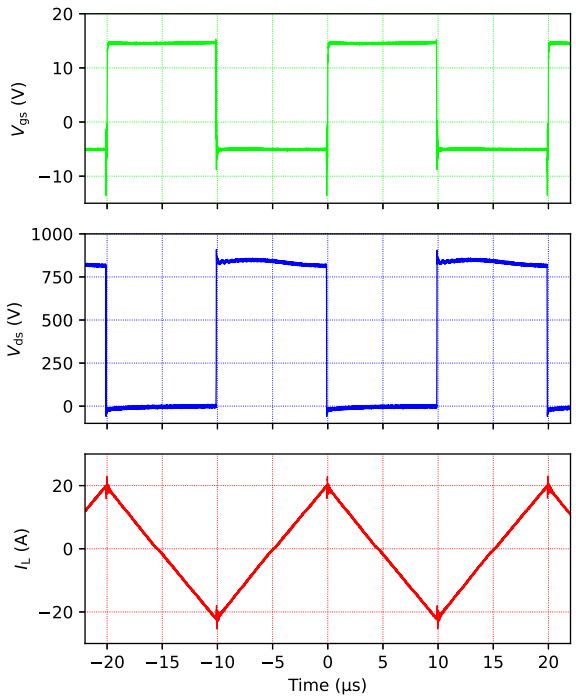


**FIGURE 8.** Gate–source voltage ($V_{gs}$), drain–source voltage ($V_{ds}$, equal to the ac terminal voltage $V_{ds} = V_{AC}$), and inductor current waveform of the power part of the test setup when energized.

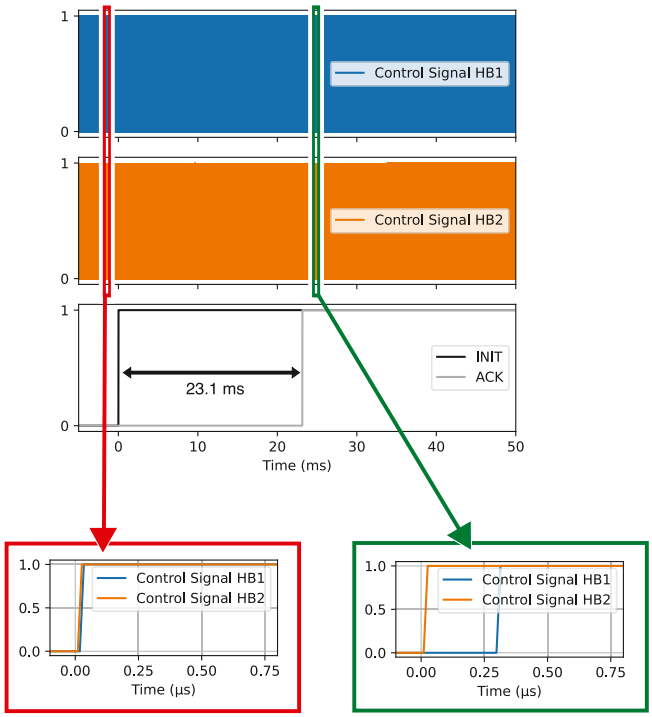


**FIGURE 9.** Control signals for HB1 and HB2 of the four-level MLVSGD Actuator during an example experiment. The rising edge of the "INIT" signal coincides with the initiation, and the rising edge of "ACK" with the gate driver having successfully interpreted the command transmitted over BLE.

the upper and lower quartile as (vertical) box boundaries, the mean value with a diamond shaped mark, and the median with a dotted line. Values that are located further away from the upper quartile than 1.5 times the range between upper and lower quartile are interpreted as outliers and indicated with circles.

With the power part of the test setup de-energized, the average information transmission delay is 26.6 ms, and the absolute extremes are 20.9 and 41.2 ms. With the power part of the test setup energized, the average information transmission delay is 26.4 ms, and the absolute extremes are 20.9 and 44.5 ms. This means that in the continuous presence of fast switching voltage and current transitions in the direct vicinity of the Bluefruit LE Friend BLE peripheral device, the delay times do not systematically increase. However, more measurements are counted as outliers, and the absolute maximum delay time is 8% longer than with a de-energized power part. Otherwise, the experimental results of the two experiment variants are almost identical.

### *E. DISCUSSION*

It was expected that the presence of fast switching slopes does not have a significant influence on the information transmission over BLE because of the difference in operation frequency of approximately one decade (see Section I). While a weak effect on the worst case delay time can be observed, the increase in information transmission delay time is not detrimental. It could be confirmed that the latency introduced

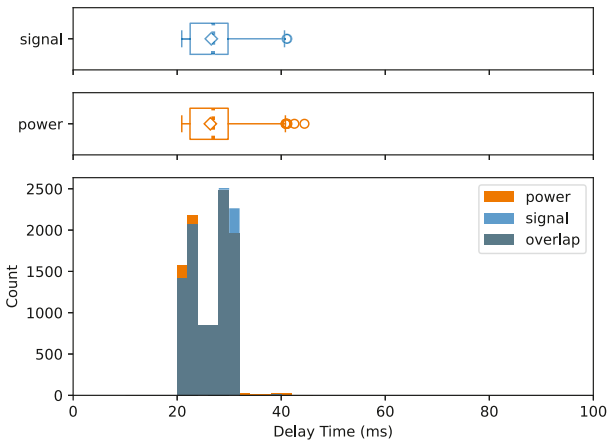


**FIGURE 10.** **Information transmission delay measurement result.**

by BLE is by far shorter than 100 ms, as stated in Table 2, even in a practical scenario with fast switching transitions near the wireless hardware. This proves that BLE is suitable for realizing AL4 ITRs under the definition given in Section II-B.

The string ":TEST:TDON 300" consists of 15 characters plus 2 end-of-line characters. The information transmitted over UART equals $17 \times 8$ bit $= 136$ bit. With a symbol rate of 9600 Bd, which is the maximum recommended for the Bluefruit LE Friend [33], and a symbol length of 1 bit, the transmission of this string takes 14.2 ms. Optimizing the command alphabet could, therefore, significantly improve the information transmission delay.

The experimental results show that the wireless connection between the ESP32 and TMS320F280049C MCUs over BLE can be realized with an information transmission delay below 40 ms. This enables control over, for example, the switching losses and voltage and current slopes in the AGD driven SiC MOSFET. As mentioned earlier, possible applications include active temperature control, EMI control, and efficiency optimization.

## V. CONCLUSION

This article provided a practical approach for assessing the use of WCT for information transmission in PESs. A basic future PES structure that incorporates active gate drivers and incorporates ITRs was presented, and the characterization of ITRs was systematized with a novel ITR taxonomy. Seven specific WCTs were characterized with respect to their latency, range, and data rate. For every ITR, a recommendation for or against using WCTs was given, and suitable WCTs among the previously presented were indicated. In particular, the ITR between converter and AGD control received special attention by examining safety and security implications in greater detail.

With its focus on converter-level signal transmission, the proposed taxonomy is a useful tool for power electronics engineers who consider using wireless ITRs to improve the converter design, and it also helps to coordinate efforts between design engineers that each are responsible for different components within a PES. In addition, the taxonomy helps to define an interface to grid control for the interconnected electrical network of the future.

Experimental results demonstrated the control of a four-level MLVSGD by means of UART over BLE. The results showed that using this WCT, a remote MCU can exert full control over the features of an AGD. For example, the switching losses of the SiC MOSFET driven by the four-level MLVSGD can be manipulated with an associated information transmission delay below 45 ms, which is sufficient for applications such as active temperature control and EMI control.

## REFERENCES

[1] J. Biela, M. Schweizer, S. Waffler, and J. W. Kolar, "SiC versus Si—Evaluation of potentials for performance improvement of inverter and DC–DC converter systems by SiC power semiconductors," *IEEE Trans. Ind. Electron.*, vol. 58, no. 7, pp. 2872–2882, Jul. 2011.

[2] J. Henn et al., "Intelligent gate drivers for future power converters," *IEEE Trans. Power Electron.*, vol. 37, no. 3, pp. 3484–3503, Mar. 2022.

[3] X. Ding, X. Song, Z. Zhao, Z. Shan, and B. Wang, "Active junction temperature control for SiC MOSFETs based on a resistor-less gate driver," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 5, pp. 4952–4964, Oct. 2022.

[4] G. L. Rødal and D. Peftitsis, "An adaptive current-source gate driver for high-voltage SiC MOSFETs," *IEEE Trans. Power Electron.*, vol. 38, no. 2, pp. 1732–1746, Feb. 2023.

[5] Y. Yang, Y. Wen, and Y. Gao, "A novel active gate driver for improving switching performance of high-power SiC MOSFET modules," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7775–7787, Aug. 2019.

[6] S. Zhao, X. Zhao, A. Dearien, Y. Wu, Y. Zhao, and H. A. Mantooth, "An intelligent versatile model-based trajectory-optimized active gate driver for silicon carbide devices," in *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 429–441, Mar. 2020.

[7] R. Li et al., "Dynamic gate drive for SiC power MOSFETs with sub-nanosecond timings," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2023, pp. 324–330.

[8] H. B. Ekren, D. A. Philipps, G. L. Rødal, and D. Peftitsis, "Four level voltage active gate driver for loss and slope control in SiC MOSFETs," in *Proc. IEEE 13th Int. Symp. Power Electron. Distrib. Gener. Syst.*, 2022, pp. 1–6.

[9] K. Miyazaki et al., "General-purpose clocked gate driver IC with programmable 63-level drivability to optimize overshoot and energy loss in switching by a simulated annealing algorithm," *IEEE Trans. Ind. Appl.*, vol. 53, no. 3, pp. 2350–2357, May/Jun. 2017.

[10] S. Zhao et al., "Adaptive multi-level active gate drivers for SiC power devices," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1882–1898, Feb. 2020.

[11] S. Zhao, X. Zhao, Y. Wei, Y. Zhao, and H. A. Mantooth, "A review of switching slew rate control for silicon carbide devices using active gate drivers," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 4, pp. 4096–4114, Aug. 2021.

[12] W. T. Cui et al., "A dynamic gate driver IC with automated pattern optimization for SiC power MOSFETs," in *Proc. IEEE 34th Int. Symp. Power Semicond. Devices ICs*, 2022, pp. 33–36.

[13] H. Obara, K. Wada, K. Miyazaki, M. Takamiya, and T. Sakurai, "Active gate control in half-bridge inverters using programmable gate driver ICs to improve both surge voltage and switching loss," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 1153–1159.

[14] V. Grau and R. W. D. Doncker, "The effects of steep voltage slopes on insulation systems of coil windings caused by next generation power semiconductor devices," in *Proc. IEEE Elect. Insul. Conf.*, 2019, pp. 26–29.

[15] C. Luedecke, G. Engelmann, and R. W. D. Doncker, "Optimized IGBT turn-on switching performance using the full device safe operating area," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, 2019, pp. 1–8.

[16] C. Lüdecke, G. Engelmann, and R. W. D. Doncker, "Optimized IGBT turn-off switching performance using the full device safe operating area," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2019, pp. 1319–1325.
[17] H. Riazmontazer, A. Rahnamaee, A. Mojab, S. Mehrnami, S. K. Mazumder, and M. Zefran, "Closed-loop control of switching transition of SiC MOSFETs," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2015, pp. 782–788.
[18] Z. Zhang, J. Dix, F. F. Wang, B. J. Blalock, D. Costinett, and L. M. Tolbert, "Intelligent gate drive for fast switching and crosstalk suppression of SiC devices," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9319–9332, Dec. 2017.
[19] S. Kalker, C. H. van der Broeck, and R. W. D. Doncker, "Online junction-temperature sensing of SiC MOSFETs with minimal calibration effort," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, 2020, pp. 1–7.
[20] K. Yamamoto, F. Ichihara, K. Hasegawa, M. Tukuda, and I. Omura, "60 GHz wireless signal transmitting gate driver for IGBT," in *Proc. IEEE 27th Int. Symp. Power Semicond. Devices ICs*, 2015, pp. 133–136.
[21] J.-J. Lin, J.-L. Lin, and W.-T. Shen, "Implementation of a wireless controlled gate driver," in *Proc. IEEE 2nd Int. Conf. Circuits, System Simul.*, 2018, pp. 17–21.
[22] J.-J. Lin, "Design and implementation of a wirelessly powered and controlled gate driver," *IEEE J. Radio Freq. Identification*, vol. 5, no. 1, pp. 40–45, Mar. 2021.
[23] Y. Tsutsumi, K. Akita, H. Kitagawa, K. Suzuki, R. Saito, and Y. Tawada, "High-speed and low-latency transmission by millimeter-wave digital wireless system for Si-IGBT/SiC-MOSFET driver control," in *Proc. Int. Power Electron. Conf.*, 2022, pp. 2275–2279.
[24] K. Sung, Y. Ouchi, S. Amagai, K. Sagara, Y. Kawasaki, and H. Sung, "Gate drive method using wireless multiplex transmission of power and signal," in *Proc. Int. Power Electron. Conf.*, 2022, pp. 2082–2087.
[25] S. Brehaut and F. Costa, "Gate driving of high power IGBT by wireless transmission," in *Proc. CES/IEEE 5th Int. Power Electron. Motion Control Conf.*, 2006, pp. 1–5.
[26] C. Batard, G. Andrieux, N. Ginot, and M. A. Mannah, "Wireless transmission of IGBT driver control," in *Proc. IEEE 24th Annu. Appl. Power Electron. Conf. Expo.*, 2009, pp. 1257–1262.
[27] P. Bogónez-Franco and J. B. Sendra, "EMI comparison between Si and SiC technology in a boost converter," in *Proc. Int. Symp. Electromagn. Compat.*, 2012, pp. 1–4.
[28] W. Ma, Y. Wu, H. Li, and D. Chu, "Investigation of the gate resistance and the RC snubbers on the EMI suppression in applying of the SiC MOSFET," in *Proc. IEEE Int. Conf. Mechatron. Autom.*, 2019, pp. 2224–2228.
[29] G. C. Montanari and F. Ciani, "Inverter design and partial discharge phenomenology in insulation systems of rotating machines," in *Proc. IEEE Int. Electr. Mach. Drives Conf.*, 2017, pp. 1–5.
[30] K. T. McDonald, "Capacitance of a thin conducting disk and of conducting spheroids," Feb. 25, 2003. Accessed: Jul. 13, 2023. [Online]. Available: http://kirkmcd.princeton.edu/examples/thindisc.pdf
[31] D. A. Philipps, T. N. Ubostad, and D. Peftitsis, "Low inductive platform for long- and short-term dynamic characterization of SiC MOSFETs," in *Proc. Int. Power Electron. Conf.*, 2022, pp. 2621–2627.
[32] D. A. Philipps, P. Xue, T. N. Ubostad, F. Iannuzzo, and D. Peftitsis, "Low inductive characterization of fast-switching SiC MOSFETs and active gate driver units," *IEEE Trans. Ind. Appl.*, vol. 59, no. 5, pp. 6384–6398, Sep./Oct. 2023.
[33] *Adafruit Bluefruit LE UART Friend—Bluetooth Low Energy (BLE)*, Adafruit Industries, New York, NY, USA. Accessed: Jan. 25, 2023. [Online]. Available: https://www.adafruit.com/product/2479

**DANIEL A. PHILIPPS** (Student Member, IEEE) was born in Moers, Germany, in 1994. He received the B.Sc. and M.Sc. degrees in distribution grid stability and low-power dc–dc conversion from RWTH Aachen University, Aachen, Germany, in 2016 and 2020, respectively. He is currently working toward the Ph.D. degree in adaptive gate-driving methods for medium-voltage applications with the Norwegian University of Science and Technology, Trondheim, Norway.

**DIMOSTHENIS PEFTITSIS** (Senior Member, IEEE) was born in Kavala, Greece. He received the Diploma degree (Hons.) in electrical and computer engineering from the Democritus University of Thrace, Xanthi, Greece, in 2008, and the Ph.D. degree in the field of power electronics from the KTH Royal Institute of Technology, Stockholm, Sweden, in 2013.

He is currently a Professor of Power Electronics with the Department of Electric Energy, Norwegian University of Science and Technology (NTNU), Trondheim, Norway, where he has been a Faculty Member since 2016. In his final year of studies, he spent six months with ABB Corporate Research, Västerås, Sweden, writing his thesis. From 2013 to 2014, he was a Postdoctoral Researcher involved in the research on SiC converters with the Department of Electrical Energy Conversion, KTH Royal Institute of Technology, Stockholm, Sweden. He was a Postdoctoral Fellow with the Laboratory for High Power Electronics Systems, ETH Zürich, Zürich, Switzerland, where he was involved in dc breakers for multiterminal high-voltage dc (HVDC) systems from 2014 to 2016. He has authored or coauthored more than 80 journal and conference papers. He is the coauthor of one book chapter and the presenter of five conference tutorials. His research interests include power converter design using wide-bandgap devices (e.g., SiC and GaN) including adaptive drive circuits, dc-breaker design for medium-voltage dc and HVDC systems, as well as reliability assessment and lifetime modeling of high-power semiconductor devices, including reliability of SiC power switches.

Dr. Peftitsis is a Member of the Outstanding Academic Fellows Program of NTNU, a Member of the EPE International Scientific Committee, and an Academic Advisor for the Power Electronic Conversion Technology Annex, International Energy Agency. He is the Chairman on the Norway IEEE Power Electronics Society/IEEE Industry Applications Society/IEEE Industrial Electronics Society Joint Chapter.