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Cascaded Multilevel Structure With Three-Phase and Single-Phase H-Bridges for Open-End Winding Induction Motor Drive

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ABSTRACT A new multilevel topology for an open-end winding motor drive is proposed in this article, presenting a similar structure to the cascaded H-bridge multilevel inverter. The proposed topology combines three-phase and single-phase conventional H-bridge voltage source inverters. The topology is flexible, allowing to increase the number of voltage levels through the simple integration of new single-phase H-bridge inverters connected in wye. Based on this topology, it is possible to obtain two different configurations. These modular multilevel topologies can be easily extended, both in terms of voltage level and the number of voltage levels. The topology is characterized by the capability to a supply higher voltage to the motor windings or use lower dc voltages when compared with classical solutions. Well-known modulation schemes, such as the multilevel sinusoidal pulsewidth modulation technique, can be easily adapted to the proposed topology. The operation and characteristics of the two configurations for the proposed multilevel topology are confirmed by several experimental tests realized through a laboratory prototype.

INDEX TERMS Multilevel inverter, cascaded, H-bridge, open-end windings, sinusoidal pulsewidth modulation (SPWM) modulation.

I. INTRODUCTION

Inductionmotors are widely used in transportation and industrial applications [1], [2], due to their important and interesting characteristics, such as simple and rough construction, high reliability, low maintenance, and low cost. Nevertheless, over the last decades this machine (especially the three-phase type) has been extended to other areas, such as household appliances [3], aeronautics [4], medical devices [5], new traction applications (e.g., electric vehicles and electric scooters) [6], [7], among others. In many industrial applications an *ac* motor drive is required to control the motor speed. These drives are also essential for the electrical transportation. The conventional power circuit topology used in *ac* drives has been the three-phase two-level voltage source inverter (*VSI*), especially in low voltage. However, for *ac* medium voltage three-phase two-level *VSIs* present many limitations, mainly the required power semiconductors relatively high-blocking voltage capability. Multilevel topologies [8], [9], [10], [11] emerged as a solution to mitigate this drawback since they allow the use of power semiconductors with a reduced blocking voltage, while reducing the *ac* voltage harmonic distortion. This last property is valuable even for low-voltage applications.

Due to the abovementioned advantages, many multilevel topologies have been developed and implemented in *VSI* drives. The most known, studied and used are the neutral-point-clamped (*NPC*), the flying capacitor, cascaded H-bridge

topologies, and T-Type [12], [13], [14], [15], [16], [17], [18]. The first two topologies need to balance the capacitors voltages, requiring more elaborated control systems [19], [20], [21], [22]. Meanwhile, many multilevel topologies have been proposed, mainly to overcome capacitor voltage balance issues while retaining the multilevel advantages. Among the new proposals, the modular multilevel converter (*MMC*) is receiving special attention, even for medium voltage motors [23], [24], [25], [26].

A different approach to provide multilevel voltages in drives is to use induction motors with open-end windings (with two accessible terminals per winding). This kind of topology was initially described in [4] and is now considered as an alternative approach, as it allows obtaining multilevel phase voltage waveforms [14]. Associated with this kind of drives, there are very interesting advantages over the conventional ones, such as the reduced component count [9], [14] (when compared with the classical equivalent neutral-point-clamp and flying capacitor converters for example), operation over a wider speed range (or use of switches with reduced blocking voltage) and no floating neutral point [27], [28]. In this way, one of the industry proven is the drive with two-level *VSIs*. In this case, the resulting multilevel *VSI* topology will be connected to both terminals of each winding. This topology uses two-level *VSIs* to increase the number of voltage levels (NVL) with fewer modules and to improve the reliability and resilience to *VSI* semiconductor faults [29], [30]. Earlier topologies proposed for open-end winding motors use two conventional three-phase *VSIs*, each one connected to one of the sides of the open-end windings [31], [32], [33]. With this multilevel *VSI* topology, considering the two *dc* voltage sources with the same value, nine voltage levels can be applied to each winding. However, this topology does not allow an easy extension of the NVL while control strategies and modulators are complex. To extend the voltage levels, the new solution first proposed in [34] uses two three-phase two-level inverters fed by two *dc* sources and six single-phase two-level inverters connected to floating capacitors. Another topology that uses two two-level inverters in cascade connected in one side of the motor windings and a single two-level inverter from the other side was also proposed [35]. Multilevel inverter topologies using a combination of single-phase two-level inverters with three-level *NPC* inverters were also proposed [36], [37]. However, all these multilevel inverters require complex control and modulator subsystems. On the other hand, these last two structures require a high number of switches, as well as, switches with different maximum blocking voltage. It is also not clear how it can be extended to more voltage levels, and in a flexible way. Therefore, a topology using just three conventional two-level three-phase inverters was proposed in [36]. This inverter topology allows implementing well-known modulation techniques, such as sinusoidal pulsewidth modulation (*SPWM*). However, the topology in [38] does not allow an easy extension of the of voltage levels.

As described, drives using induction motors with open-end windings present some advantages over the conventional ones, leading in the last years to several research works addressing open-end windings motor drives. As stated, several multilevel topologies have been proposed for this kind of drives. However, some topologies do not allow increasing the NVL, while some others do not use modular configurations and many topologies require complex control systems. Taking into consideration these aspects, a new multilevel modular topology for open-end winding induction motor drive is proposed. This new topology was developed to present the following features.

1) New modular multilevel topologies that can be easily extended, both in terms of voltage level and NVL.
2) Multilevel topologies based on industry proven H-bridges (three-phase and single-phase) in modular configurations, ensuring industrial scalability, higher power quality, and fault-tolerant capability.
3) Topologies that can operate using industry accepted PWM modified modulators.
4) Topologies capable of operation in fault-tolerant mode in the event of an open-switch fault without adding any extra components or changing the modulation strategy.

The hereafter proposed solution is suitable for several applications, including induction motor drives of electric transportation vehicles.

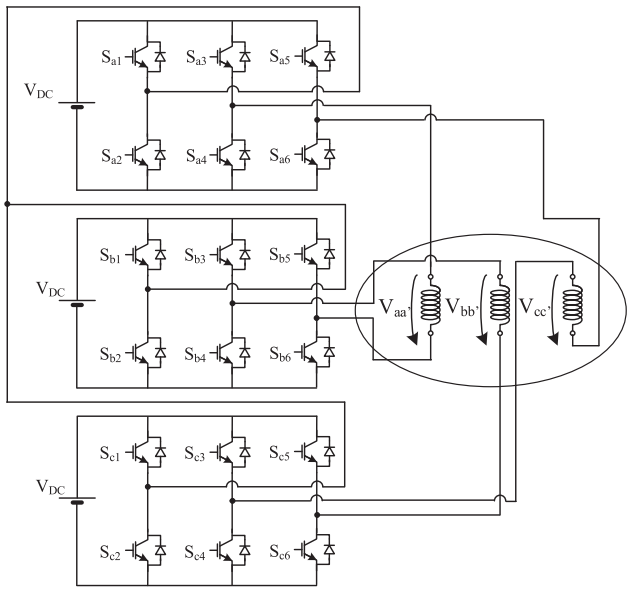

FIGURE 1. Basic multilevel inverter topology for open-end windings induction motor drive [38].

II. PROPOSED SOLUTION

The proposed circuit topology for the open-end winding induction motor drive is derived from the topology using three three-phase two-level inverters proposed by [38] (see Fig. 1). The three three-phase two-level inverters are fed by separate *dc* voltage sources and phase *A* in each one of the three inverters are all connected together (in wye). The two remaining output phases of each inverter are connected to the terminals of two different stator windings (see Fig. 1). This topology

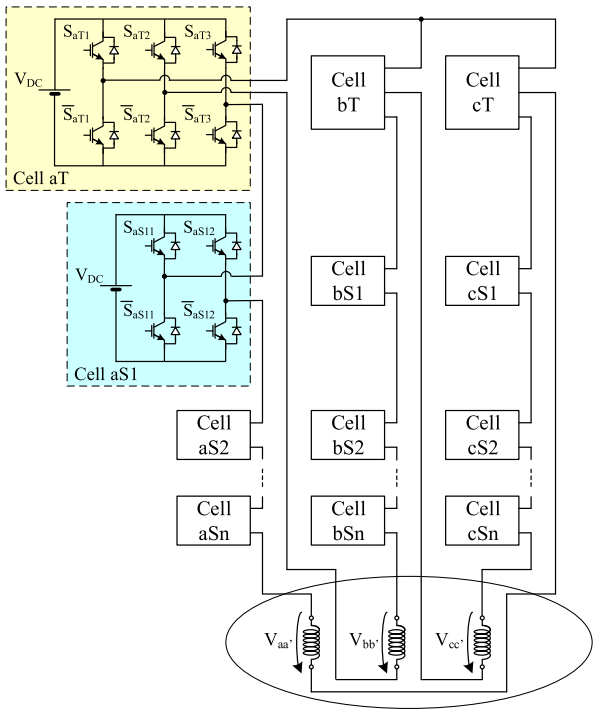

FIGURE 2. **Proposed new T–S cells multilevel inverter topology of the *n*-level proposed multilevel inverter with the windings connected to the single-phase inverters.**

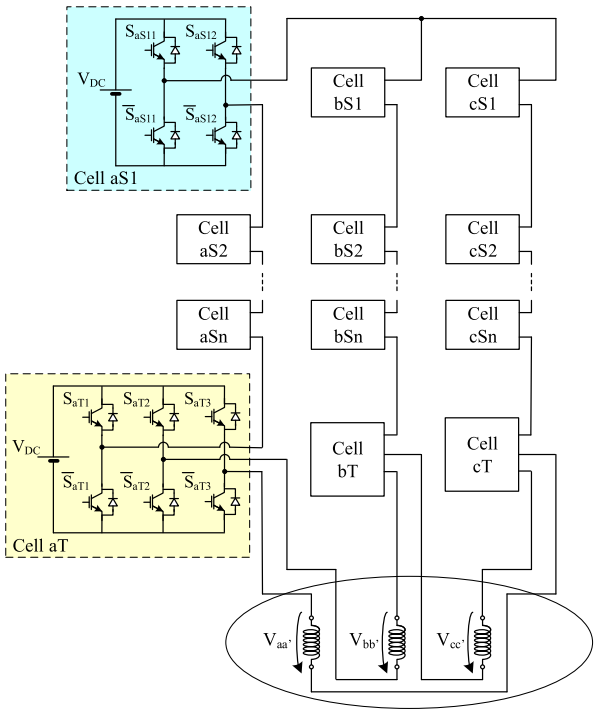

FIGURE 3. **Proposed new S–T cells multilevel inverter topology of the *n*-level proposed multilevel inverter with the windings connected to the three-phase inverters.**

allows five voltage levels at the motor windings. It also allows windings maximum voltages that double the *dc* voltage sources value.

The topology of Fig. 1 lacks flexibility as it is not modular, being unclear how to extend the NVL. In fact, the classic approach of using more identical inverters (three-phase) to obtain the extension to the NVL is not suitable for this structure. Thus, instead of using the same type of inverters (as usually), this work proposes a hybrid approach, where different types of H-bridge inverters are merged. The hereafter proposed new multilevel topology uses a combination of single-phase two-level VSIs and three-phase two-level *VSIs*. This new approach can achieve extended voltage levels just by increasing the number of power converters, maintaining modularity. Fig. 2 illustrates the proposed cascaded topology for the extended voltage levels. This new topology connects three-phase two-level inverters with single-phase two-level H-bridge inverters in a cascaded connection. The new inverter topology uses a combination of three three-phase inverters (each called Cell *T*) with single-phase inverters (each called Cell *S*). The motor windings are connected to the single-phase inverters (Cell *S*), and one phase in each three-phase inverter (Cell *T*) is connected to establish the wye connection. The modularity of the *T–S* cells multilevel inverter is still maintained requiring only two different cells.

Besides the increase of the voltage applied to the motor windings, the cascade *T–S* cells inverter topology also allows obtaining an important increase of the NVL. For example, considering one set of cells *S* (one single-phase bridge per leg), the NVL applied to each motor winding increases from five to seven ($+3V_{DC}$, $+2V_{DC}$, $+1V_{DC}$, 0, $-1V_{DC}$, $-2V_{DC}$, $-3V_{DC}$). These voltage levels are related to 64 possible switching combinations for each motor winding. This high number of switching combinations means that there are redundant combinations for some voltage levels. The redundant combinations exist in the intermediate voltage levels. In fact, for this proposed topology for the $\pm 2V_{DC}$ there are six redundant switch combinations, for the $\pm V_{DC}$ there are 11 redundant switch combinations and for the zero-voltage level there are 28 redundant switch combinations.

The generic expression for the *NVL* obtained using the cascaded *T–S* cells multilevel inverter with n sets of cells *S* is given by

$$N_{VL} = 7 + 2(n - 1). \tag{1}$$

The *T–S* cells inverter topology can be strongly improved to allow the increase of the NVL without increasing the number of bridge inverters. In the improved variant (see Fig. 3), the position of the three *T* cells and the n sets of *S* cells are interchanged. Analyzing this new *S–T* cells inverter topology, it is possible to see that the motor windings will now connect to the three-phase inverters instead of the single-phase inverters. The wye connection is now made through one terminal of the three single-phase inverters.

Using the same example of the previous topology (one set of cells *S*), it is possible to verify that the NVL applied to each motor winding now increases from five to nine ($+4V_{DC}$,

$+3V_{DC}, +2V_{DC}, +1V_{DC}, 0, -1V_{DC}, -2V_{DC}, -3V_{DC}, -4V_{DC}$). The number of possible switching combinations increases from 64 to 256 in this new topology. As in the previous topology, there are redundant switching combinations related with the intermediate voltage levels. Thus, in this new proposed topology for the $\pm 3V_{DC}$, there are eight redundant switches combinations, and 28 redundant switches combinations for the $\pm 2V_{DC}$. For the $\pm V_{DC}$, there are 56 redundant switches combinations, and for the zero-voltage level, there are 70 redundant switches combinations.

In this topology, considering a cascade inverter topology with n sets of cells S, the generic expression for the NVL is given by

$$N_{VL} = 9 + 2(n-1). \tag{2}$$

From the point of view of the NVL and maximum voltage applied to the motor windings, the S–T cells inverter topology is more advantageous regarding the T–S cells inverter.

One of the aspects that can be pointed out to these topologies is regarding the low impact on their cost when comparing with classical solutions. From the cost point of view, in high voltage (HV), the proposed solutions is equivalent to usual solutions (as the number of converters is the same), and the main difference in cost is due to the substitution of one two-branch converter by a three-branch converters. In this way, the increase in cost can be compensated by the saving in energy (as losses are lower taking into consideration the voltage levels) or by needing smaller filters (as current quality is bigger).

It should be noted that the proposed topologies adhere to the philosophy of multilevel cascaded H-bridge converters, which prevents sharing the single dc voltage source. In the case of a galvanic isolated dc/dc converter (with multiple winding outputs), the different dc voltage sources can be implemented in such a way that only a single ac/dc converter is used (single connection to the ac voltage source).

III. PROPOSED CONVERTERS ANALYSIS

A. CONVERTERS MODELLING

The voltage level to be applied to each motor winding is determined by the state of the power semiconductors. Indeed, those power semiconductors can be modeled as binary variables (γ), as shown by the expressions in the following (where $i \in \{a,b,c\}$, $j \in \{1,..,n\}$, and $k \in \{1,2,3\}$):

$$\gamma_{iTk} = \begin{cases} 1 & \text{if} \quad S_{iTk} \text{ is ON} \quad \wedge \quad \bar{S}_{iTk} \text{ is OFF} \\ 0 & \text{if} \quad S_{iTk} \text{ is OFF} \quad \wedge \quad \bar{S}_{iTk} \text{ is ON} \end{cases} \tag{3}$$

$$\gamma_{iSjk} = \begin{cases} 1 & \text{if} \quad S_{iSjk} \text{ is ON} \quad \wedge \quad \bar{S}_{iSjk} \text{ is OFF} \\ 0 & \text{if} \quad S_{iSjk} \text{ is OFF} \quad \wedge \quad \bar{S}_{iSjk} \text{ is ON.} \end{cases} \tag{4}$$

Using the previous variables, expressions for the voltages applied to the load function of the switch's state can now be established. As a result, the applied voltages to the motor windings for the T–S configuration (where n is the number of cells S sets in cascade connection) will be given by

$$v_{aa'} = (\gamma_{aT3} - \gamma_{aT1})V_{DC} + (\gamma_{cT1} - \gamma_{cT2})V_{DC} + (\gamma_{aS12} - \gamma_{aS11})V_{DC} + \cdots + (\gamma_{aSn2} - \gamma_{aSn1})V_{DC} \tag{5}$$

$$v_{bb'} = (\gamma_{bT3} - \gamma_{bT1})V_{DC} + (\gamma_{aT1} - \gamma_{aT2})V_{DC} + (\gamma_{bS12} - \gamma_{bS11})V_{DC} + \cdots + (\gamma_{bSn2} - \gamma_{bSn1})V_{DC} \tag{6}$$

$$v_{cc'} = (\gamma_{cT3} - \gamma_{cT1})V_{DC} + (\gamma_{bT1} - \gamma_{bT2})V_{DC} + (\gamma_{cS12} - \gamma_{cS11})V_{DC} + \cdots + (\gamma_{cSn2} - \gamma_{cSn1})V_{DC}. \tag{7}$$

Regarding the S–T configuration, the applied voltages to the motor windings will now be given by (where n is the number of cells S sets in cascade connection)

$$v_{aa'} = (\gamma_{aS12} - \gamma_{aS11})V_{DC} + \cdots + (\gamma_{aSn2} - \gamma_{aSn1})V_{DC} + (\gamma_{cS11} - \gamma_{cS12})V_{DC} + \cdots + (\gamma_{cSn1} - \gamma_{cSn2})V_{DC} + (\gamma_{aT3} - \gamma_{aT1})V_{DC} + (\gamma_{cT1} - \gamma_{cT2})V_{DC} \tag{8}$$

$$v_{bb'} = (\gamma_{bS12} - \gamma_{bS11})V_{DC} + \cdots + (\gamma_{bSn2} - \gamma_{bSn1})V_{DC} + (\gamma_{aS11} - \gamma_{aS12})V_{DC} + \cdots + (\gamma_{aSn1} - \gamma_{aSn2})V_{DC} + (\gamma_{bT3} - \gamma_{bT1})V_{DC} + (\gamma_{aT1} - \gamma_{aT2})V_{DC} \tag{9}$$

$$v_{cc'} = (\gamma_{cS12} - \gamma_{cS11})V_{DC} + \cdots + (\gamma_{cSn2} - \gamma_{cSn1})V_{DC} + (\gamma_{bS11} - \gamma_{bS12})V_{DC} + \cdots + (\gamma_{bSn1} - \gamma_{bSn2})V_{DC} + (\gamma_{cT3} - \gamma_{cT1})V_{DC} + (\gamma_{bT1} - \gamma_{bT2})V_{DC}. \tag{10}$$

These equations also confirm the number of switching combinations and the redundant combinations for each voltage level.

From the previous equations, it is also possible to determine the minimum level of the inverters dc voltage source. Thus, considering a classical SPWM modulation strategy (explained in the following sections), the minimum level is given in the following for the T–S and S–T configurations, respectively:

$$V_{DC\ T-S} = \frac{v_{wind\_max}}{n} \tag{11}$$

$$V_{DC\ S-T} = \frac{v_{wind\_max}}{2n} \tag{12}$$

where v_{wind_max} is the maximum voltage applied to the motor winding and n is the number of converters per leg.

To see that the open-end winding proposed topologies, namely, the S–T configuration, allow using a lower minimum level of the inverters dc voltage source, a comparison to the classical cascaded H-bridge multilevel topology is done [15]. For the H-bridge topology, the minimum level of the inverters dc voltage source can be determined by (13). Comparing this result with the one associated with the S–T configuration (12), it is seen that the open-end winding S–T configuration allows a 50% reducing of the related minimum level of the inverters dc voltage source.

$$V_{DC\ cascaded\_H-Bridge} = \frac{v_{wind\_max}}{n}. \tag{13}$$

Regarding the dynamic model of the converter, it is given by the following differential equations when considering the simplified classical equivalent model of the induction motor (*RLE* load):

$$\frac{d}{dt}\begin{bmatrix} i_{aa'} \\ i_{bb'} \\ i_{cc'} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & 0 & 0 \\ 0 & -\frac{R}{L} & 0 \\ 0 & 0 & -\frac{R}{L} \end{bmatrix} \begin{bmatrix} i_{aa'} \\ i_{bb'} \\ i_{cc'} \end{bmatrix} + \frac{1}{L}\begin{bmatrix} E_1 \\ E_2 \\ E_3 \end{bmatrix} + \frac{1}{L}\begin{bmatrix} v_{aa'} \\ v_{bb'} \\ v_{cc'} \end{bmatrix}. \tag{14}$$

As an example of a model of the proposed inverters, let us consider the basic configuration (the one with the fewest inverters, i.e., with only one set of cells *S*. The voltages applied to the motor in this case will be given by (15) for the *T*–*S* cells and (16) for the *S*–*T* cells.

$$\begin{aligned} \begin{bmatrix} v_{aa'} \\ v_{bb'} \\ v_{cc'} \end{bmatrix} &= V_{\mathrm{DC}} \begin{bmatrix} -1 & 0 & 1 \\ 1 & -1 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \gamma_{aT1} \\ \gamma_{aT2} \\ \gamma_{aT3} \end{bmatrix} + V_{\mathrm{DC}} \begin{bmatrix} 0 & 0 & 0 \\ -1 & 0 & 1 \\ 1 & -1 & 0 \end{bmatrix} \\ &\times \begin{bmatrix} \gamma_{bT1} \\ \gamma_{bT2} \\ \gamma_{bT3} \end{bmatrix} + V_{\mathrm{DC}} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 0 & 0 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} \gamma_{cT1} \\ \gamma_{cT2} \\ \gamma_{cT3} \end{bmatrix} \\ &+ V_{\mathrm{DC}} \begin{bmatrix} -1 & 1 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \gamma_{aS11} \\ \gamma_{aS12} \end{bmatrix} + V_{\mathrm{DC}} \begin{bmatrix} 0 & 0 \\ -1 & 1 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \gamma_{bS11} \\ \gamma_{bS12} \end{bmatrix} \\ &+ V_{\mathrm{DC}} \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} \gamma_{cS11} \\ \gamma_{cS12} \end{bmatrix} \end{aligned} \tag{15}$$

$$\begin{aligned} \begin{bmatrix} v_{aa'} \\ v_{bb'} \\ v_{cc'} \end{bmatrix} &= V_{\mathrm{DC}} \begin{bmatrix} -1 & 0 & 1 \\ 1 & -1 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \gamma_{aT1} \\ \gamma_{aT2} \\ \gamma_{aT3} \end{bmatrix} + V_{\mathrm{DC}} \begin{bmatrix} 0 & 0 & 0 \\ -1 & 0 & 1 \\ 1 & -1 & 0 \end{bmatrix} \\ &\times \begin{bmatrix} \gamma_{bT1} \\ \gamma_{bT2} \\ \gamma_{bT3} \end{bmatrix} + V_{\mathrm{DC}} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 0 & 0 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} \gamma_{cT1} \\ \gamma_{cT2} \\ \gamma_{cT3} \end{bmatrix} \\ &+ V_{\mathrm{DC}} \begin{bmatrix} -1 & 1 \\ 1 & -1 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \gamma_{aS11} \\ \gamma_{aS12} \end{bmatrix} + V_{\mathrm{DC}} \begin{bmatrix} 0 & 0 \\ -1 & 1 \\ 1 & -1 \end{bmatrix} \\ &\times \begin{bmatrix} \gamma_{bS11} \\ \gamma_{bS12} \end{bmatrix} + V_{\mathrm{DC}} \begin{bmatrix} 1 & -1 \\ 0 & 0 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} \gamma_{cS11} \\ \gamma_{cS12} \end{bmatrix}. \end{aligned} \tag{16}$$

The inverters' applied motor voltages can also be expressed as a vector equation (in the $\alpha\beta$ plane) using the following transformation:

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = P \begin{bmatrix} v_{aa'} \\ v_{bb'} \\ v_{cc'} \end{bmatrix} \tag{17}$$

where

$$P = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}. \tag{18}$$

Using the above transformation, the applied voltages in the $\alpha\beta$ vector variables for *T*–*S* cells and *S*–*T* cells are given by the expressions:

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = P \begin{bmatrix} v_{aa'} \\ v_{bb'} \\ v_{cc'} \end{bmatrix} \tag{19}$$

$$\begin{aligned} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} &= V_{\mathrm{DC}} \begin{bmatrix} \frac{1}{\sqrt{6}} & \frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{6}} \\ \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} & 0 \end{bmatrix} \begin{bmatrix} \gamma_{aT\alpha} \\ \gamma_{aT\beta} \end{bmatrix} \\ &+ V_{\mathrm{DC}} \begin{bmatrix} 0 & \frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{6}} \\ -\frac{2}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} \gamma_{bT\alpha} \\ \gamma_{bT\beta} \end{bmatrix} \\ &+ V_{\mathrm{DC}} \begin{bmatrix} \sqrt{\frac{3}{2}} & -\sqrt{\frac{3}{2}} & -\frac{1}{\sqrt{6}} \\ \frac{1}{\sqrt{2}} & 0 & -\frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} \gamma_{cT\alpha} \\ \gamma_{cT\beta} \end{bmatrix} \\ &+ V_{\mathrm{DC}} \begin{bmatrix} -\sqrt{\frac{2}{3}} & \sqrt{\frac{2}{3}} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \gamma_{aS\alpha} \\ \gamma_{aS\beta} \end{bmatrix} \\ &+ V_{\mathrm{DC}} \begin{bmatrix} \sqrt{\frac{1}{6}} & -\sqrt{\frac{1}{6}} \\ -\frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} \gamma_{bT\alpha} \\ \gamma_{bT\beta} \end{bmatrix} \\ &+ V_{\mathrm{DC}} \begin{bmatrix} \sqrt{\frac{1}{6}} & -\sqrt{\frac{1}{6}} \\ \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} \gamma_{cS\alpha} \\ \gamma_{cS\beta} \end{bmatrix} \end{aligned} \tag{20}$$

$$\begin{aligned} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} &= V_{\mathrm{DC}} \begin{bmatrix} \frac{1}{\sqrt{6}} & \frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{6}} \\ \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} & 0 \end{bmatrix} \begin{bmatrix} \gamma_{aT\alpha} \\ \gamma_{aT\beta} \end{bmatrix} \\ &+ V_{\mathrm{DC}} \begin{bmatrix} 0 & \frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{6}} \\ -\frac{2}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} \gamma_{bT\alpha} \\ \gamma_{bT\beta} \end{bmatrix} \\ &+ V_{\mathrm{DC}} \begin{bmatrix} \sqrt{\frac{3}{2}} & -\sqrt{\frac{3}{2}} & -\frac{1}{\sqrt{6}} \\ \frac{1}{\sqrt{2}} & 0 & -\frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} \gamma_{cT\alpha} \\ \gamma_{cT\beta} \end{bmatrix} \\ &+ V_{\mathrm{DC}} \begin{bmatrix} -\sqrt{\frac{3}{2}} & \sqrt{\frac{3}{2}} \\ \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} \gamma_{aS\alpha} \\ \gamma_{aS\beta} \end{bmatrix} \\ &+ V_{\mathrm{DC}} \begin{bmatrix} \sqrt{\frac{3}{2}} & -\sqrt{\frac{3}{2}} \\ -\frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} \gamma_{bT\alpha} \\ \gamma_{bT\beta} \end{bmatrix} \\ &+ V_{\mathrm{DC}} \begin{bmatrix} 0 & 0 \\ \sqrt{2} & -\sqrt{2} \end{bmatrix} \begin{bmatrix} \gamma_{cS\alpha} \\ \gamma_{cS\beta} \end{bmatrix}. \end{aligned} \tag{21}$$

After analyzing these two last equations and taking into account all of the switching combinations, it is possible to conclude that there are 187 different voltage vectors for the *T*–*S* configuration and 197 different voltage vectors for the S–T configuration. Taking the number of voltage vectors into account, the second configuration is advantageous.

From the analysis of these equations and the obtained voltage vectors, modulation methods, such as space vector modulation and discontinuous pulsewidth modulation [39],

[40], can be developed and implemented for the proposed topologies. However, industry proven traditional techniques, such as the *SPWM,* can also be adapted for these inverter topologies, as will be shown in the next section.

B. POWER LOSS AND EFFICIENCY THEORETICAL ANALYSIS

Power losses in converters are mainly due to the nonideality of the power semiconductors devices (PSDs). Parasitic resistors and saturation voltages together with the PSD switching process generate conduction and switching power losses, lowering the system's efficiency. The presence of parasitic resistors and voltage drops in PSDs has significant impact. In PSDs, such as the insulated gate bipolar transistor (IGBT), the saturation voltage drop (v_{CEsat}) must be considered, being the ON-state collector–emitter voltage (v_{CE}) given as

$$v_{CE} = v_{\text{CEsat}} + R_C i_C \tag{22}$$

where R_C the collector–emitter ON-state resistance and i_C the collector current.

A similar approximation can be used for power diodes. Taking this into account, the conduction losses of IGBTs and diodes can be estimated as:

$$P_{\text{cond\_IGBT}} = v_{\text{CEsat}}\, i_{C\_av} + R_C\, i^2_{C\_\text{rms}} \tag{23}$$

$$P_{\text{cond\_diode}} = v_{F0}\, i_{D\_av} + R_F\, i^2_{D\_\text{rms}} \tag{24}$$

where v_{F0} is the diode ON-state zero-current forward voltage drop, R_F is the diode ON-state resistance, and $i_{D\text{-}av}$ and $i_{D\text{-rms}}$ are the diode current average and root-mean-square (rms) values, respectively.

The conduction power losses of metal oxide semiconductor field effect transistors (MOSFETs) can be estimated as

$$P_{\text{cond\_MOSFET}} = R_{\text{DS}}\, i^2_{D\_\text{rms}} \tag{25}$$

where R_{DS} is the drain–source ON-state resistance and i_D is the drain current of the MOSFET.

Regarding the switching loss, it is associated with the turn-ON or turn-OFF delay of the power semiconductor. In accordance with this, these losses can be determined by

$$P_{\text{switching}} = P_{\text{switching\_ON}} + P_{\text{switching\_OFF}} \tag{26}$$

where

$$P_{\text{switching\_ON}} = f_S \int_0^{t_{ON}} v_{\text{CE}}\, i_C\, dt = \\ = f_S \int_0^{t_{\text{ON}}} \frac{V_{\text{CE}}}{t_{\text{ON}}} t \left(-\frac{I_C}{t_{\text{ON}}}(t - t_{\text{ON}})\right) dt = \tfrac{1}{6} f_S V_{\text{CE}} I_C t_{\text{ON}} \tag{27}$$

$$P_{\text{switching\_OFF}} = f_S \int_0^{t_{\text{OFF}}} v_{\text{CE}}\, i_C\, dt = \\ = f_S \int_0^{t_{\text{OFF}}} \frac{V'_{\text{CE}}}{t_{\text{OFF}}} t \left(-\frac{I'_C}{t_{\text{OFF}}}(t - t_{\text{OFF}})\right) dt = \tfrac{1}{6} f_S V'_{\text{CE}} I'_C t_{\text{OFF}} \tag{28}$$

being f_S is the switching frequency, V_{CE} and V'_{CE} are the ON-state voltage and OFF-state voltage, and I_C and I'_C are the ON-state current and OFF-state current.

The efficiency of the proposed topologies can be estimated by determining the power losses of the converters PSDs.

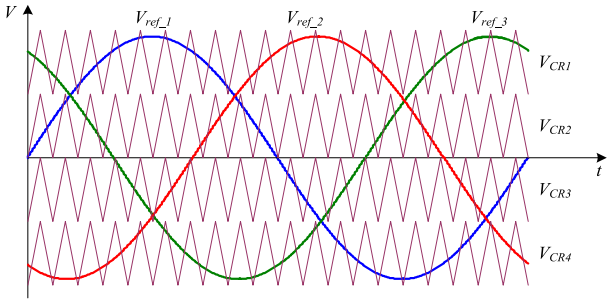

FIGURE 4. PD-SPWM applied to proposed multilevel inverter with two bridges per leg.

IV. IMPLEMENTATION OF THE MODULATORS

A. TRADITIONAL SPWM TECHNIQUES

One of the characteristics of the proposed *T–S* cells and *S–T* cells multilevel inverter topologies for the open-end induction motor is that the traditional *SPWM* techniques can be adapted for these inverter topologies. This can be achieved by the application of the phase disposition sinusoidal *PWM* method (*PD-SPWM*) to the proposed inverter topologies. To analyze the implementation of *PD-SPWM*, both the *T–S* cells and *S–T* cells of multilevel inverter topology with two bridges per leg (one *T* cell and one *S* cell) will be considered. The *PD-SPWM* modulation concept is presented in Fig. 4. Four triangular carrier waveforms are used to generate seven or nine voltage levels.

It should be noted that the modulation strategy can be applied in both *T–S* cells and *S–T* cells inverters. Indeed, although the voltage levels are different, the number of bridges and semiconductors are exactly the same. Therefore, no change is required in the modulation strategy of the *T–S* cells and *S–T* cells inverter variants.

The detailed operation of the circuit taking into consideration this proposed modulator technique can be seen through the analysis of the generation of the transistors gating signals associated with the stator winding of phase *A*. Thus, in this case, it is considered the reference signal $V_{\text{ref\_1}}$ and the four carrier signals. The result of these comparisons will give those transistor gating signals. So, for the *T–S* topology, those signals will be generated by the circuit presented in Fig. 5. Regarding the *S–T* topology, the circuit that will generate the transistors gating signals can be seen in Fig. 6.

Several other *SPWM* techniques used in multilevel inverters, such as the phase opposition disposition *PWM* (*PODPWM*), alternative *PODPWM*, and phase shift *PWM* (*PSPWM*), can also be adapted for the proposed topologies. This can be verified through the application of the *PSPWM* technique to the proposed topologies. For this implementation, it is considered again both the *T–S* cells and *S–T* cells of multilevel inverter topology with two bridges per leg (one *T* cell and one *S* cell). In this implementation, carrier signals with sinusoidal references are considered, as shown in Fig. 7. In this case, only two triangular carrier waveforms are used, but six sinusoidal references are needed (three of which are in

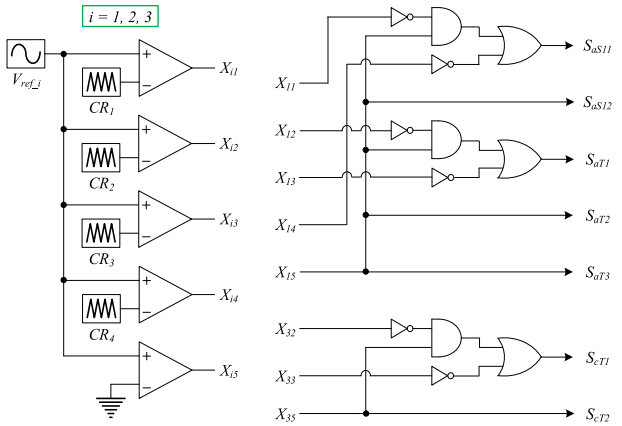

FIGURE 5. Circuit for the generation of the transistor gating signals for the T–S proposed topology for the PD-SPWM implementation.

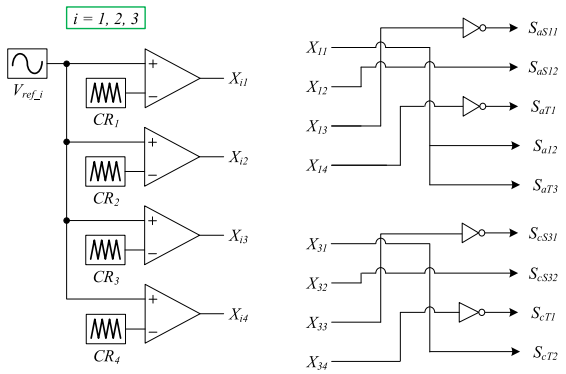

FIGURE 6. Circuit for the generation of the transistor gating signals for the S–T proposed topology for the PD-SPWM implementation.

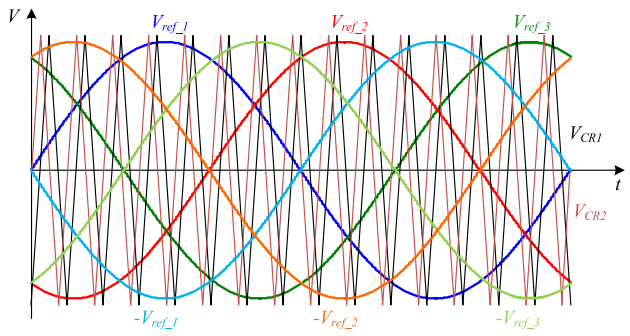

FIGURE 7. PS-SPWM applied to proposed multilevel inverter with two bridges per leg.

phase opposition). Again, this modulator can produce seven or nine voltage levels.

The circuits that allow the switch signals to be generated can be seen in Figs. 8 and 9, where the first is associated with *T–S* cells and the second with *S–T* cells. These are only related to the phase *A* stator winding.

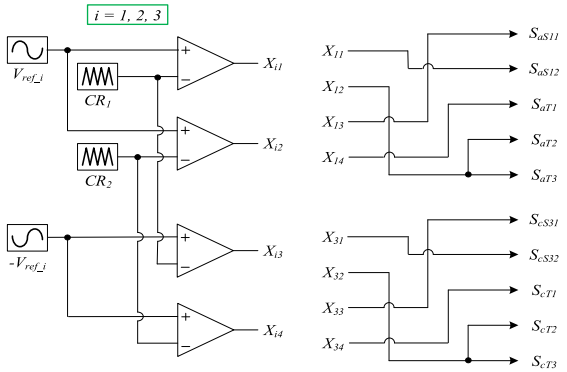

FIGURE 8. Circuit for the generation of the transistor gating signals for the T–S proposed topology for the PS-SPWM implementation.

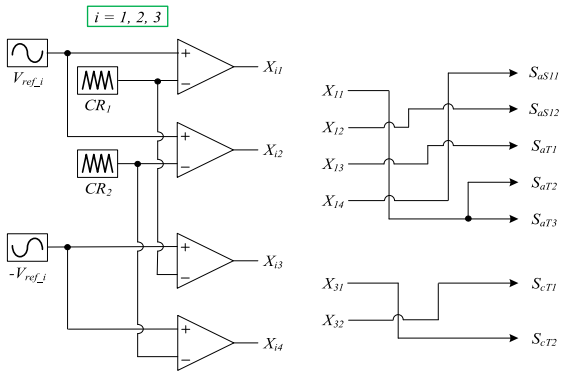

FIGURE 9. Circuit for the generation of the transistor gating signals for the S–T proposed topology for the PD-SPWM implementation.

B. OPERATION OF THE CONVERTERS UNDER A POWER SEMICONDUCTOR FAILURE

One of the most interesting features of a multilevel converter is its fault-tolerant capability in the event of a power semiconductor open failure. This critical feature is also present in the proposed topologies. In fact, they can operate in a fault-tolerant mode without the addition of additional hardware. This is possible while retaining the modulation strategy.

When a power semiconductor fails (open-state), the NVL available to the motor winding associated with that semiconductor is reduced by one. To keep the drive running, the healthy controlled power semiconductor of the leg where the open-switch fault occurs should be turned ON during all the time. However, because the NVL applied to the motor will only affect the winding associated with the faulty power semiconductor, voltage imbalances may occur. As a result when the drive is nearing its nominal power (requiring all voltage levels), this issue must be considered. One strategy that can be used with minimum effect in the required modulation changes is to permanently turn OFF the power semiconductors in the same position as the one under the open fault.

Let us consider a fault in the power semiconductor S_{aS12} as an example of the above strategy. The other power semiconductor of the correspondent leg ($\bar{S}_{aS12}$) will be permanently

TABLE 1. Comparison of the Characteristics Between the Proposed and Other Multilevel Inverters for Open-End Winding Motor Drive

Topology	[34]	[35]	[36]	[37]	T-S cells	S-T cells
Number of voltage levels for the basic configuration	9	6	7	5	5	7
Number of switches	36	24	48	36	30	30
DC voltage sources	2	3	6	4	6	6
DC voltage Sources with the same voltage level	no	no	no	yes	yes	yes
Requiring floating capacitors	yes	no	no	no	no	no
TSV_{pu}	12	10.5	14	15	10	7.5
Maximum Blocking voltage (pu)	8/14	2/3	1	1/2	1/2	1/3
Control complexity	high	high	medium	medium	low	Low
Easily extended to higher voltage levels	no	no	no	no	yes	yes

turned ON in this faulty situation. Furthermore, the power semiconductors in the same position as the one under fault (S_{bS12} and S_{cS12}) will be turned OFF permanently. The other power semiconductors in the correspondent leg ($\bar{S}_{bS12}$ and $\bar{S}_{cS12}$) will be turned ON permanently.

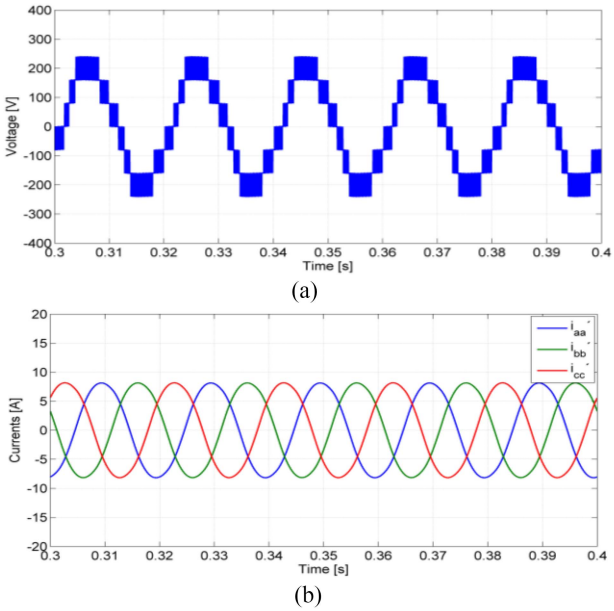

FIGURE 10. Obtained simulation waveforms for the T–S cells topology and PD-SPWM technique: (a) winding voltage *aa′* and (b) winding currents.

V. COMPARISON ANALYSIS

With the purpose to compare the proposed topologies with other ones that have been presented for the open-end winding motor drive, in Table 1, is presented a comparison of their characteristics. From Table 1, it is possible to see that the proposed topologies are the ones that require more *dc* voltage sources. However, they do not require floating capacitors. On the other hand, they are among the ones that require less number of power semiconductor switches. It also allows using *dc* voltage sources with the same voltage level. However, they can also use *dc* voltage sources with different voltage levels, allowing in that case to extend the NVL. Another important aspect, is that, in the case of the proposed *S–T* cells, is the one that requires switches with lower maximum blocking voltage considering the maximum voltage level that appears at the motor windings. A comparison of the voltage stress of power semiconductors is also presented, taking into account not just one, but all of the semiconductors in the converter. The total standing voltage (*TSV*) was used for this comparison [41], [42]. In *per units* (p.u.), the $TSV_{p.u.}$ is the sum of the peak hold-off voltages of all power semiconductors divided by the output voltage amplitude. In terms of $TSV_{p.u.}$, it is possible to see that the proposed *S–T* cells have the lowest *TSV* value. Another feature of the proposed *T–S* cells and *S–T* cells inverters is that their control complexity is low due to the ease with which multilevel *SPWM* techniques can be adapted. Finally, the proposed topologies can be easily extended to higher voltage levels by simply introducing new single-phase two-level H-bridge inverters in a cascaded connection.

Other specificity associated with the proposed topologies is that the control complexity is low, since multilevel *SPWM* techniques can easily be adapted. Finally, the proposed topologies can also be easily extended to higher voltage levels, since simply what is need is to introduce new single-phase two-level H-bridge inverters in a cascaded connection.

This analysis revealed that the proposed solutions are competitive, particularly the topology with *S–T* cells, which is an interesting alternative to the others already presented.

VI. SIMULATION RESULTS

The verification and confirmation of the theoretical assumptions were first made through several simulation tests. These tests were carried out using the *MATLAB/Simulink* platform. The simulations considered one set of cells S, with *dc* source voltages equal to 80 V. It was also used the *SPWM* methods with triangular carriers with 4 kHz.

The first tests of the drive were made with the *PD-SPWM* method. Initially, a 50-Hz reference frequency and modulation index of 0.9 equal for both *T–S* cells and *S–T* cells topologies were used. The output *ac* voltage and current waveforms of each of the proposed topologies are presented in Figs. 10–13. Figs. 10 and 11 present the applied voltage waveform of one of the motor windings, as well as the motor three-phase currents for the topology with the three-phase inverters connected in wye. The voltage waveform in Fig. 10(a) shows the seven voltage levels applied to the motor windings. On the other hand, Fig. 10(b) shows that the motor currents are very close to the desired sinusoidal waveform shape. However, Fig. 10(a) also shows that the voltage waveform has some asymmetry (bilateral). It is apparent that the *PD-SPWM* modulator in this topology presents some limitations when the maximum number of levels is used.

To verify the quality of the waveforms, it was measured the *total harmonic distortion* (*THD*) of the motor voltages

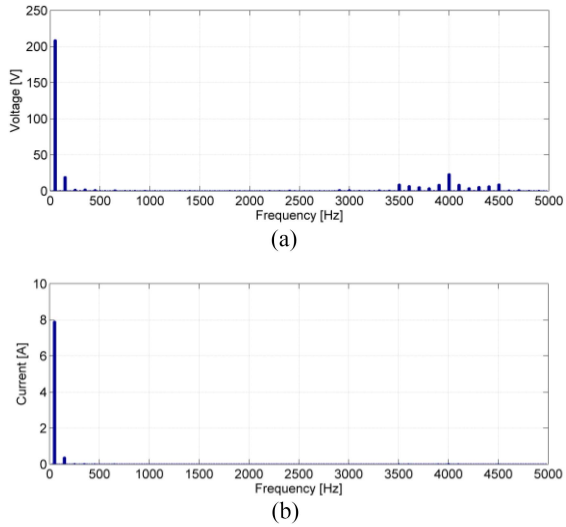

FIGURE 11. FFT of the obtained simulation waveforms for the T–S cells topology and PD-SPWM technique: (a) winding voltage *aa′* and (b) winding currents.

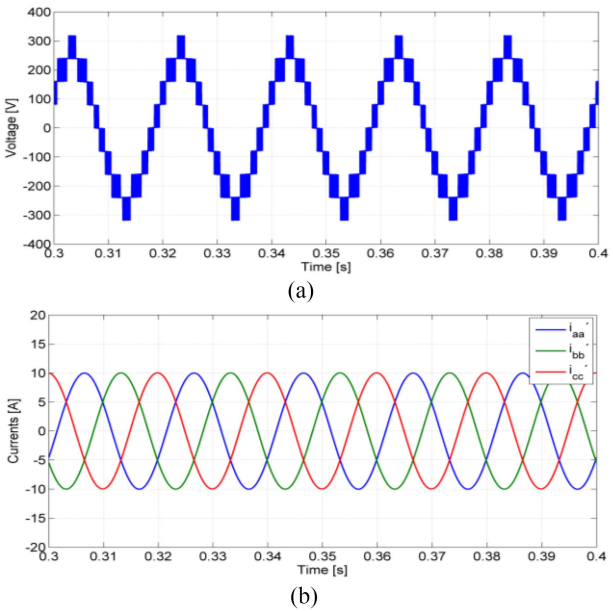

FIGURE 12. Obtained simulation waveforms for the S–T cells topology and PD-SPWM technique: (a) winding voltage *aa′* and (b) winding currents.

and currents. The *THD* of the load voltages and currents was measured to verify the quality of the waveforms. This measurement yielded a voltage *q* of 24.97% and a current *THD* of 3.67% well within the acceptable limits of most harmonic distortion standards. The fast Fourier transform (FFT) of these waveforms can be seen in Fig. 11. One of the aspects that can be seen is the presence of a small but noticeable third harmonic. This third harmonic is due to the fact that the generated voltage waveform is not perfectly symmetrical. This low-frequency harmonic is the main component in the *THD* of the inductive load current. High-frequency harmonics with

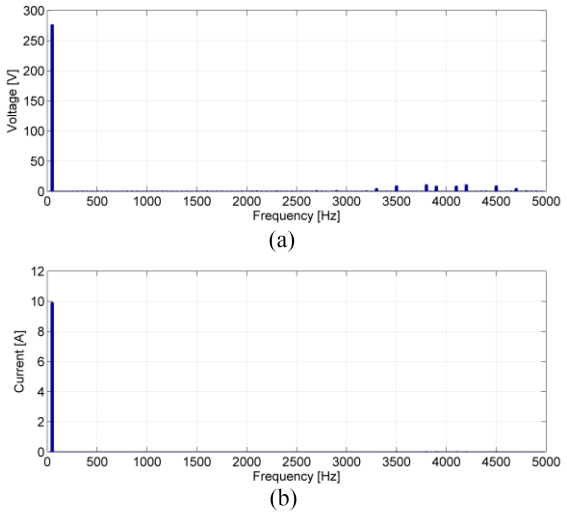

FIGURE 13. FFT of the obtained simulation waveforms for the S–T cells topology and PD-SPWM technique: (a) winding voltage *aa′* and (b) winding currents.

similar amplitude around the frequency of the carriers (4 kHz) can also be seen, as expected with negligible effect on the current. Higher frequency harmonics centered on the carriers' frequency double, triple, are residual and not represented.

The corresponding waveforms for the *S–T* topology can be seen in Fig. 12. From Fig. 12(a), it is confirmed that the NVL applied to the motor windings has increased from seven to nine. Besides that, the peak voltage applied to the motor windings has also increased from nearly 240 to 320 V. This suggests that, for the same *dc* voltage, the *S–T* cells topology is able to increase the output power, or reduce the *dc* voltage sources rating decreasing the blocking voltage of the switches, for the same output power. In terms of waveform distortion, this topology yielded a voltage *THD* of 17.41% and a current *THD* of 0.31%. It is possible to see that the waveform distortions have been reduced. This was expected because the voltage levels have increased with this topology. Furthermore, with this converter assembly, the problem of the third harmonic is eliminated, as shown in Fig. 13, which shows the FFT of the voltage and current waveforms. There are some harmonics with noticeable amplitude, but they are centered on the carrier frequency (4 kHz) and on the double, triple, and so on, of this frequency.

The efficiency of the T–S and S–T topologies for the presented test conditions was also determined. The efficiency for the T–S cells topology was 95.2%, whereas the efficiency for the S–T cells topology was 94.3%. However, the S–T cells topology efficiency was not measured at the same output power because the S–T cells topology allows for higher voltages to be applied from the same dc voltage source values. To achieve a fair comparison, the efficiencies must be measured for the condition in which the T–S cells topology has the same output currents amplitude as the S–T cells topology. Taking this new condition into account, the efficiency of the T–S cells

TABLE 2. Comparison of the Power Losses for the Two Proposed Topologies and PD-SPWM Technique (Simulation Tests)

Topology	IGBT's losses	Diode losses	Total losses
S-T cells	4.5%	0.4%	4.9 %
T-S cells	5.3%	0.4%	5.7 %

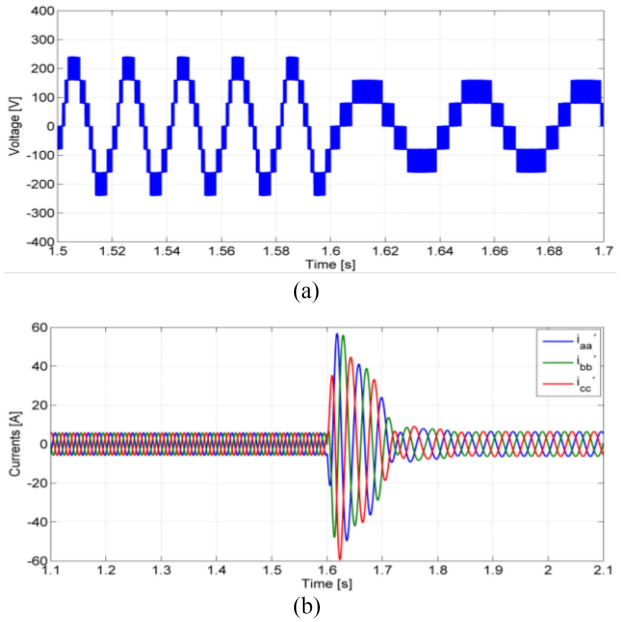

FIGURE 14. Obtained simulation waveforms for the for the T–S cells topology and PD-SPWM technique subjected to a reference frequency and modulation index step changes with open-loop control: (a) winding voltage *aa′* and (b) winding currents.

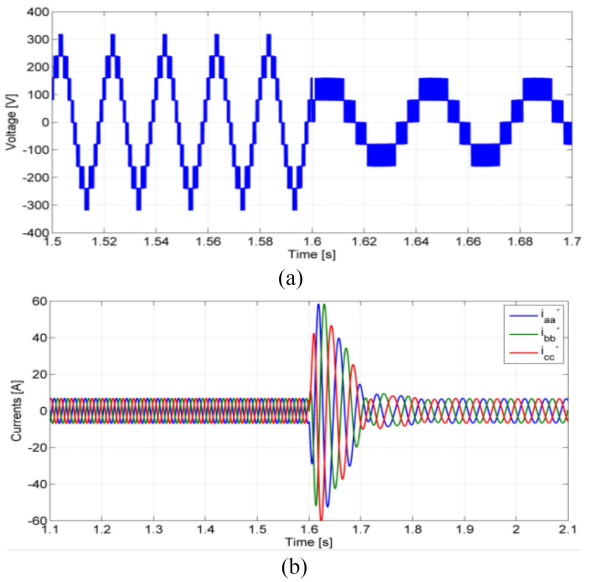

FIGURE 15. Obtained simulation waveforms for the S–T cells topology and PD-SPWM technique subjected to a reference frequency and modulation index step changes with open-loop control: (a) WINDING voltage *aa′* and (b) winding currents.

topology was 95.1%. This confirms that the T–S cell topology is more efficient. This was expected given the lower number of power semiconductors in the load current's path. The power losses are distributed among the IGBTs and diodes. However, as given in Table 2, the IGBT losses have higher impact.

To compare the efficiency of the proposed topology over existing topologies, a conventional cascaded H-bridge inverter operating in equivalent conditions was considered as the standard. In this case, a converter with two cascaded single-phase H-bridges per leg was considered. The cascaded converter is fed from two 160-V dc voltage sources to deliver the same maximum voltage at the machine windings. Operating in these conditions, the cascaded H-bridge inverter presents an efficiency of 95.1%. This result shows that the efficiencies of the proposed topologies, ranging from 94% to over 95%, are in the range of the conventional cascaded topology.

A transient test was performed, in which suddenly the reference frequency is changed from 50 to 25 Hz and the modulation index was changed from 0.9 to 0.45. The resulting voltage and current waveforms for *T–S* cells and *S–T* cells topologies are presented in Figs. 14 and 15, respectively. Both figures show the change of the frequency of those waveforms in accordance with the reference, as well as the reduction of the voltage levels when the modulation index is reduced. The number of levels of the voltage applied to the motor winding is always equal or higher in the *T–S* cells topology. The voltage waveforms in Figs. 14 and 15 show that after the modulation index reduction to 0.45 (leading to a reduction in the NVL used), the *PD-SPWM* voltage asymmetry is mostly eliminated when compared with the results for high modulation indexes in the *T–S* cells topology [see Fig. 10(a)]. An important overcurrent appears after the reference frequency changes (see Fig. 15). This is due to the load being an induction motor. In fact, the angular speed of the rotating field decreases almost immediately while the rotor is at higher speed due to inertial load conditions. Because the rotor speed exceeds the rotating field, the rotor and stator currents increase and reverse direction to produce braking torque until the rotor speed stabilizes in a new operation condition. This overcurrent happens as the test is done in open loop, without current or torque control, just to illustrate the capability of the topology to simultaneous step-change the reference frequency and the modulation index. The results show that there is no response limitation in the proposed topology regarding the step-changes. Using closed-loop control, the current overshoot can be strongly limited. To illustrate this, a simulation is presented in which a closed-loop V/f controller was used. The simulation considers a step-change in the motor speed reference from 1500 to 750 r/min (as considered in open loop). The results of this simulation for the *S–T* cells topology are seen in Fig. 16, showing a strongly reduced current overshoot.

Tests with alternative *SPWM* techniques applied to the proposed multilevel topologies were also made. The alternative considered in this case is the *PS-SPWM*, as described in Section IV. Thus, identical tests were performed as with the

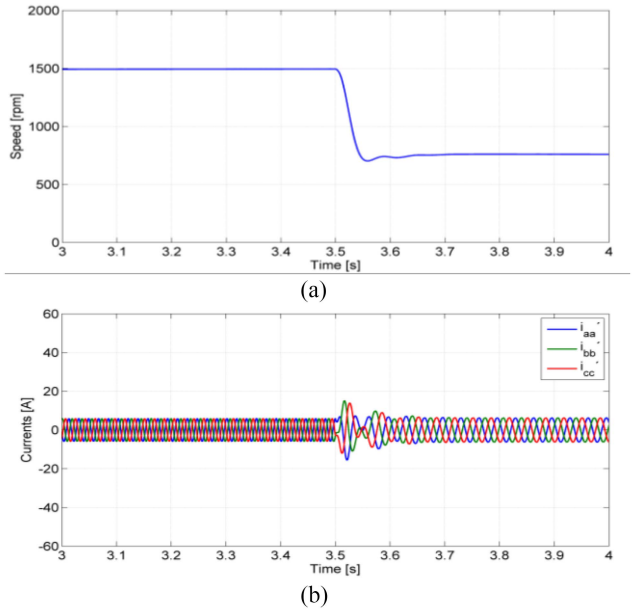

FIGURE 16. Obtained simulation waveforms for the S–T cells topology and PD-SPWM technique subjected to a reference frequency and modulation index step changes with a closed-loop V/f controller: (a) motor speed and (b) winding currents.

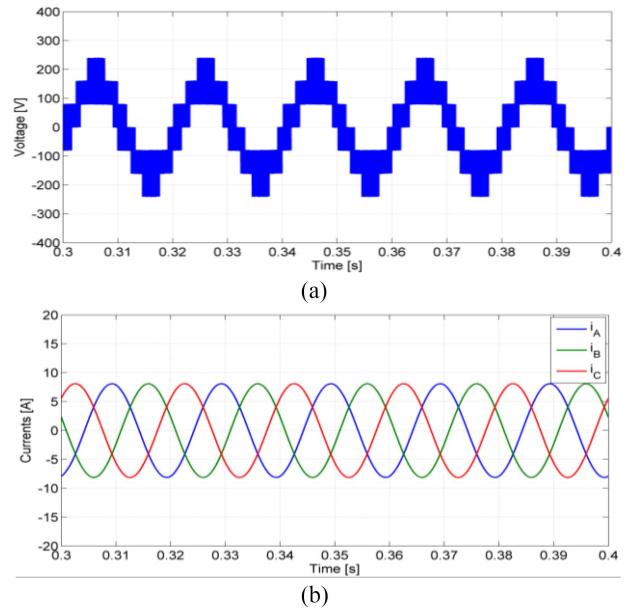

FIGURE 17. Obtained simulation waveforms for the T–S cells topology and PS-SPWM technique: (a) winding voltage *aa′* and (b) winding currents.

previous *SPWM* technique, namely, using references with a frequency of 50 Hz and a modulation index of 0.9 for both *T–S* and *S–T* cell topologies. Fig. 17 depicts the obtained results of the output *ac* voltage and current waveforms for the *T–S* cells topology. The applied voltage waveform of one of the motor windings is shown in Fig. 17(a), and the motor three-phase currents are shown in Fig. 17(b). These diagrams also show seven voltage levels applied to the motor windings

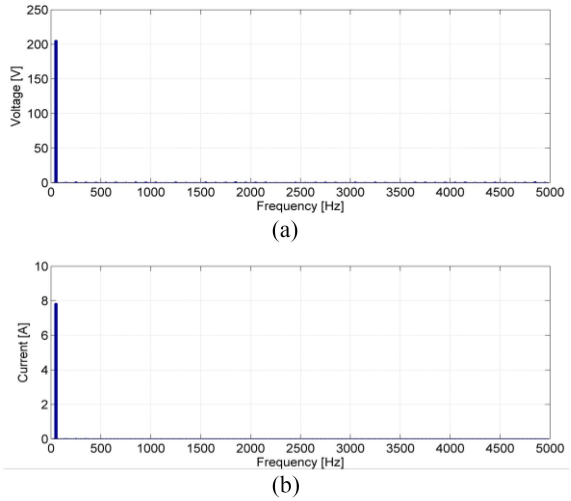

FIGURE 18. FFT of the obtained simulation waveforms for the T–S cells topology and PS-SPWM technique: (a) winding voltage *aa′* and (b) winding currents.

and nearly sinusoidal currents. *THD* voltage was 32.71% and *THD* current was 0.45% for the *PS-SPWM* technique. The voltage *TDH* in this case is higher than that obtained with *PD-SPWM* technique.

Analyzing the FFT of this waveform, the amplitude of the harmonics is nearly zero up to frequencies around 5 kHz. Despite the fact that the carriers frequency is the same (4 kHz) as in the *PD-SPWM* technique, harmonics with noticeable amplitude appear at a much higher frequency. In this case, harmonics with perceivable amplitude appear around the double of the carrier frequency, the quadruple, and so on. In contrast to the load voltage *THD*, the current *THD* is significantly lower. This is because the third harmonic is highly attenuated using this technique, as shown in Fig. 18. The high-frequency harmonics will be also strongly attenuated because the motor acts as a low-pass filter.

The corresponding waveforms for the *S–T* topology are depicted in Fig. 19 for *PS-SPWM*. Fig. 19(a) depicts the increase in voltage levels, whereas Fig. 19(b) depicts the motor currents. Again, the peak voltage applied to the motor windings has increased, this time from nearly 240–320 V. This confirms that with the *S–T* topology, for the same *dc* voltage, it is possible to increase the output power or to decrease the *dc* voltage source rating and therefore lowering the required blocking voltage of switches for the same output power.

With *PS-SPWM*, the waveform distortion decreased, as a voltage *THD* of 27.04% and a current *THD* of 0.39% were obtained. The FFT of these waveforms also revealed that the third harmonic is practically nonexistent, as shown in Fig. 20. The first harmonics with significant amplitude appear only around the quadruple of the carrier frequency.

The efficiency of these two topologies with the *PS-SPWM* technique was also determined. The values obtained for the *T–S* cells topology and the *S–T* cells topology were 95.9%

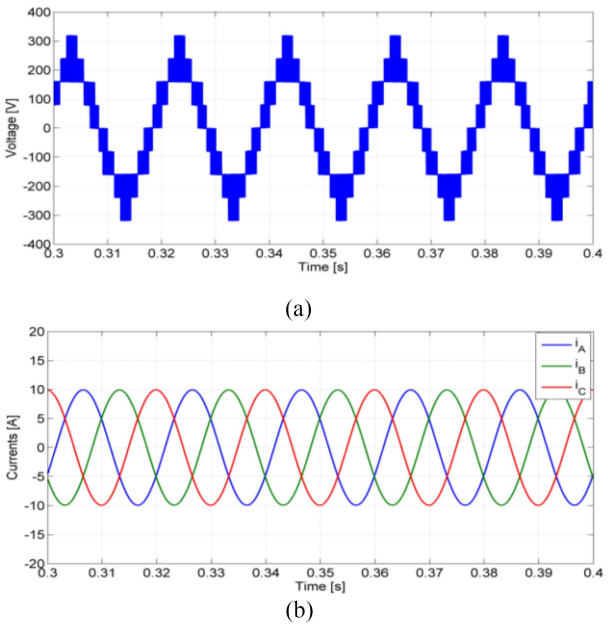

FIGURE 19. Obtained simulation waveforms for the S–T cells topology and PS-SPWM technique: (a) winding voltage *aa′* and (b) winding currents.

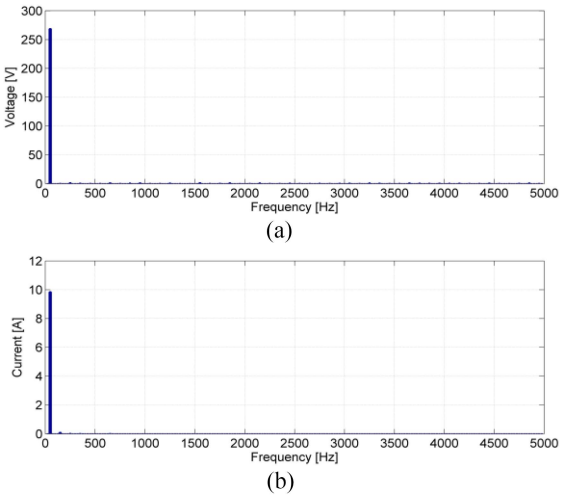

FIGURE 20. FFT of the obtained simulation waveforms for the S–T cells topology and PD-SPWM technique: (a) winding voltage *aa′* and (b) winding currents.

TABLE 3. Comparison of the Power Losses for the Two Proposed Topologies and PS-SPWM Technique (Simulation Tests)

Topology	IGBT's losses	Diode losses	Total losses
S-T cells	3.7%	0.4%	4.1 %
T-S cells	4.9%	0.8%	5.7 %

and 94.3%, respectively. Table 3 shows that the IGBTs have higher impact on power losses, as expected.

VII. EXPERIMENTAL RESULTS

The proposed multilevel power converter topologies theoretical assumptions and simulation results were confirmed using a laboratory prototype. This prototype allows to provide an output power of 2.5 kW. The controller used to implement the described SPWM modulators was Digital Signal Processor DSPACE DS1103 Controller Board. The frequency of the carriers is 4 kHz. Several experimental tests were carried out with *dc* voltage sources at 80 V and open-end windings induction motor as load with a nominal power of 2.2 kW, 220/380 V (Δ/Y), 50 Hz, and 1430 r/min. Fig. 21 depicts a photograph of the experimental setup displaying the main devices used.

Initially the drive was tested for the reference frequency of 50 Hz and the same modulation index of 0.9 for both *T–S* cells and *S–T* cells topologies. The resulting voltage and current waveforms for the *T–S* cells topology are presented in Fig. 22. Fig. 22(a) presents the applied voltage waveform in one of the motor windings, whereas Fig. 22(b) presents the motor

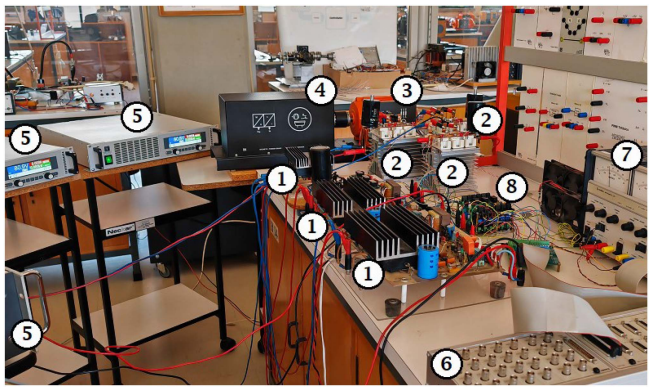

FIGURE 21. Experimental setup. (1) Three single-phase two-level H-bridge inverters. (2) Three three-phase two-level H-bridge inverters. (3) Induction motor. (4) Electromagnetic brake. (5) Six regulated dc power sources. (6) Digital Signal Processor DSPACE DS1103 Controller Board. (7) Auxiliary dc power source for gate drive circuits. (8) Gate drive circuits.

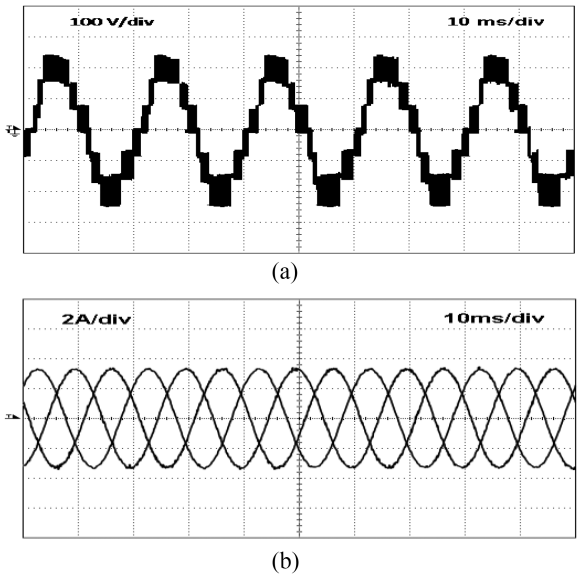

FIGURE 22. Obtained experimental waveforms for the T–S cells topology and PD-SPWM technique: (a) winding voltage *aa′* and (b) winding currents.

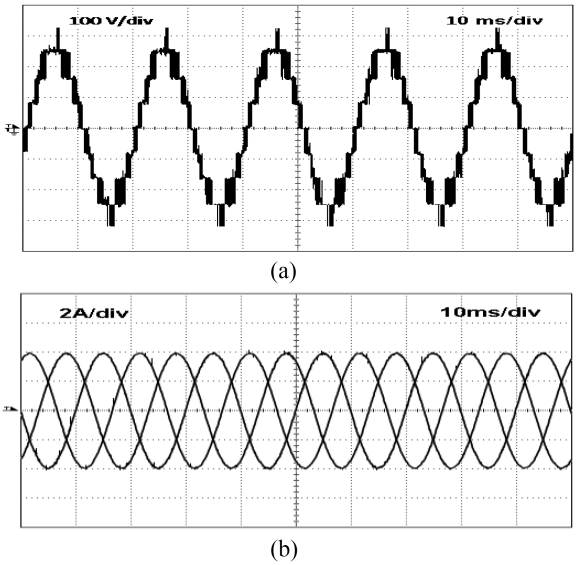

FIGURE 23. Obtained experimental waveforms for the S–T cells topology and PD-SPWM technique: (a) winding voltage *aa′* and (b) winding currents.

three-phase currents. The voltage waveform [see Fig. 22(a)] confirms that seven voltage levels are applied to the motor windings. Fig. 22(b) shows that the motor currents are nearly sinusoidal shaped. The *THD* of the motor voltages and currents were measured to be 27.1% and 4.8%, respectively. The experimental current *THD* is slightly higher than the simulation result (3.67%). This is due to experimental imperfections that increase the third harmonic amplitude characteristic of the *T–S* topology and *PD-SPWM* technique, as shown in Fig. 11. Tests with the same conditions, but now for the *S–T* cells topology, were also done. As a result of this, similar waveforms for this cells topology can now be seen in Fig. 23. The voltage waveform [Fig. 23(a) confirms that the NVL applied to the motor windings are increased from seven to nine]. It is also possible to verify that the peak voltage applied to the motor windings also increased. This confirms that the *S–T* cells topology can increase the output power, for a given *dc* source voltage, or can reduce the blocking voltage of the switches required for a given output power. Another advantage of this topology is that it allows for higher waveform quality. In fact, the voltage and current *THD* obtained are 19.12% and 0.39%, respectively.

The efficiency of these two topologies was also measured under the same power conditions. The efficiency obtained for the T–S cell topology was 94.1%, whereas the efficiency obtained for the S–T cell topology was 93.1%. As with the simulation tests, the efficiencies were also measured using the same amplitude in the output currents. According to this test, for the T–S cell topology, an efficiency of 93.9% was now obtained. Although the efficiency was increased, it still has a lower value than the T–S cells topology. This is expected given there are fewer power semiconductors in the path of the load current. As demonstrated by the simulation studies and the power losses given in Table 3, it is possible to confirm the higher impact of the IGBTs losses (see Table 4). Regarding the comparison with the conventional cascaded H-bridge inverter, a laboratory test of this classical converter operating in equivalent conditions was also done. Thus, the obtained efficiency of the classical cascaded H-bridge inverter was 94.1%, confirming that this is the range of the proposed topologies.

TABLE 4. Comparison of the Power Losses for the Two Proposed Topologies and PD-SPWM Technique (Experimental Tests)

Topology	IGBT's losses	Diode losses	Total losses
S-T cells	5.5%	0.6%	6.1 %
T-S cells	6.2%	0.7%	6.9 %

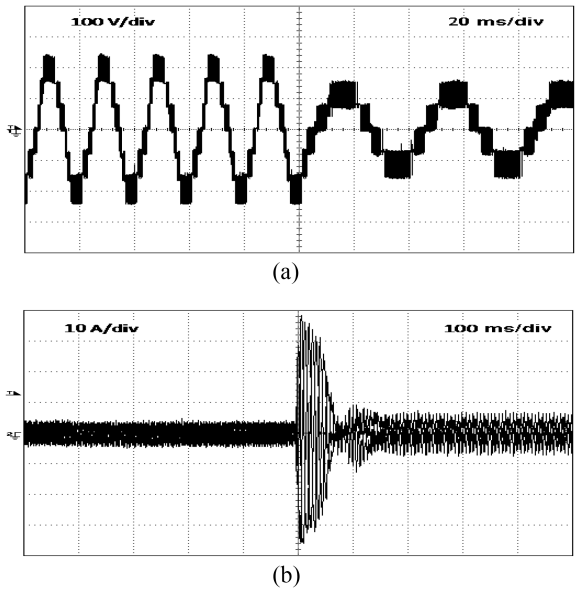

FIGURE 24. Obtained experimental waveforms for the T–S cells topology and PD-SPWM technique with reference frequency and amplitude step changes: (a) winding voltage *aa′* and (b) winding currents.

Similarly, to the simulations, transient tests were carried out, with the fundamental frequency being reduced from 50 to 25 Hz and the modulation index reduced from 0.9 to 0.45. The resulting voltage and current waveforms for the *T–S* cells topology are presented in Fig. 24. The change of the frequency is clearly seen in Fig. 24(a), also showing the reduction of the voltage levels due to the reduction of the modulation index to 0.45. The corresponding motor currents can be seen in Fig. 24(b) showing that after the frequency reference change there is a transient in these currents. During the transient, there is an important overshoot. However, as mentioned before, this large overshoot is due to the fact that there are step changes in reference frequency and modulation index. As the load is an induction motor, the step changes originate an almost immediate decrease in the angular speed of the rotating field, while the rotor is at higher speeds due to inertial load conditions. Because the rotor speed exceeds the rotating field speed, the rotor and stator currents increase and reverse direction to produce braking torque until the rotor

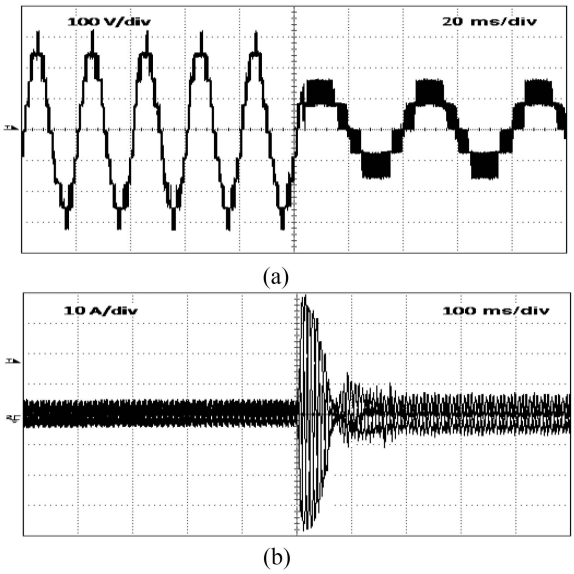

FIGURE 25. Obtained experimental waveforms for the S–T cells topology and PD-SPWM technique with reference frequency and amplitude step changes: (a) winding voltage *aa′* and (b) winding currents.

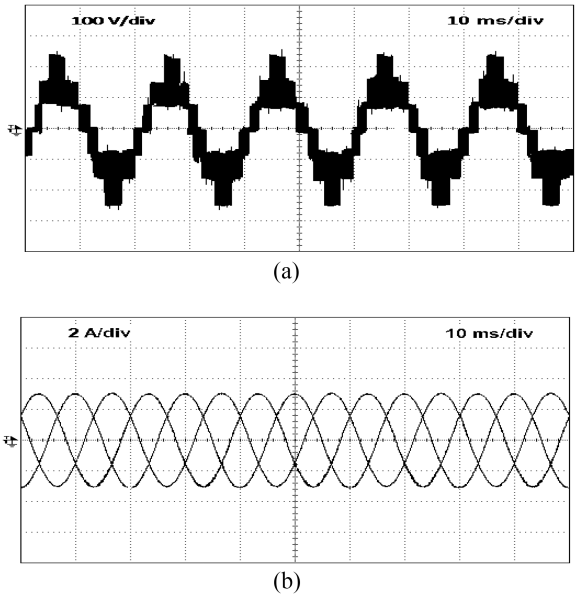

FIGURE 26. Obtained experimental waveforms for the T–S cells topology and PS-SPWM technique: (a) winding voltage *aa′* and (b) winding currents.

speed stabilizes in a new operating condition. This open-loop experiment was done without current or torque control to illustrate the proposed topology capability to simultaneously step change the reference frequency and the modulation index. The results show that the proposed converter is very fast in applying the step-changes to the motor. This overshoot can be limited using a closed-loop control, as shown in the simulation results. Fig. 25 shows similar transient results from the *S–T* cells topology. It can be seen that the number of levels of the voltage applied to the motor winding is higher at the rated voltage for the *S–T* cells topology [see Fig. 25(a)], regarding the *T–S* cells topology [see Fig. 24(a)].

The developed laboratory prototype was also driven using the *PS-SPWM* alternative *SPWM* technique. The test conditions were identical to those that were shown in the simulation tests. Fig. 26 shows the load *ac* voltage and current waveforms for the *T–S* cells topology. It is possible to identify the seven voltage levels that are distinctive of this topology, resulting in a voltage *THD* of 43.5%, which is higher regarding the *PD-SPWM* technique. The currents exhibit a nearly sinusoidal shape with a *THD* value of 0.58%, an important reduction due to the fact that the *PS-SPWM* third harmonic is almost nonexistent.

Fig. 27 shows the corresponding waveforms for the *S–T* topology when using the *PS-SPWM*. It is again possible to confirm the increase in the NVL. The peak voltage applied to the motor has increased, which is may be advantageous. Regarding the waveform quality, the *S–T* topology with *PS-SPWM* outperforms the *S–T* topology with *PS-SPWM* because a voltage *THD* of 31.5% and a current *THD* of 0.47% were obtained. However, it is obvious that the *PS-SPWM* technique yields worse results when compared with *PD-SPWM*.

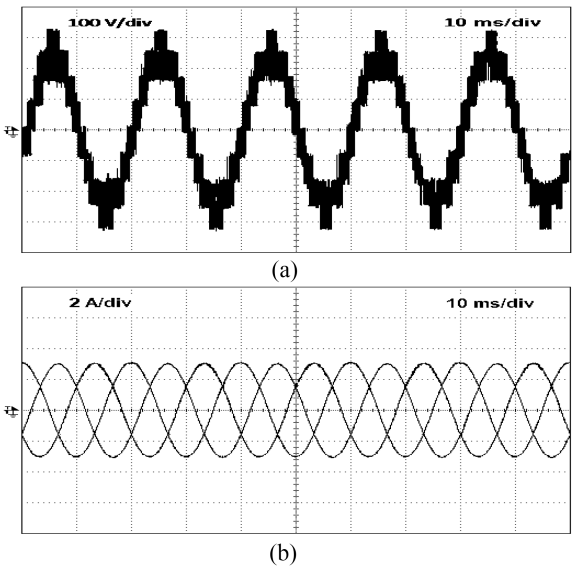

FIGURE 27. Obtained experimental waveforms for the S–T cells topology and PS-SPWM technique: (a) winding voltage *aa′* and (b) winding currents.

TABLE 5. Comparison of the Power Losses for the Two Proposed Topologies and PS-SPWM Technique (Experimental Tests)

Topology	IGBT's losses	Diode losses	Total losses
S-T cells	4.8%	0.5%	5.2 %
T-S cells	6.1%	0.7%	6.8 %

The efficiency of both topologies was also measured using the *PS-SPWM* technique. The obtained losses are given in Table 5. Analyzing these values reveals that they are consistent with what was expected. In terms of power losses, however, the IGBTs continue to have the highest impact, as demonstrated by previous tests.

VIII. CONCLUSION

A new multilevel inverter topology for drives feeding induction motors with open-end windings was proposed. The topology is characterized by a cascaded inverter in which it is possible to increase the NVL through the introduction of conventional single-phase H bridge inverters. Two topology configurations, the T–S cells topology, and the *S–T* cells topology were presented. It was verified that the *S–T* cells topology supplies a higher number of levels and higher voltages to the motor windings, with the same *dc* voltage source. This advantage can instead be used to use lower *dc* voltages and lower blocking voltage semiconductors needed for a given output power. Both the *T–S* cells topology and the *S–T* cells topology allow to use adapted conventional modulation strategies, such as *PD-SPWM*. Obtained experimental results confirm the number of levels and higher output voltages for *ST* cells topology. When using the maximum number of levels at high modulation indexes, the *PD-SPWM* method for the *T–S* cells topology applies asymmetric voltage waveforms to the motor windings. Consequently, the motor current shows a noticeable but still acceptable level of third harmonic. This issue almost disappears when using a lower NVL. The proposed inverter topology with two cascaded *T–S* cells or two *S–T* cells can apply to the motor winding a maximum voltage that is three or four times the value of the *dc* voltage sources, respectively. Output currents are nearly sinusoidal with measured *THD*s lower than 4.8% down to 0.39% when using *PD-SPWM*.

Although the proposed solution has been simulated and tested at low voltage (LV) scale. However, it can especially be appropriate to HV motors, where usually MMCs and the higher number of voltages applied improve the quality of currents requiring in this way smaller filters and produce lower losses than other solutions (as discussed in the paper). From the cost point of view, in HV, the proposed solutions are equivalent to usual solutions (as the number of converters is the same) and the main difference in cost is due to the substitution of one two-branch converter by a three-branch converters. Thus, the increasing in cost can be compensated by the saving in energy (as losses are lower taking into consideration the same NVL) or by needing smaller filters (as current quality is bigger).

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