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Coupled Inductor Assisted High-Voltage Gain Half-Bridge Z-Source Inverter

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ABSTRACT A half-bridge-based impedance-source inverter with two T-shaped coupled inductors is proposed in this article. Unlike the conventional half-bridge structure, the proposed topology can generate a zero-voltage level at its output stage. First, the proposed configuration and its modulation method are described, which will analyze the topology's various operational modes. Second, the boost factor is determined, and a way to design the necessary passive devices is found. Third, a power loss breakdown study is investigated in order to devise a solution to improve the efficiency of the proposed structure. Fourth, various comparisons show the benefits and drawbacks of the presented design. These comparisons show that the proposed topology can provide a high boost factor when coupled inductors are used. Furthermore, it has reduced voltage stresses on the components, resulting in a smaller size and lower cost. Finally, the experimental results are obtained by employing a prototype designed by the methodology presented in this article. These results are used as a benchmark to determine whether the proposed topology works well. In addition, the power loss analysis and efficiency comparison are displayed.

INDEX TERMS Half-bridge inverter, half-bridge-based Z-source inverter, impedance-source inverter, Z-source inverter.

I. INTRODUCTION

Z-source-based inverters (ZSI) have recently gained popularity due to their unique characteristics, such as buck/boost voltage gain, without requiring a two-staged converter, and supporting short-circuit states known as shoot-through (ST) states [1], [2]. Peng [3] shows the first Z-source inverter, which has an impedance cell consisting of two capacitors and two inductors. This topology's configuration includes a diode in its input path. As a result, this structure has a discontinuous input current and cannot be used in applications that require a continuous input current. Furthermore, the capacitors must withstand high-voltage stress, and the output boost factor is insufficient. As a result, some additional structures are presented to alleviate the problems associated with basic ZSI. For example, the quasi-Z-source inverter (QZSI) [4] has a continuous input current and less voltage stress on the capacitors compared to ZSI. In addition, the embedded Z-source structure [5], which employs two dc voltage sources, resolves the input current discontinuity. However, the boost factor of these structures is the same as that of the basic ZSI configuration. In trying to increase the boost factor of these topologies, researchers have presented an array of configurations in the literature.

Using switched inductors to improve the output boost factor is one option. Switched inductor cells [6] replace the simple inductors used in the ZSI structure. Loh and Blaabjerg [7] showed another topology that employs switched inductor cells. This topology replaces one of the QZSI structure's inductors with a switched inductor cell. In this technique, both inductors are charged in the ST states and then discharged on the output stage in the other states, increasing the output boost factor. However, using this technique demands many passive devices, resulting in an excessive volume and high cost. Furthermore, capacitors must withstand high voltage, resulting in a greater volume.

Another method for increasing boost factor is to use coupled inductors. Furthermore, the voltage stress on the other components is significantly reduced due to the using of the

coupled inductors. Having the different turns number in the primary and secondary windings of a set of coupled inductors, these coupled inductors can increase the boost factor in the output stage without forcing devices, including active and passive ones, to bear high-voltage stress. In the literature, there is a good deal of impedance-source-based topologies with coupled inductors. For example, Qian et al. [8] described the trans-Z-source inverter, which replaces the QZSI's inductors with coupled inductors. It is required to note that one capacitor is mitigated in this topology, resulting in a lower component count. Loh and Blaabjerg [7] presented various topologies based on the shape of the coupled inductors, including T-source, Γ-source, and flipped Γ-source configurations. Divya and Prabhu [9] presented another topology that employs coupled inductors. In this topology, two inductors are used instead of one of the QZSI's inductors, resulting in a higher boost factor. Siwakoti et al. [10] presented another structure called the Y-source inverter, which employs three-winding coupled inductors. Because of the coupling of three windings, the boost factor is high in this structure, but its complexity is high. Another topology that uses coupled inductors is presented in [11], in which two coupled inductors are added to the basic ZSI structure. The boost factor increases in this topology due to coupled inductors, but it suffers from the same issues as the basic ZSI configuration. As previously stated, adding coupled inductors can cause a higher output boost factor and lower voltage stress on capacitors, but they have an inherent flaw. Because of their magnetic flux losses, coupled inductors always have a small leakage inductor. Because of the current flowing through it, the inductor mentioned above becomes charged in the ST state. The issue arises during the transition from an ST to a normal state. A path for discharging the energy of this inductor cannot be found in this situation. This problem causes clamping diodes, as demonstrated by [12].

Another type of impedance-source inverter includes a switch in its impedance-source cell, resulting in reduced components, especially passive devices. Ravindranath et al. [13] showed an example of this type of impedance-source topology in which a switch is added to the impedance side, but the number of passive devices is reduced. Compared to the basic ZSI topology, the switched Z-source topology has a lower boost factor, but the number of devices and the voltage stresses on these devices are reduced.

Other impedance-source inverters use a half-bridge inverter at their output stage. For instance, Babaei and Asl [14] presented a topology that includes two cells similar to the ZSI topology. This topology is intended to be used in electrochemical applications. Nevertheless, the boost factor of this configuration does not have any improvements over the ZSI's boost factor, and the use of a high number of components overshadows its novelty. Babaei and Asl [15] presented another half-bridge-based topology constructed from the basic impedance cell. While this topology allows for a low number of devices, its boost factor is still low. Adding coupled inductors to these topologies is a way to increase their boost factor. Different topologies are presented in [16], [17], and [18] regarding this description. The structure presented in [16] permits using a low number of devices to give a high boost factor. However, the presented topology in [17] comprises an even lower number of devices. With these structures, it can be seen that they can make a voltage level of zero, but the traditional half-bridge inverter cannot make this voltage level at its output stage.

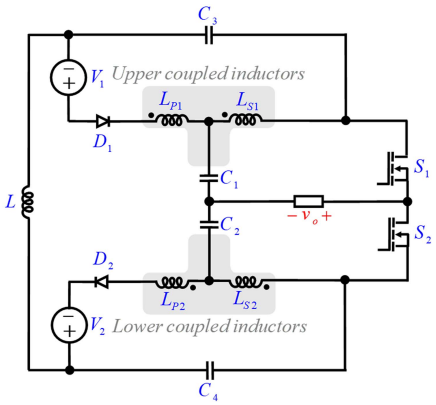

FIGURE 1. Proposed half-bridge-based Z-source inverter.

A new half-bridge-based impedance-source inverter topology is presented in this article. The coupled inductors in this structure are configured in T format, allowing for a high boost factor to be conducted to the output stage. First, the configuration of the proposed design and the appropriate modulation method are investigated in Section II. Then, in Section III, various analyzes for this topology to determine its boost factor are presented. Then, multiple studies for this topology to determine its boost factor are given and some equations for dimensioning passive devices and power loss calculation. After that, various comparisons are made to compare the proposed configuration's features with those of other structures in Section IV. Finally, in order to collect experimental data, a prototype based on the method used in this article was designed in Section V. These findings are being used to test the validity of the proposed topology. Moreover, the power loss breakdown is investigated, and the efficiency of the proposed structure is compared to other configurations to determine which works best.

II. PROPOSED HALF-BRIDGE-BASED Z-SOURCE CONFIGURATION

Fig. 1 depicts the power circuit of the proposed structure. As illustrated in the figure, this topology has two coupled inductors. The proposed topology includes four capacitors, two diodes, two power switches, two dc voltage sources, and one inductor. Furthermore, the magnitudes of the input dc voltage sources can be selected to be unequal in the general form. Two power switches are presented, each with its own set of gate pulse signals. The method for obtaining these two gate pulse signals is depicted in Fig. 2. The modulation method's input parameters are four signals: U_{ST1}, U_{ST2}, U_{tri}, and U_{step}. First, two reference levels of U_{ST1} and U_{ST2} are compared to

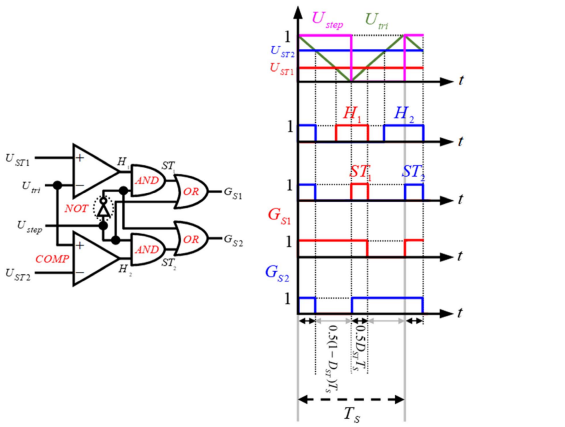

FIGURE 2. Way to obtain gate pulse signals.

a triangular carrier waveform called U_{tri}. As a result of these comparisons, two signals of H_1 and H_2 are obtained, where H_1 is the same as one when U_{ST1} is greater than U_{tri}.

Similarly, H_2 is equal to one when U_{ST2} is lower than U_{tri}. Second, the signals of ST_1 and ST_2 are obtained with H_1, H_2, U_{step}, and the logical operators. U_{step} is a pulse signal that is the same as one in the first half-period and zero in the other half-period.

Regarding these descriptions, ST_1 is obtained from the logical AND of H_1 and the logical NOT of U_{step}. Similarly, ST_2 is obtained from the logical AND of H_2 and U_{step}. Third, the gate pulse signals of G_{S1} and G_{S2} are obtained using ST_1, ST_2, U_{step}, and the logical operators. G_{S1} is obtained from the logical OR of ST_1 and U_{step}. Also, G_{S2} is obtained from the logical OR of ST_2 and the logical NOT of U_{step}.

It is seen that there are four operational states for the proposed half-bridge-based impedance-source inverter by considering the obtained pulse gate signals. Both switches are turned ON simultaneously in the first state, which leads to an ST state. In the second working mode, S_1 is switched ON, and the other switch, named S_2 is turned OFF. In the subsequent operational mode, both switches are switched ON which is the same as what has happened in the first operational mode. Finally, the switch of S_2 is switched ON and the other switch is turned OFF in the fourth operational state. It is important that it is considered that this control method can be used regardless of the magnitudes of the dc voltage sources. However, the magnitude of zero may not be generated if the conditions of the circuit are not identical. It is required to mention T_{ST} stands for the period when both switches are ON. By having this definition, D_{ST}, the ST duty cycle, can be declared as T_{ST} divided by T_S, the switching period. Each of these operational states is analyzed in the next section in detail.

III. ANALYSIS OF THE SUGGESTED STRUCTURE

Some assumptions must be made before proceeding with the analysis of the proposed half-bridge-based impedance-source inverter. First, the operational states of the proposed topology are thoroughly examined using these assumptions. The boost factor of this topology is then calculated using the results of the analysis of the operational mode. Then, some equations will be generated to estimate the required passive components, such as capacitors and inductors. Furthermore, the voltage and current ratings of active devices, such as switches and diodes, are obtained. Finally, a power loss analysis is performed to determine the efficiency of the proposed topology.

A. ANALYSIS OF THE OPERATIONAL STATES

1) The coupled inductors are modeled as ideal transformers parallel with a magnetizing inductor (L_m). In addition, the leakage effect of the coupled inductors is modeled as a leakage inductor (L_k) connected in series with the ideal transformer. It is supposed that the numbers of turns of the primary and secondary windings are the same as N_1 and N_2, respectively. By considering this assumption, the following equation can be written for the voltages and currents of the ideal transformers:

$$\frac{v_1}{v_2} = \frac{i_{P2}}{i_{P1}} = \frac{i_{N2}}{i_{N1}} = \frac{N_1}{N_2} = N_{12}. \tag{1}$$

As seen from (1), N_{12} is supposed as N_1 divided by N_2. It is required to mention that the following equation can be considered to estimate the leakage inductor's voltage as the last point about the coupled inductors:

$$v_{Lk} = g\, v_{Lm} \tag{2}$$

where v_{Lk} and v_{Lm} are the voltages of the leakage inductor and magnetizing inductor, respectively. Moreover, g is a related parameter to the coupled inductors, generally ranging from 0.01 to 0.03.

2) The capacitors are supposed to be large enough. As a result, all capacitors' instantaneous and average voltage can be considered the same. Also, the type of load is regarded as the ohmic type with the value of R.

The equivalent circuits for each operational state can be obtained following the modulation method and the taken assumptions. Fig. 3 depicts these equivalent circuits for each operating state. Analyzing the voltage and current of each element regarding these circuits can be done using Kirchhoff's voltage and current laws (KVL and KCL). Also, two fundamental equations of $v_L{=}L\, di_L/dt$ and $i_C{=}C\, dv_C/dt$ are used in these analyses.

1) FIRST STATE ($0 < T < 0.5D_{\text{ST}}T_S$)

As seen in Fig. 3(a), both switches are turned ON, leading to the OFF state for both diodes. The following equations can be obtained using KCL:

$$i_{P1} = i_{N1} = -i_{Lm} \tag{3}$$

$$C_1 \frac{dv_{C1}}{dt} = C_2 \frac{dv_{C2}}{dt} = -N_{12} i_{Lm} \tag{4}$$

$$C_3 \frac{dv_{C3}}{dt} = C_4 \frac{dv_{C4}}{dt} = -i_L. \tag{5}$$

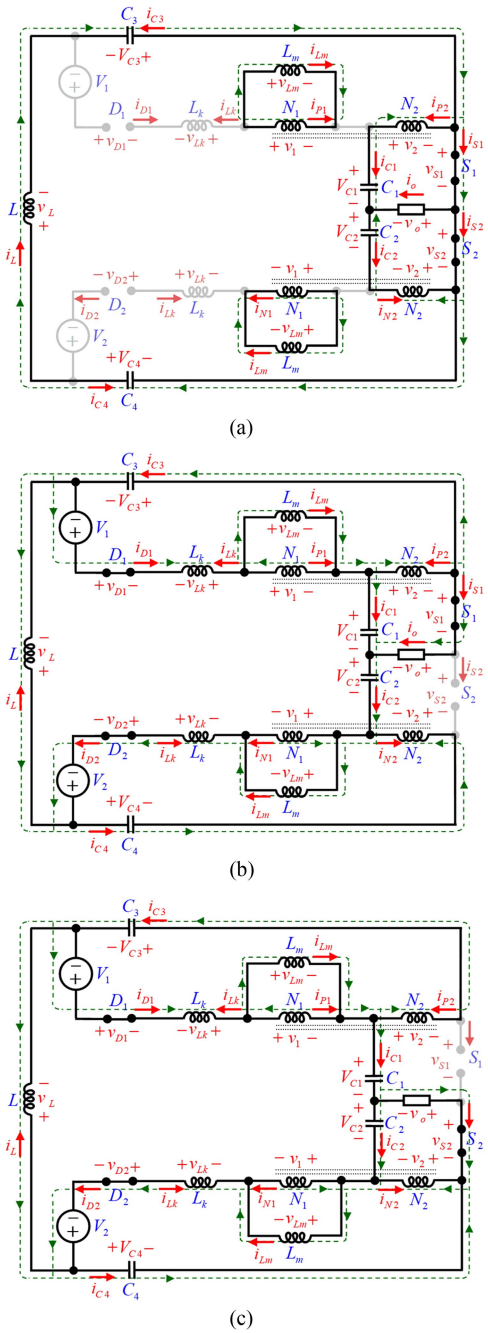

FIGURE 3. Equivalent circuits in each of the operational states: (a) first and third state, (b) second state, and (c) fourth state.

Regarding (4), it can be obtained that

$$i_o = 0. \tag{6}$$

Also, the following equations can be driven for the currents of diodes and switches:

$$i_{D1} = i_{D2} = 0 \tag{7}$$

$$i_{S1} = i_{S2} = i_L + N_{12} i_{Lm} \tag{8}$$

$$v_o = 0 \tag{9}$$

$$V_{C1} = V_{C2}. \tag{10}$$

Regarding (6) and the ohmic output load, the following equations can be obtained for the output voltage in this mode and the voltages of C_1 and C_2:

Also, other voltages can be obtained as follows using KVL:

$$L\frac{di_L}{dt} = V_{C3} + V_{C4} \tag{11}$$

$$L_m\frac{di_{Lm}}{dt} = v_1 = N_{12}V_{C1} \tag{12}$$

$$\begin{aligned} v_{D1} = v_{D2} &= -[1 + N_{12}(1-g)]\,V_{C1} - (V_{C3} - V_1) \\ &= -[1 + N_{12}(1-g)]\,V_{C1} - (V_{C4} - V_2) \end{aligned} \tag{13}$$

$$v_{S1} = v_{S2} = 0. \tag{14}$$

Regarding (12), it can be concluded that

$$V_{C3} - V_1 = V_{C4} - V_2. \tag{15}$$

Both diodes' voltages are negative regarding (13), so they will be turned OFF as was assumed. Also, it is required to describe that (10) and (15) are valid for the other operational states because the capacitors' voltages remain constant in every state.

2) SECOND STATE ($0.5D_{ST}T_S < T < 0.5T_S$)

S_1 and S_2 are turned ON and OFF in this state. Also, both diodes are in the ON state. The following equations can be derived using Fig. 3(b) and KVL:

$$L\frac{di_L}{dt} = -2V_{C1} + \frac{2N_{12}(1-g)(V_{C3} - V_1)}{1 + N_{12}(1-g)} + V_1 + V_2 \tag{16}$$

$$L_m\frac{di_{Lm}}{dt} = v_1 = -\frac{N_{12}(V_{C3} - V_1)}{1 + N_{12}(1-g)}. \tag{17}$$

The output voltage, which is positive, can be obtained as follows using (17), where V_{om} is the maximum magnitude of the output voltage:

$$v_o = V_{om} = V_{C1} + \frac{V_{C3} - V_1}{1 + N_{12}(1-g)}. \tag{18}$$

In addition, the active components' voltages can be obtained

$$v_{D1} = v_{D2} = 0 \tag{19}$$

$$v_{S1} + 2V_{om} = v_{S2} = 2V_{om}. \tag{20}$$

Also, the passed currents through every component can be obtained as follows using KCL:

$$i_o = I_{om} = \frac{V_{om}}{R} \tag{21}$$

$$C_1\frac{dv_{C1}}{dt} + I_{om} = C_2\frac{dv_{C2}}{dt} = i_L \tag{22}$$

$$C_3\frac{dv_{C3}}{dt} + \frac{I_{om}}{1 + N_{12}} = C_4\frac{dv_{C4}}{dt} = \frac{N_{12}(i_{Lm} - i_L)}{1 + N_{12}} \tag{23}$$

$$i_{P1} + \frac{I_{om}}{1+N_{12}} = i_{N1} = -\frac{i_{Lm} - i_L}{1+N_{12}} \tag{24}$$

$$i_{D1} + \frac{I_{om}}{1+N_{12}} = i_{D2} = \frac{N_{12} i_{Lm} + i_L}{1+N_{12}} \tag{25}$$

$$i_{S1} = i_{S2} + I_{om} = I_{om}. \tag{26}$$

The passed currents through both diodes are positive regarding (25). So the taken assumption about these diodes is right. It is required to note that both output voltage and output current are positive in this operational state and are at their maximum value. So the output voltage and output current are named as V_{om} and I_{om} in this operational mode.

3) THIRD STATE ($0.5T_S < T < 0.5(1+D_{ST})T_S$)

The first and third operational modes are identical regarding Fig. 3(a). So this mode is not analyzed, and (3)–(15) are also valid for this operational state.

4) FOURTH STATE ($0.5(1+D_{ST})T_S < T < T_S$)

The second and fourth operational states have some similarities regarding Fig. 3(b) and (c). In this operational mode, S_1 and S_2 are turned OFF and ON. Also, both diodes are in the ON state, the same as the second operational state. Equations (16) and (17) are valid for this operational mode because of the symmetry of Fig. 3(b) and (c). The output voltage can be obtained as follows using (16) and (17):

$$v_o = -V_{om} = -V_{C1} - \frac{V_{C3} - V_1}{1 + N_{12}(1-g)}. \tag{27}$$

The output voltage is negative in this operational mode, as seen in (27). Furthermore, the voltages on diodes and switches can be obtained

$$v_{D1} = v_{D2} = 0 \tag{28}$$

$$v_{S1} = v_{S2} + 2V_{om} = 2V_{om}. \tag{29}$$

Moreover, the passing currents through all components can be got as follows using Fig. 3(c) and KCL:

$$i_o = -I_{om} = -\frac{V_{om}}{R} \tag{30}$$

$$C_1 \frac{dv_{C1}}{dt} = C_2 \frac{dv_{C2}}{dt} + I_{om} = i_L \tag{31}$$

$$C_3 \frac{dv_{C3}}{dt} = C_4 \frac{dv_{C4}}{dt} + \frac{I_{om}}{1+N_{12}} = \frac{N_{12}(i_{Lm} - i_L)}{1+N_{12}} \tag{32}$$

$$i_{P1} = i_{N1} + \frac{I_{om}}{1+N_{12}} = -\frac{i_{Lm} - i_L}{1+N_{12}} \tag{33}$$

$$i_{D1} = i_{D2} + \frac{I_{om}}{1+N_{12}} = \frac{N_{12} i_{Lm} + i_L}{1+N_{12}} \tag{34}$$

$$i_{S1} + I_{om} = i_{S2} = I_{om}. \tag{35}$$

Both diodes pass positive currents regarding (34), so the claim to their ON state is true. Furthermore, the evidence shows that the output voltage and output current are equal to $-V_{om}$ and $-I_{om}$ in this operational mode, which shows that they are in the minimum state. In the following subsection, the boost factor of the proposed topology will be estimated using the analyzes of the operational modes.

B. BOOST-FACTOR CALCULATION

To calculate the boost factor of the proposed half-bridge-based impedance-source structure, apply the voltage-balance law. This law states that the average voltage on an inductor over a period is equal to zero. In the proposed structure, there are two types of inductors: regular inductors and magnetizing inductors. Applying the voltage-balance law to these inductors yields the average voltage on the capacitors

$$V_{C1} = V_{C2} = \frac{1 - D_{ST}}{1 - \left[2 + N_{12}(1-g)\right] D_{ST}} \frac{V_1 + V_2}{2} \tag{36}$$

$$V_{C3} - V_1 = V_{C4} - V_2 = \frac{\left[1 + N_{12}(1-g)\right] D_{ST}}{1 - \left[2 + N_{12}(1-g)\right] D_{ST}} \frac{V_1 + V_2}{2}. \tag{37}$$

By supposing (36) and (37) in the V_{om} equation shown in (18), the maximum magnitude of the output voltage can be obtained. Using this supposition, we can obtain the following equation:

$$V_{om} = \frac{1}{1 - \left[2 + N_{12}(1-g)\right] D_{ST}} \frac{V_1 + V_2}{2}. \tag{38}$$

The boost factor of the suggested structure can be obtained from (38)

$$B = \frac{2V_{om}}{V_1 + V_2} = \frac{1}{1 - \left[2 + N_{12}(1-g)\right] D_{ST}}. \tag{39}$$

C. DESIGN OF PASSIVE AND ACTIVE COMPONENTS

First, we are going to obtain the required passive devices, including capacitors and inductors. After, the voltage and current stresses of the active devices, such as switches and diodes, are calculated. The average voltage of the capacitors, the average passed current through the inductors, the capacitors' voltage ripples, and the inductors' current ripples must be calculated to design the passive components. The average voltages on the capacitors were previously calculated in (36) and (37) using the voltage-balance law. A similar approach, named current-balance law, must obtain the average passed current through the inductors. Regarding it, the average passed current through a capacitor in a period equals zero. By applying this law to the got results from operational modes analysis, the following equations can be obtained:

$$I_L = \frac{1 - D_{ST}}{2R\left[1 - (2 + N_{12})D_{ST}\right]\left[1 - (2 + N_{12}(1-g))D_{ST}\right]} \times \frac{V_1 + V_2}{2} \tag{40}$$

$$I_{Lm} = \frac{(1 + N_{12})(1 - D_{ST})}{2N_{12}R\left[1 - (2+N_{12})D_{ST}\right]\left[1 - (2+N_{12}(1-g))D_{ST}\right]} \times \frac{V_1 + V_2}{2} \tag{41}$$

where I_L and I_{Lm} depict the average current that passes through the inductors of L and L_m, respectively. After obtaining these parameters, we must obtain the current ripple of the inductors to design their inductances. Supposing one of the operational states and applying the fundamental equation of an inductor (v_L=L di_L/dt) in this operational state. The inductors' current ripple results can be obtained by supposing the second operational state and paying attention to the fact that this state lasts for $0.5(1-D_{ST})T_s$

$$|\Delta i_L| = \frac{D_{ST}(1-D_{ST})}{L f_s \left[1-(2+N_{12}(1-g))D_{ST}\right]} \frac{V_1+V_2}{2} \tag{42}$$

$$|\Delta i_{Lm}| = \frac{N_{12} D_{ST}(1-D_{ST})}{2L_m f_s \left[1-(2+N_{12}(1-g))D_{ST}\right]} \frac{V_1+V_2}{2} \tag{43}$$

where $|\Delta i_L|$ and $|\Delta i_{Lm}|$ show the absolute current ripple of L and L_m, respectively. Besides, f_s depicts the switching frequency that equals one divided by T_s. Similarly, capacitor voltage ripples can be obtained by using the fundamental equation of a capacitor ($i_C = C\ dv_C/dt$) in the second operational state

$$|\Delta v_{C1,2}| = \frac{(1-D_{ST})^2}{4RC_1 f_s \left[1-(2+N_{12})D_{ST}\right]\left[1-(2+N_{12}(1-g))D_{ST}\right]} \times \frac{V_1+V_2}{2} \tag{44}$$

$$|\Delta v_{C3,4}| = \frac{(1-D_{ST})^2}{4RC_3 (1+N_{12}) f_s \left[1-(2+N_{12})D_{ST}\right]\left[1-(2+N_{12}(1-g))D_{ST}\right]} \times \frac{V_1+V_2}{2} \tag{45}$$

where $|\Delta v_C|$ shows the absolute voltage ripple of capacitors. The values of inductances and capacitances can be obtained through (36), (37), and (40)–(45), which are based on $|\Delta i_L| = x_L\%\ I_L$ and $|\Delta v_C| = x_C\%\ V_C$

$$L = \frac{2D_{ST}R\left[1-(2+N_{12})D_{ST}\right]}{x_L\%\ f_s} \tag{46}$$

$$L_m = \frac{N_{12}^2 D_{ST}R\left[1-(2+N_{12})D_{ST}\right]}{(1+N_{12})\,x_{Lm}\%\ f_s} \tag{47}$$

$$C_1 = C_2 = \frac{(1-D_{ST})^2}{4R\left[1-(2+N_{12})D_{ST}\right]x_{C1}\%f_s} \tag{48}$$

$$C_3 = C_4 = \frac{(1-D_{ST})^2}{4R\,(1+N_{12})\left[1-(2+N_{12})D_{ST}\right]\ x_{C3}\%f_s}. \tag{49}$$

The leakage inductors associated with the coupled inductors do not affect the passive components' values, as seen from (46) to (49). Estimating the current and voltage stresses of the switches and diodes is required to complete the design process. These equations are depicted as follows:

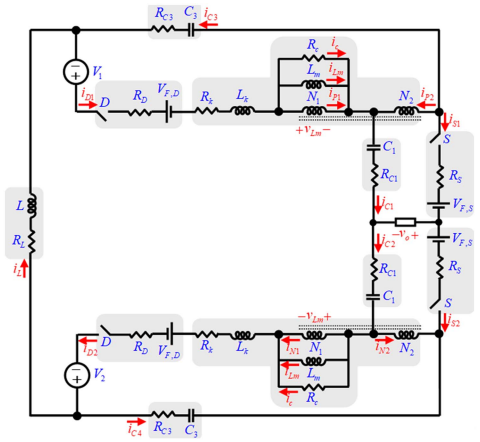

FIGURE 4. Practical model of the suggested structure to obtain its power losses.

$$V_S = \frac{2}{1-\left[2+N_{12}(1-g)\right]D_{ST}} \frac{V_1+V_2}{2} \tag{50}$$

$$\text{PIV}_D = \frac{1+N_{12}(1-g)}{1-\left[2+N_{12}(1-g)\right]D_{ST}} \frac{V_1+V_2}{2} \tag{51}$$

$$I_S = \frac{(2+N_{12})(1-D_{ST})}{2R\left[1-(2+N_{12})D_{ST}\right]\left[1-(2+N_{12}(1-g))D_{ST}\right]} \times \frac{V_1+V_2}{2} \tag{52}$$

$$I_D = \frac{(2+N_{12})(1-D_{ST})}{2R\,(1+N_{12})\left[1-(2+N_{12})D_{ST}\right]\left[1-(2+N_{12}(1-g))D_{ST}\right]} \times \frac{V_1+V_2}{2} \tag{53}$$

where V_S and I_S are the switches' voltage and current stress, respectively. Besides, PIV_D and I_D show diodes' peak inverse voltage and current stress, respectively.

D. POWER LOSS STUDY

In this section, the components' power losses consumed are studied to assess the efficiency of the proposed half-bridge-based impedance-source structure. As shown in Fig. 1, the proposed design contains a variety of devices, including switches, diodes, coupled inductors, inductors, and capacitors. These devices were thought to be ideal for analyzing the operational mode. Nonetheless, each component consumes a portion of the input power in practice. In order to calculate the power losses of each part, a practical model of the proposed structure is provided in Fig. 4. When switched or diodes are turned ON, they can be represented as a voltage drop next to a resistor. As seen in Fig. 4, $V_{F,S}$ and R_S for switches depict these voltage drops and resistors. Besides, they are symbolized by $V_{F,D}$ and R_D for diodes. Also, the model of a magnetizing device is used to model the power losses of the coupled inductors, including R_k as the leakage resistor and

TABLE 1. Detailed Power Losses Associated With Different Components

Switches	$P_{S1,cond} = P_{S2,cond}$	$V_{F,S}\left[(I_L + N_{12}I_{Lm})D_{ST} + 0.5\,I_{om}\,(1-D_{ST})\right]$ $+R_S\left[(I_L + N_{12}I_{Lm})^2 D_{ST} + 0.5\,{I_{om}}^2\,(1-D_{ST})\right]$	$P_S = 2(P_{S1,cond} + P_{S1,sw})$
	$P_{S1,sw} = P_{S2,sw}$	$\frac{1}{6}(2V_{om})(I_L + N_{12}I_{Lm})(t_{on} + t_{off})f_s$	
Diodes	$P_{D1,cond} = P_{D2,cond}$	$V_{F,D}\left[0.5\,\frac{2N_{12}I_{Lm} + 2I_L - I_{om}}{1+N_{12}}\,(1-D_{ST})\right]$ $+R_D\left\{0.5(1-D_{ST})\left[\left(\frac{N_{12}I_{Lm} + I_L}{1+N_{12}}\right)^2 + \left(\frac{N_{12}I_{Lm} + I_L - I_{om}}{1+N_{12}}\right)^2\right]\right\}$	$P_D = 2(P_{D1,cond} + P_{D1,sw})$
	$P_{D1,sw} = P_{D2,sw}$	$\frac{1}{6}\left\{\left[1 + N_{12}(1-g)\right]V_{om}\right\} I_{rr}\,t_b\,f_s$	
Coupled Inductors	P_{Rk}	$R_k\left\{D_{ST}{I_{Lm}}^2 + 0.5(1-D_{ST})\left[\left(\frac{I_{Lm} - I_L}{1+N_{12}}\right)^2 + \left(\frac{I_{Lm} - I_L - I_{om}}{1+N_{12}}\right)^2\right]\right\}$	$P_{coupled\ inductors} = 2(P_{Rk} + P_{Rc})$
	P_{Rc}	$\frac{1}{R_c}\left\{(N_{12}V_{C1})^2 D_{ST} + \left[\frac{N_{12}(V_{C3} - V_1)}{1 + N_{12}(1+g)}\right]^2 (1-D_{ST})\right\}$	
Passive Devices	$P_{C1} = P_{C2}$	$R_{C1}\left\{(N_{12}I_{Lm})^2 D_{ST} + 0.5(I_L - I_{om})^2(1-D_{ST}) + 0.5\,{I_L}^2(1-D_{ST})\right\}$	$P_{passive} = 2(P_{C1} + P_{C2}) + P_L$
	$P_{C3} = P_{C4}$	$R_{C3}\left\{{I_L}^2 D_{ST} + 0.5\left[\frac{N_{12}(i_{Lm} - i_L) - I_{om}}{1+N_{12}}\right]^2 (1-D_{ST}) + 0.5\left[\frac{N_{12}(i_{Lm} - i_L)}{1+N_{12}}\right]^2 (1-D_{ST})\right\}$	
	P_L	$R_L{I_L}^2$	

R_c as the core resistor. Moreover, an equivalent series resistor is used for capacitors and inductors named by R_C and R_L to model their power losses.

The power losses associated with switches, diodes, coupled inductors, capacitors, and inductors are listed in Table 1. Table 1 shows that switches and diodes have two types of power losses, including conduction losses ($P_{S,\text{cond}}$ for switches and $P_{D,cond}$ for diodes) and switching losses ($P_{S,\text{sw}}$ for switches and $P_{D,\text{sw}}$ for diodes). Besides, t_{ON} and t_{OFF} depict the turning-ON and turning-OFF times for switches. Similarly, I_{rr} and t_b show the reverse-recovery current for diodes and a time associated with the diodes' switching.

The following equation can be used to estimate the output power:

$$P_{\text{output}} = V_{om}\,I_{om}\,(1 - D_{\text{ST}}). \tag{54}$$

Regarding Table 1 and (54), the efficiency of the suggested structure can be obtained from the following:

$$\eta\,\% = \frac{P_{\text{output}}}{P_{\text{output}} + P_S + P_D + P_{\text{coupled inductors}} + P_{\text{passive}}} \times 100. \tag{55}$$

IV. COMPARISON ASSESSMENT

This section aims to compare the features of the suggested structure with the other existing topologies. The elements used in the comparison assessment are boost factor, capacitors' voltage stresses, diodes' voltage stresses, switches' voltage stresses, and the number of required devices. As previously explained, the presented structure is based on the half-bridge configuration. Therefore, it is better to compare it with similar half-bridge-based structures. However, the number of existing half-bridge-based topologies is limited. So it is compared the presented system with the other Z-source inverter shown by other researchers in the boost-factor comparison. However, some of the existing half-bridge-based Z-source inverters are used in the other detailed comparisons. This section includes two subsections. The different factors and indexes of the suggested structure are analyzed in the first subsection. After, the proposed design is compared with the existing ones to determine the advantages and disadvantages of the recommended configuration.

A. EVALUATION OF THE PROPOSED STRUCTURE

The proposed topology has two dc voltage sources, which have different magnitudes. The maximum output voltage generated by the suggested structure was obtained in (38). It can be shown that this equation is at its maximum if both dc voltage sources have equal magnitudes. So it is supposed that V_1 and V_2 are the same as V_i to analyze the suggested structure indexes. The different indexes of the proposed structure, including boost factor and total voltage stresses on the capacitors, diodes, and switches, can be obtained as follows regarding these assumptions:

$$B = \frac{V_{om}}{V_i} = \frac{1}{1 - \left[2 + N_{12}(1-g)\right]D_{\text{ST}}} \tag{56}$$

$$V_{C,\text{total}} = \frac{4(1 - D_{\text{ST}})}{1 - \left[2 + N_{12}(1-g)\right]D_{\text{ST}}} \tag{57}$$

$$V_{D,\text{total}} = \frac{2\left[1 + N_{12}(1-g)\right]}{1 - \left[2 + N_{12}(1-g)\right]D_{\text{ST}}} \tag{58}$$

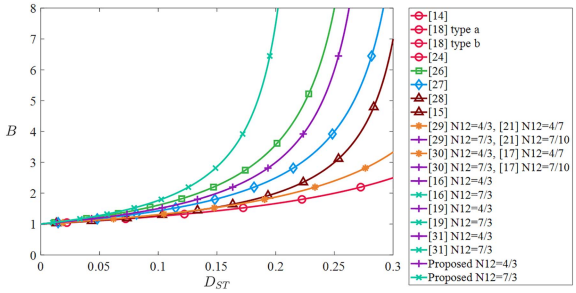

FIGURE 5. Boost-factor comparison (B: boost factor, D_{ST}: ST state's duty cycle).

$$V_{S,\text{total}} = \frac{4}{1-\left[2+N_{12}(1-g)\right]D_{\text{ST}}}. \tag{59}$$

As seen in (56)–(59), these parameters depend on the leakage inductor besides the coupled inductors' turn ratios and the ST duty cycle. Also, the boost factor and the voltages on different components will reduce if the leakage inductors are increased.

B. BOOST-FACTOR COMPARISON

As mentioned before, the boost factor of the suggested structure is compared with the same parameter in the existing Z-source inverters. The comparison plots are depicted in Fig. 5. The effect of the leakage inductors is neglected in these comparisons to have a fair comparison. Moreover, the topologies considered in the comparison are presented in [14], [15], [16], [18], [19], [24], [27], [28], [29], [30], [31]. Regarding Fig. 5, structures including the coupled inductors are supposed to have greatest boost factors compared to other topologies. Including coupled inductors, the proposed topology can produce the highest boost factor among other topologies. However, it is seen that the permittable period for D_{ST} is the lowest for this situation, regarding the inverse relation between boost factor and this parameter. Also, it is seen that the structure presented in [19] always has a boost factor half of that of the proposed structure. Moreover, it is seen that for the topologies, which include coupled-inductors, the higher N_{12} is, the higher boost factor is.

C. DETAILED COMPARISON WITH HALF-BRIDGE-BASED TOPOLOGIES

As previously stated, it is preferable to contrast the proposed structure with other existing half-bridge-based Z-source topologies. This article can provide more detailed comparisons based on factors, such as total voltage stresses and component count. As illustrated in Fig. 6, the existing structure in [26] requires the highest device count. In addition, the same structures suffer from a high amount of voltage not only on diodes but also on power switches according to Fig. 6(a) and (b).

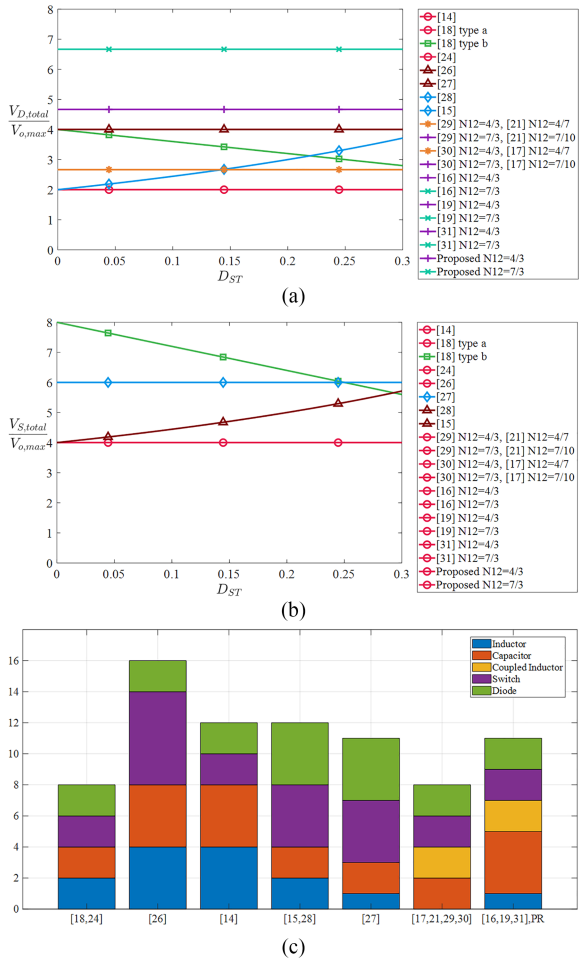

FIGURE 6. Detailed comparison of the suggested structure with the other similar topologies (a) from diodes' total voltage stresses aspect ($V_{D,\text{total}}$: sum of the diodes' voltage stresses, BV_i: maximum magnitude of the output voltage, D_{ST}: ST state's duty cycle), (b) from switches' total voltage stresses aspect ($V_{S,\text{total}}$: sum of the switches' voltage stresses, BV_i: maximum magnitude of the output voltage, D_{ST}: ST state's duty cycle), and (c) from the components count aspect.

With regard to Fig. 6(a) and (b), it can be seen that the diodes used in proposed topology have to endure a high-voltage stress on them; however, the voltage stress on the output switches is reduced. Nonetheless, this topology requires numerous components according to Fig. 6(c). Also, it can be seen that unlike topologies presented in [17] and [21], the proposed topology does require an additional inductor. With regard to boost-factor comparison, it can be seen that the effect of using this inductor shows its advantage in increasing boost factor because it is charged in non-ST state and discharged to the output stage in the other state. Because of the reduced voltage stresses on the active devices and the low number of required components, the proposed topology has the best situation among all half-bridge-based topologies.

The components stress factor (CSF) and switching devices' power (SDP) are the other indexes that can be considered enhancing the comparative study. For a converter, CSF can be

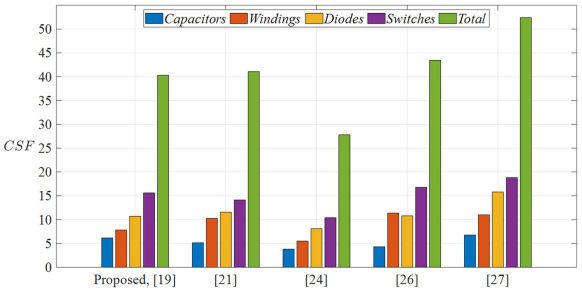

FIGURE 7. Comparison from the components stress factor view.

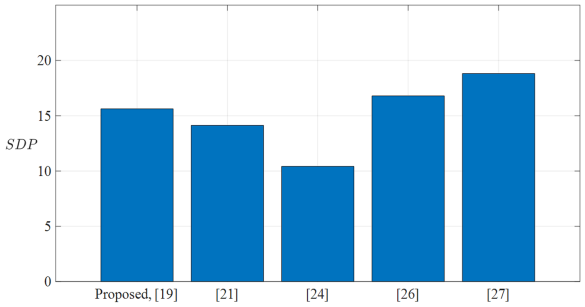

FIGURE 8. Comparison from the switching devices' power view.

torn down into different components, including SCSF, DSCF, WSCF, and CSCF, which are related to the power switches, diodes, windings, such as inductors and coupled inductors, and capacitors. Each of these components can be obtained as follows [32]:

$$\text{SCSF} = \sum_{j=1}^{N_s} \frac{V_{S,j(\max)} \times I_{S,j(\text{rms})}}{P_{\text{out}}} \tag{60}$$

$$\text{DCSF} = \sum_{j=1}^{N_D} \frac{V_{D,j(\max)} \times I_{D,j(\text{rms})}}{P_{\text{out}}} \tag{61}$$

$$\text{WCSF} = \sum_{j=1}^{N_W} \frac{V_{L,j(\max)} \times I_{L,j(\text{rms})}}{P_{\text{out}}} \tag{62}$$

$$\text{CCSF} = \sum_{j=1}^{N_C} \frac{V_{C,j(\max)} \times I_{C,j(\text{rms})}}{P_{\text{out}}} \tag{63}$$

where N_S, N_D, N_W, and N_C are the count of the used switches, diodes, windings, and capacitors in each configuration. Regarding these equations, the comparison from the CSF point of view can be depicted in Fig. 7. It is required to note that it is assumed that the input and voltages are the same as 20 and 100 V for all the topologies to have a fair comparison.

As seen in Fig. 7, the existing topology in [24] has the lowest CSF among the other topologies because of the lowest voltage stresses on the diodes and capacitors. The second lowest CSF among other topologies belong to the proposed topology as well as the one existing in [19]. Another comparison is SDP, which gives a numeric result about the powers of the switches that are used in different topologies. Regarding the given descriptions, the results can be depicted in Fig. 8.

Regarding Fig. 8 and comparing it with Fig. 6(b), it can be seen that the proposed topology and the presented ones in [19], [21], and [26] have the same voltage stresses on their switches. However, their SDP indexes are different, which point out that the passed current through these switches is not the same.

V. EXPERIMENTAL RESULTS

This section aims to indicate the experimental results for the proposed half-bridge-based Z-source inverter to ensure its

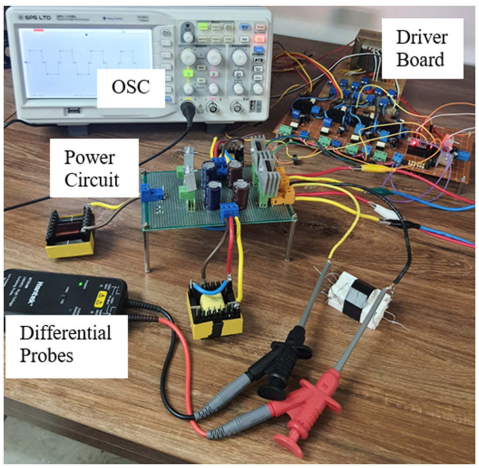

FIGURE 9. Experimental setup.

proper operation. Moreover, these results can validate the obtained results from operational modes' analysis and the other resulting equations. First, it is required to design a prototype of the suggested structure. The equations to design this prototype were obtained in (46)–(53). As these equations indicate, some parameters, such as the D_{ST}, N_{12}, f_s, and R must be given. Thus, these parameters must be supposed to design the experimental prototype. It is required to note that g cannot be measured in practice to use in the prototype design. So the practical topology is assumed to be ideal with a g of zero. As was previously stated, the maximum boost factor can be obtained if both dc voltage sources have equal magnitudes. Thus, the magnitudes of both dc voltage sources are supposed as 20 V. In addition, the magnitude of the desired output voltage is set to 100 V, and N_{12} is assumed as the same as 2. As a result, D_{ST} is equal to 0.2 by taking (56) into account. f_s and R are supposed to equal 100 kHz and 100 Ω, respectively.

By substituting these values in (46)–(49) and having $x_L\%$, $x_{Lm}\%$, $x_{C1}\%$, and $x_{C3}\%$ equal to 8%, 3%, 0.08%, and 0.13%, respectively, the values of required passive devices can be obtained as L, L_m, C_1, and C_3 can be obtained equal to 1 mH, 1.8 mH, 100 μF, and 20 μF, respectively. The required coupled inductors can be designed by having the supposed N_{12} the obtained L_m, and using techniques such as choosing the

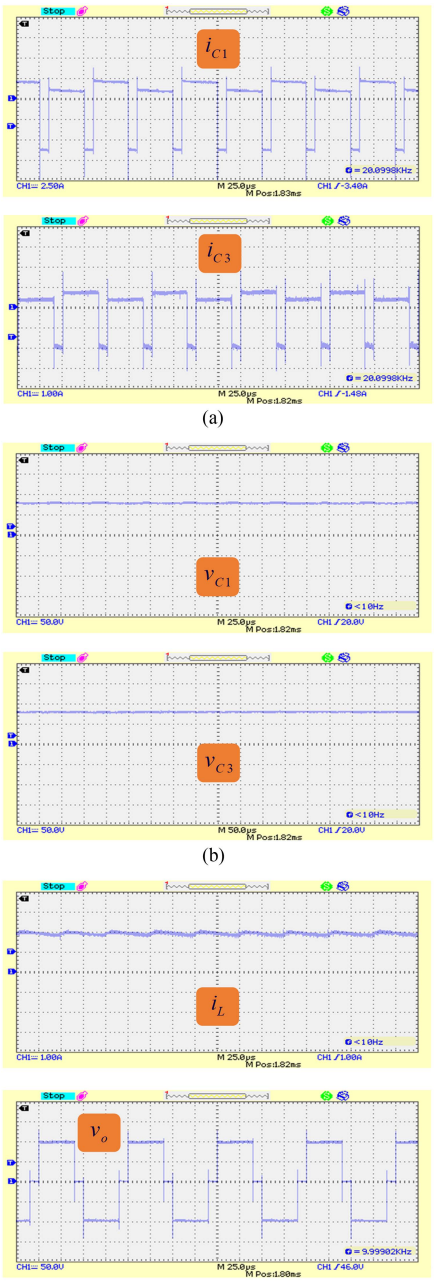

FIGURE 10. Experimental results in steady-state (a) currents passing through capacitors, (b) voltages on capacitors, and (c) passing current through the inductor, and output voltage.

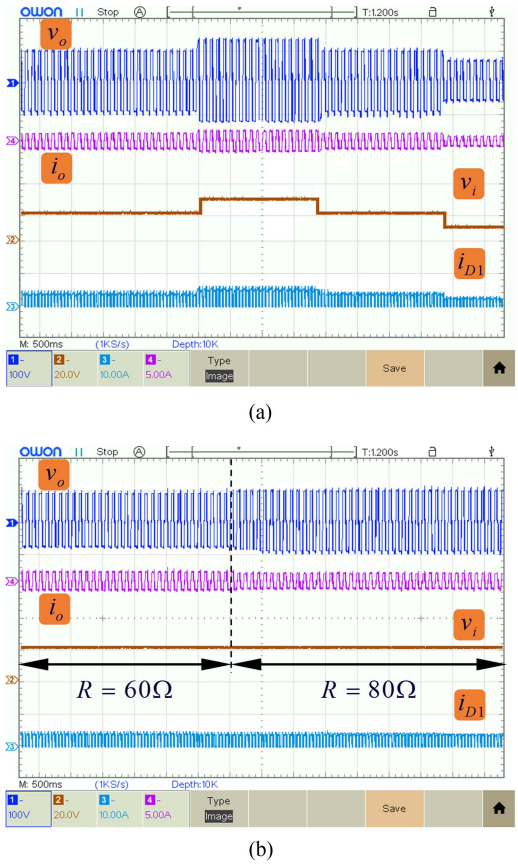

FIGURE 11. Experimental results in steady-state (a) currents passing through capacitors, (b) voltages on capacitors, and (c) passing current through the inductor, and output voltage.

appropriate magnetic core and compressed winding. Moreover, the voltage and current stresses for the switches and diodes are obtained equal to 200 V and 2 A and 300 V and 2.67 A. According to these values, IRFP460 MOSFETs and MUR1560 diodes are used in this experiment. We can bring the experimental prototype by considering the obtained values as shown in Fig. 9. The experimental results are depicted in Fig. 10. The currents and voltages of C_1 and C_3 are shown in Fig. 10(a). Regarding the current waveforms, it can be seen that they follow the same equations obtained from the working modes' analysis. In other words, these equations are valid and can study the currents that pass through the capacitors. Besides, the average voltage on C_1 and C_3 can be read as 40 and 80 V from Fig. 10(b). The same values can be obtained by having (36) and (37), which leads to the verification of these equations. Finally, the current that passes through the inductor L and the output voltage are depicted in Fig. 10(c). From this figure, the results show that the average current that passes through the inductor L is the same as the value obtained from (40), so this equation is received correctly. Moreover, it is seen that the output voltage is a three-level voltage with a maximum magnitude of 100 V, equal to the considered magnitude in the prototype's design. As a result, the correctness of the whole experiment is verified.

In addition to the previous experimental results in which the steady state results for the proposed structure were shown, Fig. 11 shows the study under the transient state where Fig. 11(a) dedicates to showing the changes of output voltage and output current waveforms with regard to the changes of the input voltage. As it is seen in this figure, the higher the input voltage is, the higher output voltage's magnitude will be, which is an apparent outcome of (56). Due to using a resistive load in the output stage, the output voltage waveform will

TABLE 2. Parameters Used in Power Losses Calculation

for Switches	$V_{F,S}=0.7V, R_S=0.5\Omega$ $t_{on}=40ns, t_{off}=60ns$
for Diodes	$V_{F,D}=0.6V, R_D=0.15\Omega$ $t_b=15ns, I_{rr}=20\mu A$
for Coupled Inductors	$R_k=1.4\Omega$ $R_c=69k\Omega, g=0.02$
for Passive Devices	$R_{C1}=0.12\Omega, R_{C3}=0.3\Omega$ $R_L=0.2\Omega$

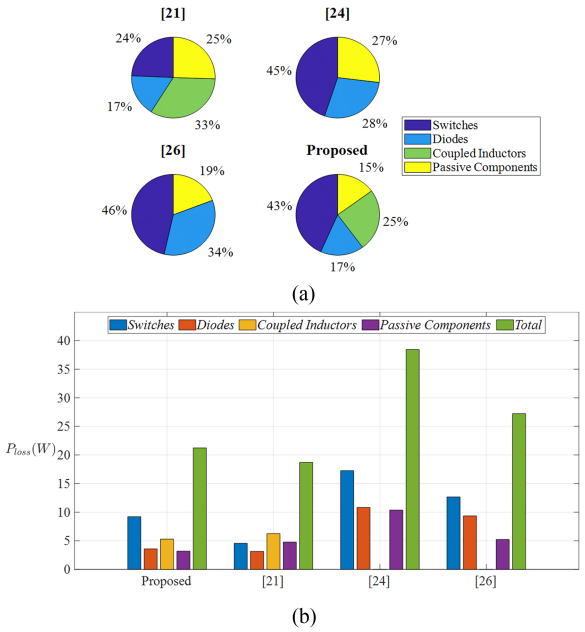

FIGURE 12. Power losses' sharing comparison for output power of 150 W: (a) power losses sharing in percent, and (b) comparison of the different sorts of the power losses (P_{loss}: the power loss in watts).

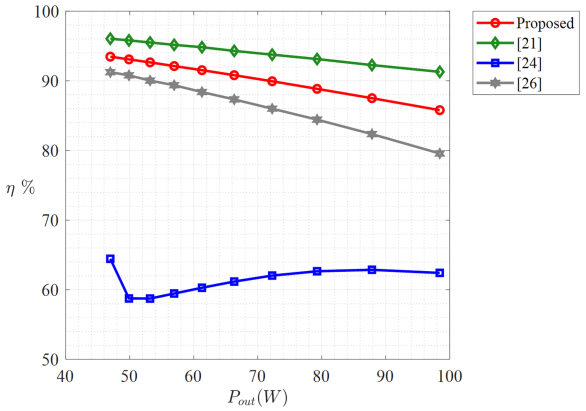

FIGURE 13. Results of comparison from the efficiency perspective *c* (η%: efficiency in percent, P_{out}: the output power in watts).

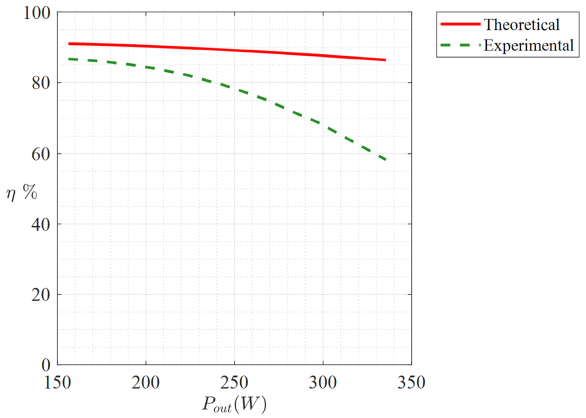

FIGURE 14. Theoretical efficiency in versus with that of experimental (η%: efficiency in percent, P_{out}: the output power in watts).

have the same behavior as that of output voltage. Besides, it is seen that the input current alters according to the differences in the output voltage, which is obvious according to the fact that the input and output currents are related to each other.

Moreover, the changes of these parameters are studied when there is a change in the output load. As Fig. 11(b) illustrates, any changes in the output load will show its result in the output current. Besides, due to the fact that a change in the output current will affect the power losses of the circuit, it can be seen that the output voltage's magnitude will be diminished regardless of (56) which states the constant boost factor without mentioning the output load. To put it differently, an alternation in the output load will directly influence the output voltage's waveform because the lower the output load is, the higher output current's will be resulting in higher output power losses, which will diminish the output voltage's magnitude.

The subsequent study depicted in this section is associated with the power losses and efficiency comparison. The equations to obtain different kinds of power losses in Watts were previously obtained and were listed in Table 1. The parameters listed in Table 2 can be used to be substituted in the equations shown in Table 1 to obtain the amount of power losses consumed by each type of device, including switches, diodes, coupled inductors, and passive devices. By having these power losses, the ratio of each kind of power loss can be obtained in percent. These results are shown in Fig. 12, and by this figure, we can see which devices consume more power losses. Besides, this figure shows the power loss sharing in the other topologies used in the efficiency comparison.

Regarding Fig. 12(a), the higher sharing of power losses is consumed by switches. Besides, the efficiency comparison is depicted in Fig. 13. As this figure shows, the existing structure in [21] has a higher efficiency than the proposed topology. However, the proposed topology has better features than this configuration from other aspects, including boost factor and voltage stresses on components. It is required to note that the efficiency comparison is made between the topologies with two input voltage sources, like the suggested structure.

Besides the comparative study in terms of efficiency and power losses, Fig. 14 shows the comparison between the theoretical and experimental efficiency of the proposed half-bridge-based Z-source inverter. Because of this figure, the

higher output power is, the lower the efficiency will be. The root cause behind this difference is higher output current in higher output powers. Regarding this point, the power losses will be higher in the higher output voltage, leading to a reduction in the efficiency.

VI. CONCLUSION

This article describes a half-bridge-based impedance source inverter with two T-shaped linked inductors with a high boost factor. As a result, there are two switches on it. A suitable modulation method for obtaining gate pulses for both switches was showed. This modulation scheme has shown that the proposed topology includes four operational stages, two of which are ST-type. These operating modes were the boost factor and equations for designing passive devices were then determined using the functional mode analysis equations derived using the voltage- and current-balance laws, respectively. The power loss breakdown study was then evaluated to determine the proposed structure's efficiency. Studied the benefits and drawbacks of the proposed design, the proposed topology was compared with several parameters, including boost factor, total voltage stresses on devices and switches, and the number of required devices. For example, when N_{12} equals 4/3 and D_{ST} equals 0.1, the proposed structure yields a boost factor of 1.5. In the same conditions, the topologies presented in [19] and [21] produce boost factors of 0.75 and 1.33, respectively. Finally, experimental results were obtained by building a prototype with the given equations. These results show that the proposed configuration is capable of valid performance and that all the provided equations are correct. Then, power loss and efficiency analyzes reveal which parts consume the most power, and the proposed topology is sufficiently efficient across a wide range of output powers.

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