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Characterization of GaN HEMTs' Aging Precursors and Activation Energy Under a Wide Range of Thermal Cycling Tests

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ABSTRACT In this article, 650-V/7.5-A-rated enhancement-mode gallium nitride (GaN) high-electron-mobility transistors (HEMTs) with integrated gate drivers are characterized under thousands of accelerated thermal cycling (ATC) at different junction temperature stresses. This research helps in developing fundamental insights into GaN HEMTs' aging characteristics through the degradation of 10 devices under ATC tests. For over 20 000 thermal cycles, the forward and reverse conduction losses, I_{GSS}, C_{oss}, and the RDS_{on} are experimentally measured to identify the parameter shifts and the corresponding precursors. Results indicate that both I_{GSS} and C_{oss} do not deviate much, but the values of RDS_{on}, the forward and reverse conduction losses vary considerably with device aging. This article also presents an empirical method to estimate the correlation between the acceleration factors of the GaN FETs' degradation process and the thermal cycling conditions. The value of the activation energy of the tested GaN HEMT devices is also derived using the empirical equations to be about 1.13 eV under the applied stress factors. This study finds that the degradation process of GaN HEMTs with age facilitates a reasonable correlation with different failure mechanisms, which further helps in reliability improvement.

INDEX TERMS Gallium nitride (GaN) high-electron-mobility-transistors (HEMTs), reliability assessment, online health monitoring, aging precursors, thermal cycling test, activation energy, performance degradation.

I. INTRODUCTION

In modern power applications such as data centers, electrified transportation, renewable energy, fossil energy production, and crypto mining, power electronics are considered as some of the weakest links affecting the overall system reliability and the associated maintenance/repair costs [1], [2], [3]. Gallium nitride (GaN) high-electron-mobility-transistors (HEMTs) are emerging as a promising choice for future power converters. However, it is still necessary to gain further insight into the reliability metrics for GaN HEMTs, including the degradation profile of the devices and the failure mechanisms, considering that there is still not sufficient field data on GaN HEMTs since they have been popularly used in commercial power applications for less than a decade.

Most GaN devices available today are HEMTs, which take advantage of the two-dimensional electron gas (2DEG) layer formed at the heterojunction between GaN and AlGaN layers to achieve faster switching time and lower losses than conventional Silicon (Si) MOSFETs. Surface trapping and deep trapping are the two main trapping phenomena associated with the heterojunction fabrication of GaN FETs [4], [5], [6]. "Surface trapping" refers to the phenomenon where the charges accumulate near the drain edge of the gate terminal once the device is turned OFF. Thus, the trap captures the "hot electron" as it crosses the AlGaN barrier. These trapped charges act as a "virtual gate" once the device is turned ON (or semi-ON), weakening the 2DEG until they are released, resulting in dynamic RDS_{on} characteristics. Due to carbon

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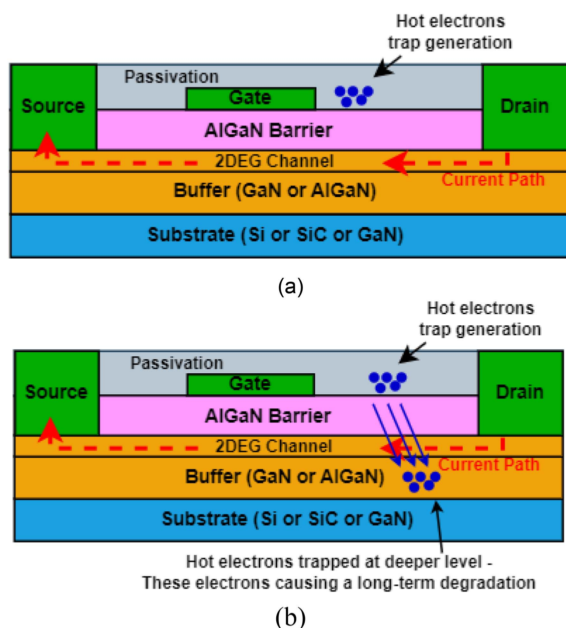


FIGURE 1. GaN HEMTs layout. (a) During the OFF state, charges on the surface are trapped near the drain edge of the gate terminal. (b) During the next ON-state, hot electrons cross the AlGaN barrier to a deeper level causing long-term degradation in the device performance.

doping in the buffer layer, deep traps are formed, which capture "hot electrons." These trapped charges cause long-term degradation of the device and weaken the 2DEG. Surface trapping occurs when the device turns OFF [see Fig. 1(a)]; deep trapping occurs when it turns ON [see Fig. 1(b)].

The degradation of RDS_{on} has been attributed to hot-electronic trapping in the GaN buffer layers during the transition from ON to OFF states and detrapping during the transition from OFF to ON states [7], [8], [9], [10]. During the hot electron trapping process, charge carriers are reduced in the GaN channel, leading to a collapse of the drain current (I_D) collapse in RDS_{on}. Detailed studies on the trapping and detrapping processes were presented in [11]. A high drain–source voltage (V_{DS}) in the OFF state may result in electrons being trapped under the gate and the gate–drain region, resulting in a reduction in the transconductance (g_m) of the device [8]. The junction temperature, electric field, and drain bias contribute to a shift in the gate–source threshold voltage and an increase in the gate leakage current [12]. The forward and reverse conduction modes of GaN HEMTs have been examined in [13], [14], and [15]. In terms of failure modes, GaN HEMTs do not differ significantly in either operation mode. Accelerated power cycling of GaN HEMTs has revealed possible gate degradation with device aging [16]. Several studies have reported only a negligible increase in gate–source leakage currents of GaN HEMTs as they age [13], [14], [15], [16], [18]. The gate aging can be attributed to the defect/leakage paths in the p-type (AlGaN buffer) gate interface caused by the hot electrons.

Several studies have shown that GaN HEMTs operate reliably under junction temperatures of about 150 °C (and no other stress factors), although RDS_{on} slightly increases because of the trapping of hot electrons [19], [20], [21], [22]. Gate degradation in GaN HEMTs results from electrons that accumulate on the surface of the semiconductor due to traps (which can be generated during the OFF-state stress voltage [23]) or defect formation in the gate region. Electrons create an electrostatic charge that partially depletes the conducting channel, reducing gate channel current [24], [25]. A few studies examining the degradation parameters and indicators of GaN HEMTs can be found in [26], [27], [28], and [29].

There is, however, a lack of comprehensive characterization and analysis of the changes in the static electrical parameters of GaN HEMTs over a wide range of thermal cycling throughout the aging process. Accelerated thermal cycling (ATC) can contribute to mechanical stress between the GaN HEMTs' layers due to the differential thermal expansion coefficients of the various materials, as reported in [30], [31], [32], [33], and [34]. In this research, multiple thermal cycling windows are used, which provide a better insight into the devices' degradation performance with aging and their associated explanations. Furthermore, an empirical method is proposed to estimate the correlation between the acceleration factors of the GaN FETs' degradation process and the thermal cycling conditions. The value of the activation energy (E_a) of the tested GaN HEMT devices is also derived using empirical equations and validated through multiple case scenarios. The experimental evaluation of GaN HEMTs' degradation performance over time and the resulting research findings can lead to the development of effective methods for improving the reliability of the devices over their mission profile.

The main contributions of this article are as follows.

1) Test setup and methods that enable continual measurements of key aging parameters of GaN HEMTs under a wide range of thermal cycling (25–200 °C) for reliability characterization.
2) Establishing the relationship between the GaN HEMTs' aging parameters and their degradation patterns, including their underlying mechanisms.
3) Providing an empirical approach for determining the activation energy of the tested GaN HEMTs via the analysis of acceleration factors under thermal cycling.

II. CHARACTERISTICS OF THE ENHANCEMENT-MODE GAN HEMTS UNDER TEST

Out of the prominent characteristic parameters of semiconductor switching devices, such as ON-state resistance (RDS_{on}), transconductance (g_m), gate leakage current (I_{GSS}), drain–source leakage current (I_{DSS}), and gate–source threshold voltage (V_{GSth}), not all of them can be considered as health (or aging) indicators. However, it is important to identify the critical aging parameters for a particular type of semiconductor device to assess the reliability and predict the health in real time. A summary of the main parameters of the investigated enhancement-mode GaN HEMT devices is presented in Table 1. A Keysight curve tracer B1506A is used to characterize the GaN devices at room temperature (25 °C) before placing

TABLE 1. GaN HEMTs Datasheet Ratings [35]

Parameter	Value	Parameter	Value
V_{DS} (max)	650 V	Thermal resistance (junction to case)	2 °C/W
I_D (continuous at 100 °C)	7.5 A	Reverse conduction voltage at I_{SD} = 6 A	4 V
RDS_{on}	180 mΩ	Switching rising/falling time at 400 V V_{DS}, 4 A I_D, T_j = 150 °C	12/7 ns
Output charge (Q_{oss}) at V_{DS} = 400 V	16 nC	Integrated gate driver	Yes

them in the degradation test setup. The static characteristics of a new (or fresh) device are presented in Fig. 2. The characteristics match well with the datasheet specifications, except for the additional nanoparasitic inductance and microconnection/soldering resistance contributed by the test bench. The reverse conduction loss in Fig. 2(a) is almost the same as the forward loss characteristics because both are measured at gate–source voltage (V_{GS}) of 5 V and have the current passing through the 2DEG channel. However, it is different when the reverse operation mode is conducted at V_{GS} of 0 V. Since a GaN HEMT's "virtual body diode" is formed by turning ON the 2DEG in the opposite direction at 0 V V_{GS}, there is a reverse voltage drop (a few volts) depending on the drain current and the device temperature. Therefore, the difference between both losses is determined by the voltage drop in reverse operation. Fig. 2(b) shows the gate–source leakage current, measured at 0 V and 1 V of V_{GS}. The RDS_{on} curve is presented in Fig. 2(c), and the C_{oss} in Fig. 2(d) is measured at a frequency of 100 kHz. For this study, the output capacitance measurement is conducted to determine whether 2DEG depletion has occurred near the surface. That is possible because the capacitance drops with increasing V_{DS} due to the depletion of the free electrons in the GaN layer. The following section describes the degradation process and further characterization under ATC tests.

III. GAN HEMT DEGRADATION TESTING SETUP

The schematic of the test circuit for V_{DSon} measurement is shown in Fig. 3(a) and is the same circuit demonstrated in [36] and referenced in JEDEC JEP173 [37]. The degradation setup shown in Fig. 3(c) was developed so that multiple GaN FETs could be thermally cycled sequentially, Fig. 3(d) is the power devices curve tracer, and Fig. 3(e) is GaN FET boards. Table 2 summarizes the specifications of the GaN devices examined. Fig. 3(b) illustrates how the device under test (DUT) is turned OFF when the junction temperature reaches the maximum set value, followed by heating the next device while the other devices remain OFF, and so on. Consequently, this sequential thermal cycling can significantly reduce the degradation time for multiple devices within the same system.

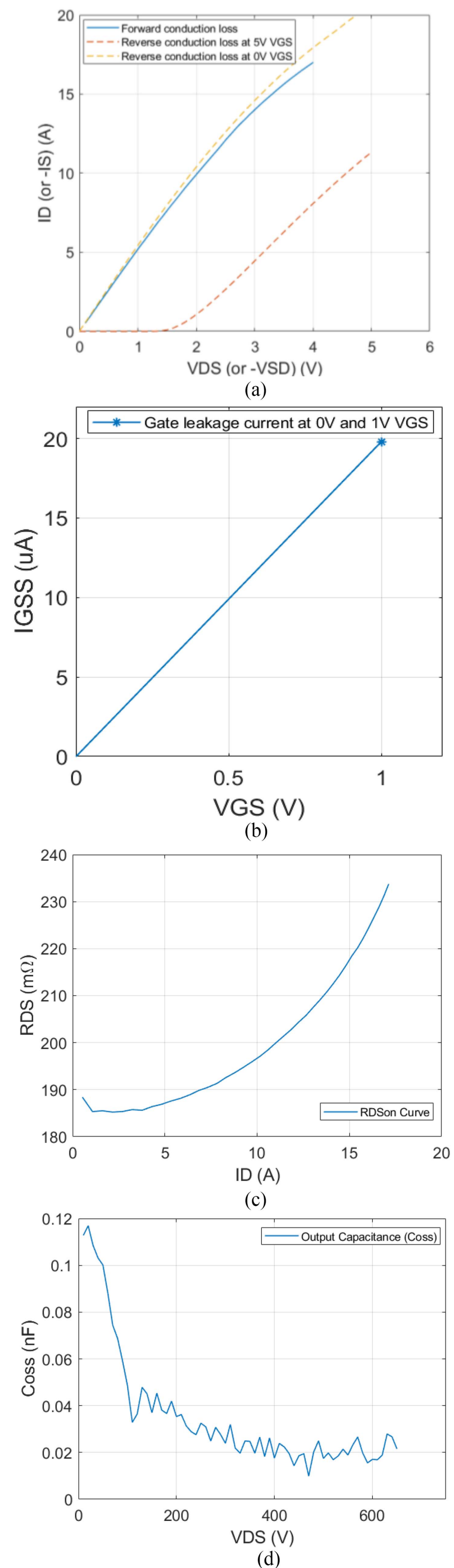
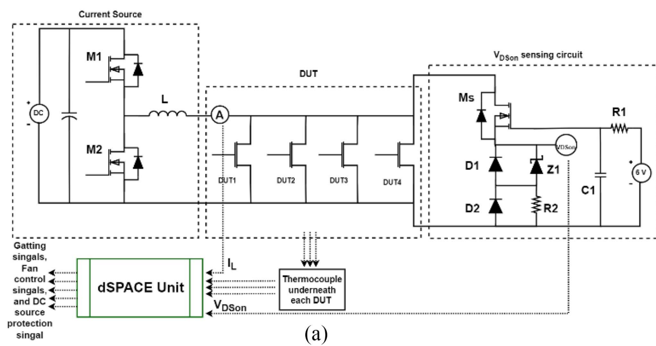
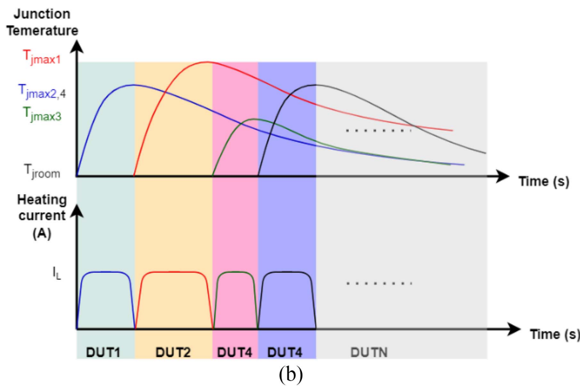


FIGURE 2. Characteristics of a fresh GaN HEMT device-1 captured at room temperature (25 °C). (a) Forward and reverse conduction (at 5 V V_{GS}) losses. (b) Gate–source leakage current. (c) RDS_{on}. (d) Output capacitance measured at 100 kHz.



(a)



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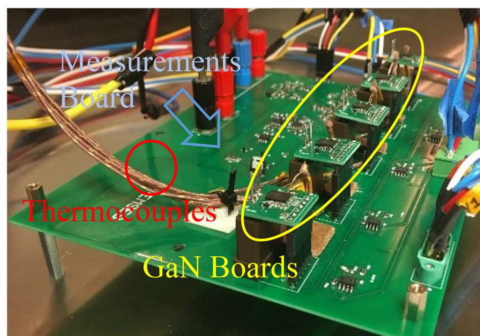

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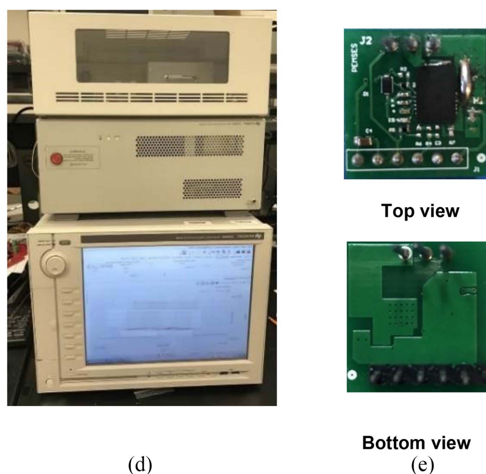

(d) (e)

FIGURE 3. Degradation testing setup. (a) Thermal cycling pattern for multiple devices under test. (b) Circuit schematic. (c) Experimental hardware setup used for characterization. (d) B1506A curve tracer. (e) Top and bottom view of the GaN board.

TABLE 2. Specifications of the Degradation Test Setup

Parameter	Value	Parameter	Value
DSpace sampling time	20 µs	Cooling method	Controlled fan per each DUT
Heating current (DC)	2–3 A	Current source	Synchronous Buck converter
Room/limit temperature	25/125–200 °C	Number of devices under test	10
Heating current rising/falling time	2 µs		

Compared to fast heating times enabled by passing currents through the DUT, GaN FETs cooling takes much longer to reach room temperature (3–4 times as long as the heating time). Using a fan setup, forced air cooling reduces the device's temperature more quickly below a specific threshold.

Based on the physics of the failure approach, an increase in junction temperature (T_j) will also reduce the lifetime of a semiconductor component [38]. Therefore, ATC is a commonly used reliability assessment method for power semiconductor switching devices [39], [40], [41]. ATC exposes the semiconductor devices to a sequence of above- and below-room temperatures for thousands of cycles—this test further sheds light on their intrinsic degradation mechanisms as well as their accelerated aging due to the mechanical stresses induced on the devices by the fast thermal cycling.

To avoid failure due to thermal runaway, monitoring the device junction temperature throughout the ATC test is imperative. In contrast to Silicon Carbide (SiC) FETs, GaN devices have relatively lower thermal conductivity, making heat management challenging during ATC. For GaN FETs, RDS_{on} increases by over twice when the T_j temperature varies between 25 °C and 150 °C compared to SiC [42] and Si MOSFETs [43]. A commercial temperature sensor, such as a thermocouple or a thermistor, has several milliseconds of time delay. That makes these sensors unsuitable for in-situ monitoring of GaN devices and rapid thermal cycling.

In order to estimate the junction temperature of GaN FETs under ATC, the RDS_{on} of the DUT is calculated for each thermal cycle. The relationship between GaN HEMT ON-state resistance and T_j was derived by soaking the GaN FETs in a thermal chamber for around 30 min before measuring the RDS_{on}. According to the pre-experimental analysis of the RDS_{on} with junction temperature shown in Fig. 4, RDS_{on} limits are used to estimate the device's stress junction temperature limit. Hence, the DUTs junction temperature range is determined based on the ON-state resistance values during the degradation/reliability setup. Detailed information on the RDS_{on} limits and junction temperature estimation technique was provided in [36]. Different RDS_{on} limits and their corresponding temperatures are tabulated in Table 3 (derived from Fig. 4).

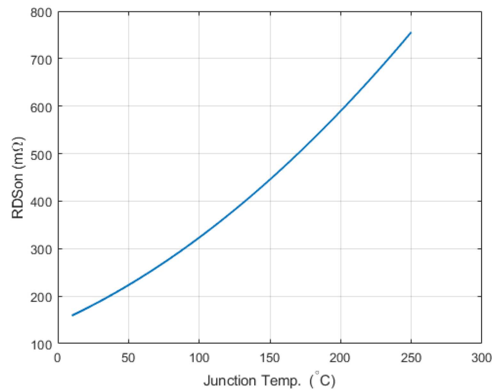

FIGURE 4. Experimentally extracted the relationship between the RDS_{on} and junction temperature of GaN HEMTs.

TABLE 3. Extracted RDS_{on} Limits Used for GaN HEMTs' Junction Temperature Estimation

RDS_{on} Limit (mΩ)	Estimated T_j (°C)
180	25
450	150
500	170
550	185
600	200

When using dc current, once the device junction heats to a specified maximum temperature (T_j limit or T_{jmax}), it is turned OFF so that the junction can get back to the minimum temperature (e.g., room temperature), which is marked as the end of the cycle. Every 1000 thermal cycles, GaN device boards [shown in Fig. 3(e)] are characterized using the B1506A curve tracer to verify the aging precursors. For up to 24 h, the devices are left idle (turned OFF) before characterization to ensure no hot electrons are trapped near the surface. The GaN FET boards are then connected to the curve tracer for characterization.

A flowchart showing the automated control flow for the degradation of ten GaN HEMTs is given in Fig. 5, which is implemented in DSpace MicrolabBox (1202). Different thermal cycling windows are assigned to each group of devices ranging from room temperature to the thermal limit listed in Table 3 to investigate other degradation profiles. The DUTs are heated using dc current within the 2–3 A range. Calculations of the RDS_{on} are based on the division of V_{DSon} and I_D, after which the junction temperature value is deduced. As soon as the junction temperature reaches the maximum set point, the DUT is turned OFF, and its forced air-cooling fan is turned ON to bring the junction temperature down to room temperature. During the cooling time of the first DUT, the next GaN FET is turned ON to begin its thermal cycle. By sequentially repeating thermal cycles, multiple devices' degradation process becomes interleaved and, hence, faster. The control algorithm also includes forced shutdowns and other automated

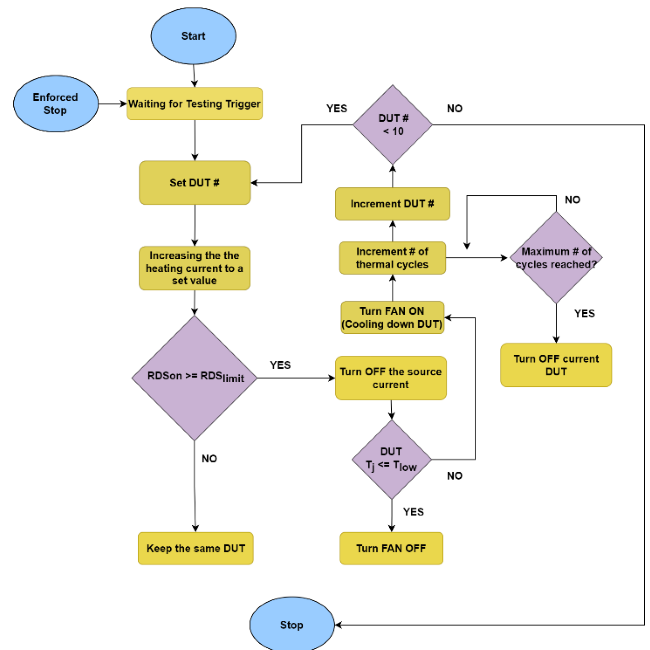

FIGURE 5. Flowchart for GaN FETs degradation process.

safety functions to stop the test in case of an error. GaN boards are designed to be plugged into a reliability test setup or a curve tracer to characterize the devices' every defined number of thermal cycles. The following section presents the experimental validation of the degradation system.

IV. EXPERIMENTAL RESULTS AND DISCUSSIONS

For this research, 10 GaN FETs are investigated at different RDS_{on} limits (or T_j limits) under ATC tests for about 20k cycles. Four selected devices are characterized at different junction temperature limits. The following are the junction temperature stress ranges for each DUT:

1) Device-1: 25–150 °C;
2) Device-2: 25–170 °C;
3) Device-3: 25–185 °C;
4) Device-4: 25–200 °C.

The characteristics of the selected devices are shown in Figs. 6–8. As the devices age through thermal cycling, their forward conduction loss increases, as shown in Figs. 6–8(a). Gate-to-source leakage current is measured at gate–source voltages of 0 and 1 V, as illustrated in Figs. 6–8(c). Despite device aging, I_{GSS} does not change significantly. That is because there is no significant trapping/detrapping of charge carriers under ATC testing, leading to almost no high leakage current. It is, therefore, not an ideal parameter for evaluating the health of GaN HEMTs. The parasitic output capacitance of GaN devices does not change much during degradation either, as shown in Figs. 6–8(b). That means there is no significant 2DEG depletion near the surface. Reverse conduction characteristics are observed at 0 V and 5 V gate-to-source voltages, as shown in Figs. 6–8. Under a reversed drain-to-source voltage and 0 V V_{GS}, the GaN HEMTs will conduct

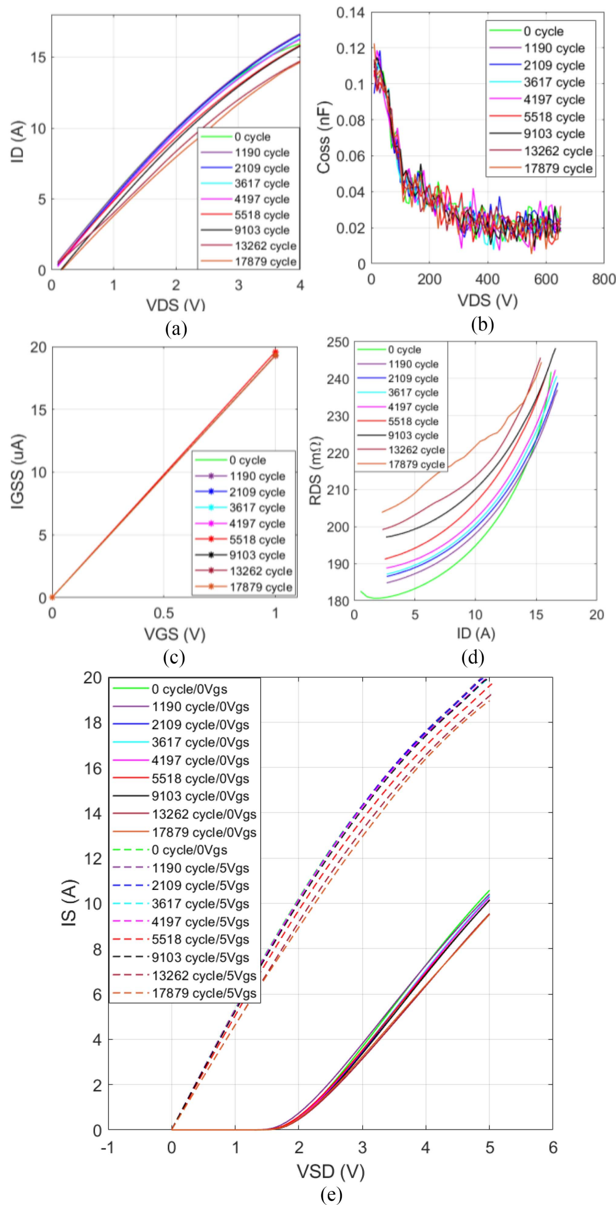

FIGURE 6. Characteristics of GaN HEMT device-1 captured after different thermal cycles at room temperature (25 °C), with the testing range of junction thermal cycling from 25 to 150 °C. (a) Drain–source voltage versus drain current. (b) RDS$_{on}$ versus drain current. (c) Gate leakage current versus gate–source voltage. (d) Drain leakage current versus constant drain–source voltage at zero gate–source voltage. (e) Source–drain voltage versus source current (reverse conduction).

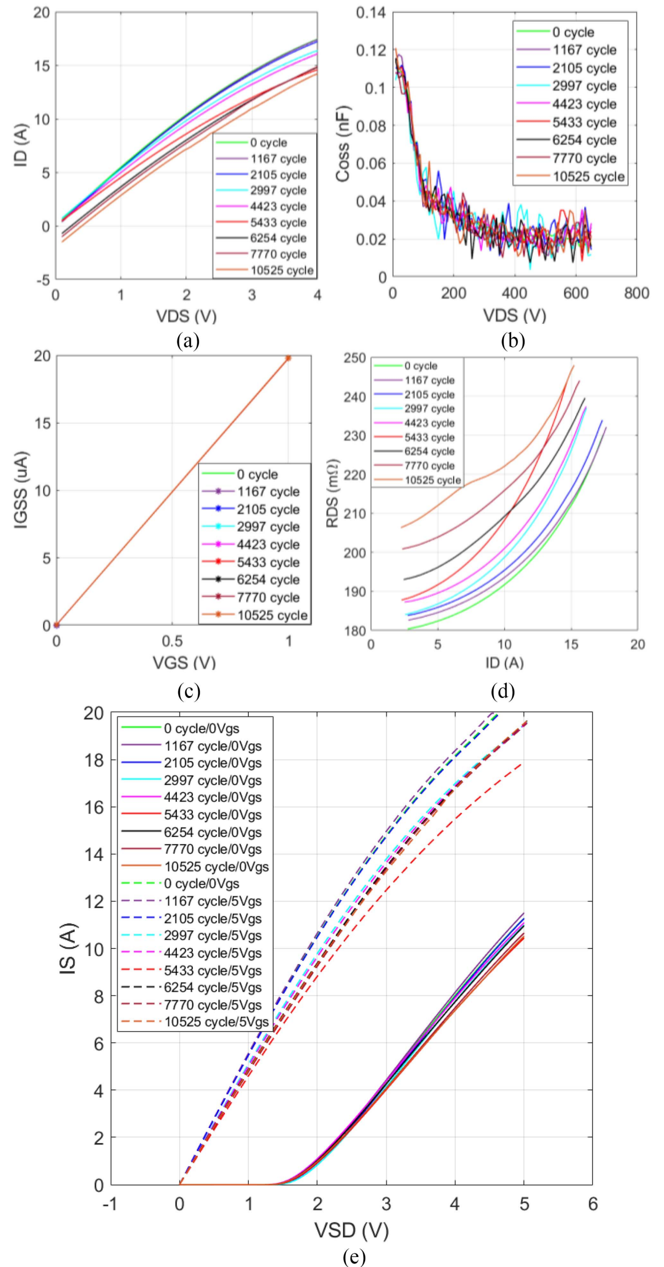

FIGURE 7. Characteristics of GaN HEMT device-2 captured after different thermal cycles at room temperature (25 °C), with the testing range of junction thermal cycling from 25 to 170 °C. (a) Drain–source voltage versus drain current. (b) RDS$_{on}$ versus drain current. (c) Gate leakage current versus gate–source voltage. (d) Drain leakage current versus constant drain–source voltage at zero gate–source voltage. (e) Source–drain voltage versus source current (reverse conduction).

as a result of a positive V_{GD} bias. During reverse conduction, the characteristics are identical to those of diodes. Compared to conventional Si MOSFETs, GaN HEMTs can have higher reverse conduction losses when switched ON with 5 V V_{GS} [5]. The RDS$_{on}$ in GaN HEMTs comprises the channel resistance originating from the 2DEGs beneath the gate, the drain and source access regions, and the gate–source and gate–drain resistances [44], [45]. The decline in 2DEG mobility results in an increase in the device's RDS$_{on}$.

Devices subjected to higher junction temperature limits (see Fig. 8) age faster when compared to those subjected to lower junction temperature limits (see Fig. 6). The RDS$_{on}$ curves in Figs. 6–8(c) demonstrate a gradual increase with thermal cycling (or aging) when considering the junction thermal cycling swing levels assigned to each GaN FET DUT. For example, since Device-4 is tested to a higher junction thermal limit than Device-1, the RDS$_{on}$ of Device-4 increases at a faster pace. It

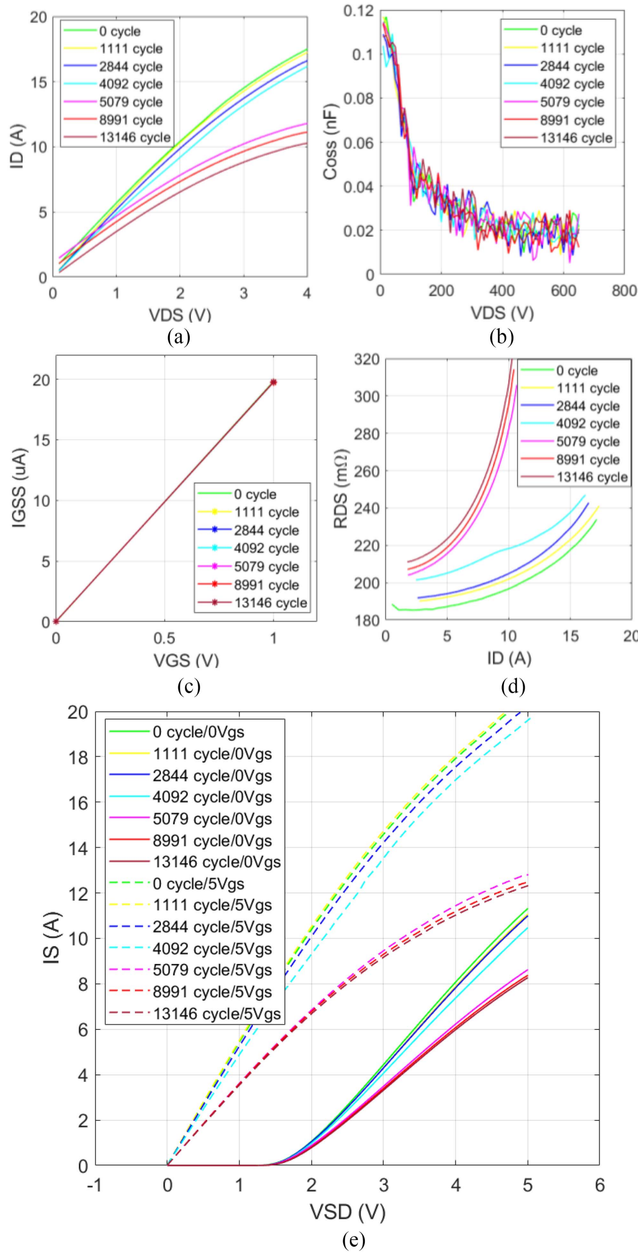

FIGURE 8. **Characteristics of GaN HEMT device-4 captured after different thermal cycles at room temperature (25 °C), with the testing range of junction thermal cycling from 25 to 200 °C. (a) Drain–source voltage versus drain current. (b) RDS_{on} versus drain current. (c) Gate leakage current versus gate–source voltage. (d) Drain leakage current versus constant drain–source voltage at zero gate–source voltage. (e) Source–drain voltage versus source current (reverse conduction).**

TABLE 4. **Summary of GaN HEMTs Aging Parameters Under ATCs**

T_j limit (°C)	Number of thermal cycles (k)	Change in RDS_{on} (%)	Forward conduction loss (w) at I_D = 5 A	Reverse condition loss (w) at I_S = 5 A and 0V V_{GS}	I_{GSS} (uA) at 1V V_{GS}	C_{OSS} (pF) at V_{DS} = 650 V and f = 100 kHz
150	0	0	4.5	4.7	19.4	20
	3	2.6	4.7	4.8	19.5	20
	6	7	4.8	5	19.5	20
	9	10	5	5.1	20	20
170	0	0	4.5	4.6	19.5	20
	3	2.8	4.63	4.75	19.5	20
	6	7.7	4.85	4.8	19.6	20
	9	14	5.13	5.2	20.2	20
185	0	0	4.5	4.6	19.3	20
	3	3.4	4.7	4.8	19.5	20
	6	8.3	4.9	5	19.6	20
	9	16	5.22	5.3	20.4	20
200	0	0	4.5	4.5	19.5	20
	3	6.6	4.8	4.9	19.7	20
	6	12.2	5.049	5.1	19.8	20
	9	17.8	5.3	5.4	20.7	20

may be noted that since the trends of the characteristics were consistent for Device-2 and Device-3, the corresponding plots of Device-3 are not shown in the article. However, a summary of the aging parameters for all the devices is presented in Table 4. The experimental results indicate that RDS_{on} is a reliable indicator for monitoring the health status and predicting the reliability of GaN HEMTs. RDS_{on} monitoring can be effectively employed in practical applications. As the device ages, other electrical parameters become increasingly vulnerable to accuracy issues. The health status of GaN FETs is heavily dependent on variations in junction temperature.

Therefore, accurate and fast junction temperature sensing circuits are critical for proper aging assessment. Conventional temperature sensors typically have slow response times (a few to several milliseconds); hence, indirect T_j measurements will be a better alternative solution as long as RDS_{on} can be measured precisely.

The research findings show that the time required to heat a GaN device to a specific RDS_{on} limit decreases with age, making it a useful condition monitoring method for GaN FETs. For example, Fig. 9 shows the experimental waveforms from multiple thermal cycles for a fresh GaN HEMT tested with 360 thermal cycles (ATC) from 25 to 180 °C. The estimated junction temperature is based on the RDS_{on} limit concept. However, for benchmarking the available temperature sensor, a thermocouple is inserted beneath the device to measure its steady-state temperature, as the measurement is depicted in Fig. 9. After 21 300 thermal cycles, the RDS_{on} is captured, as shown in Fig. 10. The RDS_{on} curves in Figs. 9 and 10 reveal that after 21 300 thermal cycles, the initial RDS_{on} value (around 190 mΩ for a new device at room temperature) increases to 300 mΩ and reaches its limit after only 1.2 s, compared to 12 s at 360 thermal cycles. It indicates that the slope of RDS_{on} increases with the device's age, further

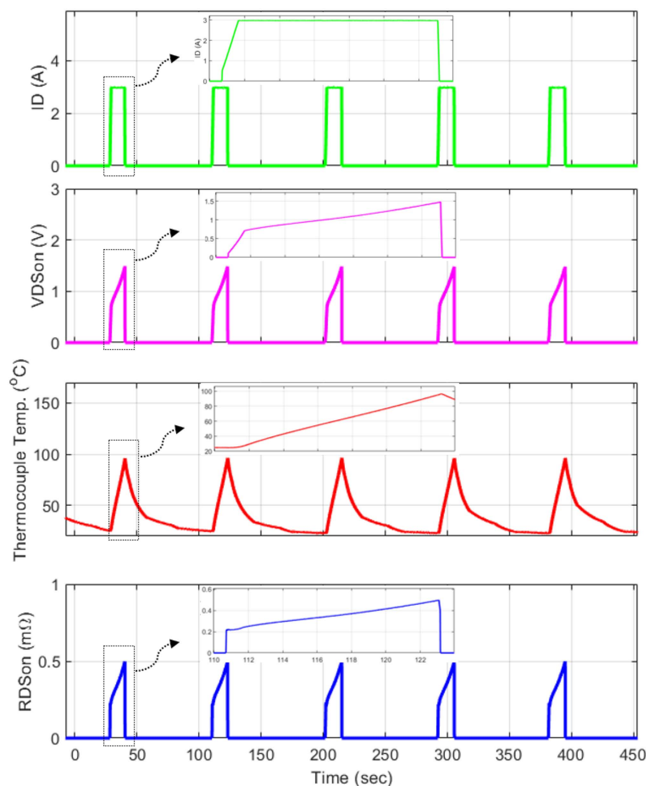

FIGURE 9. Experimental measurements of a fresh DUT under ATC (started with thermal cycle number 360) for GaN HEMT with a junction temperature swing window of 25–180 °C.

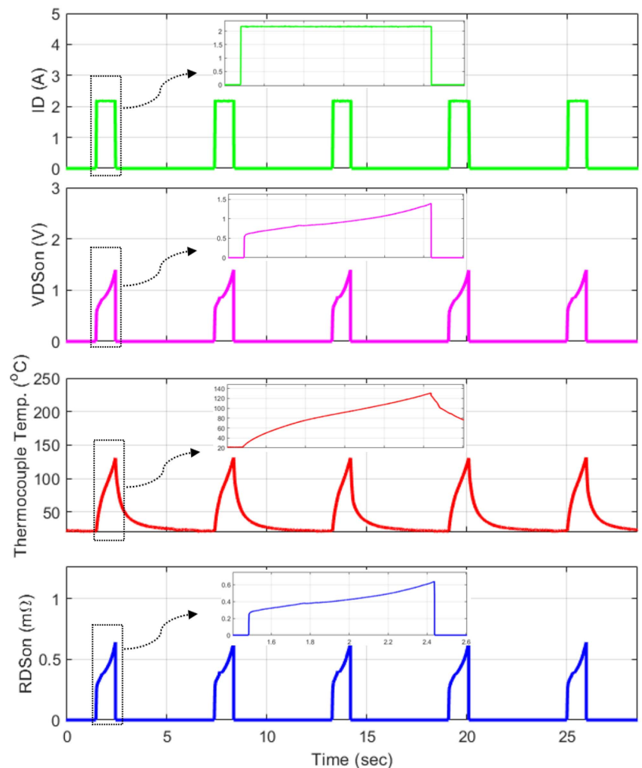

FIGURE 10. Experimental DUT measurements of aging under ATC (started with thermal cycle number 21 300) for GaN HEMT with a junction temperature swing window of 25–180 °C.

reinforcing RDS_{on} as a promising alternative for detecting junction temperature in GaN FETs.

In addition, the slope of RDS_{on} (or the rate of change in RDS_{on} over time) can also provide accurate monitoring of aging and estimation of device lifetime. As demonstrated in Figs. 9 and 10 (fresh and aging devices), a reduction in heating current from 3 to 2.25 A becomes necessary to control the rise in RDS_{on}. Despite the decreased heating current, the RDS_{on} limit (or junction temperature limit) is reached >10 times faster in the aging device compared to a new (fresh) device. Table 4 presents the shifts in GaN HEMT aging parameters under ATC. The findings show that the I_{GSS} and C_{oss} of all 10 devices investigated in the study do not change significantly over time.

That is because the ATC only applies thermal stress to the junction channel, not the gate–source channel, and does not contribute to AIGaN buffer trapping. However, it does lead to a reduction in 2DEG layer density and mobility. This results in the RDS_{on} curves increasing (or shifting upward) with aging time. Another potential cause for the performance degradation of the GaN devices under ATC is the formation of depth cracks at the junction of AlGaN and GaN due to differences in the thermal expansion coefficients of the materials. The resulting mechanical degradation also further impacts the aging pattern and the RDS_{on} value. During the ON state, more electrons are trapped in these cracks, leading to an increase in RDS_{on}. Based on the findings of this research and the proposed testing methodology, the degradation parameters of the GaN devices, their trends, and aging mechanisms are summarized in Table 5. The potential challenges that may be faced in performing the associated parameters' online (real-time) monitoring are also listed.

V. ACCELERATION FACTORS AND ACTIVATION ENERGY OF GAN HEMTS UNDER ATC

The activation energy of a reaction has been traditionally determined through the use of Arrhenius (1), which links the temperature dependence of the reaction rate constant to the activation energy [46]

$$K = A \times e^{-\left(\frac{E_a}{R}\right)\times\left(\frac{1}{T}\right)} \tag{1}$$

where K is the rate constant, A is the frequency factor, E_a is the activation energy, R is the Boltzmann constant (8.63 × 10^{-5} eV/K), and T is the absolute temperature in Kelvin (°C+273).

The junction temperatures of the DUTs in the considered ATC tests cycle between a minimum threshold (25 °C) and a maximum limit temperature (T_{jmax}). The temperature-dependent RDS_{on}, already identified as a reliable parameter for estimating the devices' aging, is used to evaluate the rate constant for calculating the activation energy of the GaN HEMTs under thermal cycling conditions. The following method empirically estimates the correlation between the

TABLE 5. Aging of Parameters, Mechanisms, and Indicators During ATC

Parameter	Indicator's trend	Degradation mechanism(s)	Online monitoring challenge(s)
RDS_{on}	Increase	Mobility reduction in the 2DEG channel due to the channel thermal stress	Introducing interference ringing/oscillation with the device voltage and current measurements
Forward conduction loss	Increase	RDS_{on} increases	Similar to the RDS_{on} measurements
Reverse conduction loss at 0 V V_{GS}	Increase	RDS_{on} increases	Similar to the RDS_{on} measurements
Gate–source leakage current	No significant change	Possibly a light gate degradation caused by the heat dissipated through the die from the drain–source channel	Not a reliable parameter for online monitoring under thermal considerations
Output capacitance	No significant change	No significant trapping near the surface under the ATC test	Not a reliable parameter for online monitoring under thermal considerations

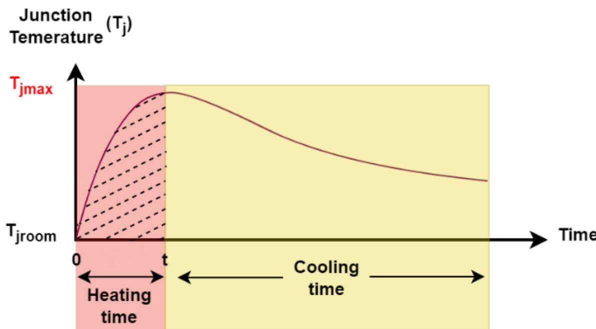

FIGURE 11. Complete thermal cycle caused by a dc heating current.

acceleration factors of the GaN FETs' degradation process and the thermal cycling conditions. The value of the activation energy (E_a) of the tested GaN HEMT devices is also derived accordingly.

1) GaN FETs (designated as device-1) undergo thermal cycling between a minimum temperature of 25 °C (room temperature) to a maximum temperature of 150 °C. The activation energy for this device is calculated using the Arrhenius equation as in

$$K_1 = A \times e^{-\left(\frac{E_a}{R}\right)\times\left(\frac{1}{T_1}\right)} \tag{2}$$

where K_1 represents the degradation time taken for the RDS_{on} to change from 200 (for relatively fresh devices) to 250 mΩ (for reasonably degraded devices), as shown in Fig. 12. T_1 refers to the average value of the junction temperature during the heating time (t_1) of device-1 (as shown using dashed lines in Fig. 11) in the ATC curve, which is during the time for the junction temperature to rise from the minimum to maximum set values as a result of the application of the dc current.

Thus, T_1 can be mathematically calculated by

$$T_1 = \frac{1}{t_1} \cdot \int_0^{t_1} T_j(t)\ dt. \tag{3}$$

2) The Arrhenius equation is also applied to GaN FETs (referred to as device-2 in the study) undergoing thermal cycling between 25 °C (room temperature) and 170 °C (maximum temperature) as in

$$K_2 = A \times e^{-\left(\frac{E_a}{R}\right)\times\left(\frac{1}{T_2}\right)} \tag{4}$$

where K_2 represents the degradation time required for the RDS_{on} of device-2 to change from its original value of 200 to 250 mΩ during the degradation process. T_2 refers to the thermal area (as shown using dashed lines in Fig. 11) in the ATC curve of device-2, which is during the time for the junction temperature to rise from the minimum to maximum set values as a result of the dc current. By dividing (2) by (4), the acceleration factor can be calculated as in

$$\frac{K_1}{K_2} = e^{-\left(\frac{E_a}{R}\right)\times\left(\frac{1}{T_1} - \frac{1}{T_2}\right)} \tag{5}$$

where $\frac{K_1}{K_2}$ is the acceleration factor (AF) for the GaN HEMTs under the abovementioned thermal cycling tests.

3) In accordance with the findings in [47], Fig. 12 presents the RDS_{on} curves against the degradation time of GaN HEMTs under various thermal cycling profiles.

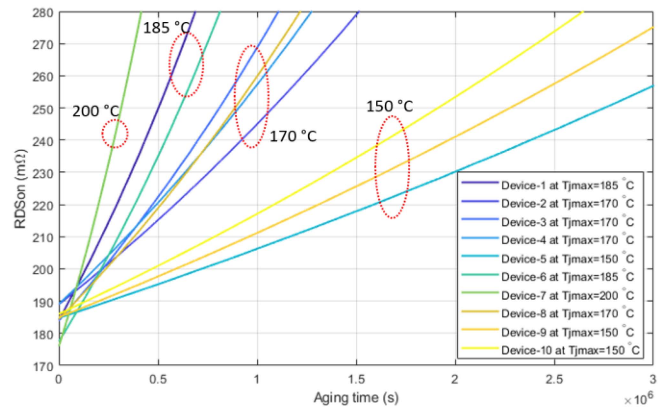

FIGURE 12. Experimental RDS_{on} with aging time at different stress temperatures fitted with an exponential curve function.

For this proposed study, all RDS_{on} values are recorded at room temperature (25 °C) for consistency. The mean RDS_{on} values based on the curve-fitted datasets of multiple devices undergoing the same ATC profile (say, 25–150 °C) are considered for calculating the activation energy, as illustrated by the clusters in Fig. 12. The following is a detailed example of activation energy calculations from these experimental datasets. Please note the time taken for the RDS_{on} of each device to change from 200 to 250 mΩ.

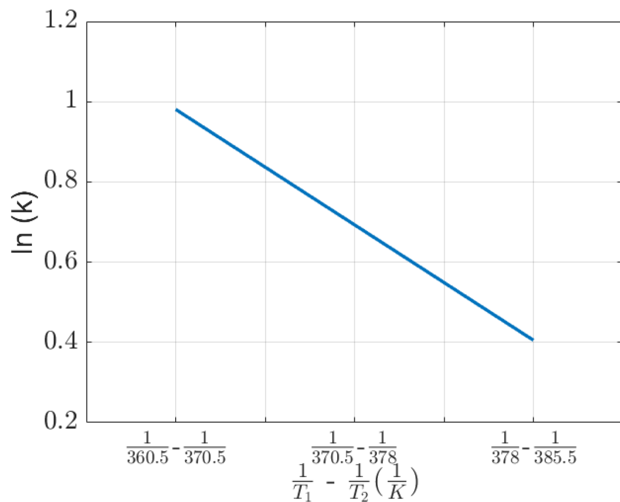

FIGURE 13. Arrhenius equation's slope based on experimental curve fitted RDS_{on} datasets under the thermal cycling tests.

Case 1:
For the devices undergoing ATC from 25 to 150 °C

$$K_1 = 1.6 \times 10^6\ s.$$

For the devices undergoing ATC from 25 to 170 °C

$$K_2 = 0.6 \times 10^6\ s.$$

Case 2:
For the devices undergoing ATC from 25 to 170 °C

$$K_1 = 0.6 \times 10^6\ s.$$

For the devices undergoing ATC from 25 to 185 °C

$$K_2 = 0.3 \times 10^6\ s.$$

Rearranging and taking the natural log of the Arrhenius equation brings a linear relation, which can then be put into a "straight-line" format as in the following equations:

$$\ln\left(\frac{K_1}{K_2}\right) = -\left(\frac{E_a}{R}\right) \times \left(\frac{1}{T_1} - \frac{1}{T_2}\right) \tag{6}$$

$$y = mx + b. \tag{7}$$

When ln *(k)* (log of the rate constant) is plotted versus the difference between the inverse of the temperature values (Kelvin), the slope represents that of the Arrhenius equation, where the activation can be determined as in

$$E_a = \frac{\ln\left(\frac{K_1}{K_2}\right)}{\left(\frac{1}{T_1} - \frac{1}{T_2}\right)} \times R = Slope \times R. \tag{8}$$

The slope of the Arrhenius equation, shown in Fig. 13, is plotted based on the case studies illustrated in Table 6.

From Fig. 13, it can be observed that the activation energy for the devices is constant regardless of the changes in the thermal cycling window (T_{jroom} and T_{jmax}). These calculations are validated by comparing the ratio of the acceleration factors (AFs) and the temperature terms in both case 1 and case 2 (presented in Table 6) as in

TABLE 6. Summary of Calculations for GaN HEMTs Activation Energy Under Different Thermal Cycling Windows

Case study	Thermal cycling window	Acceleration factor (k) = $\left(\frac{K_1}{K_2}\right)$	$\frac{1}{T}$ (μk^{-1}) $= \frac{1}{T_1 + 273} - \frac{1}{T_2 + 273}$
1	T_1 = 25 −150 °C T_2 = 25 −170 °C	$\frac{1.6}{0.6} = 2.67$	$\frac{1}{360.5} - \frac{1}{370.5} = 74.87$
2	T_1 = 25 −170 °C T_2 = 25 −185 °C	$\frac{0.6}{0.3} = 2.00$	$\frac{1}{370.5} - \frac{1}{378} = 53.55$

$$\frac{\ln\left(\frac{K_1}{K_2}\right)_{\text{case 1}}}{\ln\left(\frac{K_1}{K_2}\right)_{\text{case 2}}} \approx \frac{\left(\frac{1}{T_1} - \frac{1}{T_2}\right)_{\text{case 1}}}{\left(\frac{1}{T_1} - \frac{1}{T_2}\right)_{\text{case 2}}}$$

$$\frac{\ln(2.67)}{\ln(2.00)} = \frac{0.982}{0.693} \approx \frac{74.87\mu}{53.55\mu} \approx 1.4. \tag{9}$$

Since the ratio of the acceleration factors and the temperature terms of both cases is roughly equal to 1.4, it can be concluded that the calculation of the slope of the activation energy is accurate. By multiplying the slope with the Boltzmann constant, the activation energy of the devices is calculated to be about 1.13 eV.

Typically, high activation energy suggests that the device is more robust and can withstand higher levels of thermal stress. The activation energy of the GaN HEMTs has been reported to be around 1.84 eV considering bare dies [48]. However, the components' package and the presence of auxiliary components will lower the overall devices' activation energy. Moreover, the mechanical stresses created by the ATC tests further degrade the device more quickly due to the fast temperature transients compared to constant temperature tests. These analyses help engineers design for better reliability of GaN FETs-based converters.

VI. CONCLUSION

This article presents a comprehensive investigation of the aging characteristics of GaN HEMTs. The results of the ATC tests show that there are no substantial changes in the gate–source leakage current or the output capacitance of the GaN HEMTs. Degradation occurs, however, primarily due to reduced 2DEG layer density and mobility caused by channel heating. The characterization results indicate that the RDS_{on} increases as the device degrades, making it a reliable indicator of aging. Moreover, the time (designated as degradation time) taken for RDS_{on} to change from one value to another also

increases with aging, making it a useful precursor for health monitoring. The proposed empirical method uses the degradation time to estimate the activation energy of GaN HEMTs under ATC.

This study highlights the following key findings.

1) The RDS_{on} measurement is an effective way to monitor the aging profile and estimate the junction temperature of FETs as it is closely related to the device degradation, unlike other parameters such as I_{GSS} and I_{DSS}, which are prone to issues with sensing accuracy.
2) The degradation of the GaN HEMT is not only caused by hot-electron trapping but also by the reduction of mobility and density in the 2DEG layer as a result of channel heating.
3) The RDS_{on} curves get slightly distorted after a few thousand cycles, indicating the high reduction in mobility and density of the 2DEG layer in devices subjected to high thermal cycling windows.
4) Regardless of the thermal cycling window, the empirical method of calculating activation energy shows a high activation energy of ~1.13 eV. By establishing the relationship between activation energy and thermal cycling tests, designers and manufacturers can improve the reliability of GaN HEMTs- based converters.
5) Higher potential stress combined with ATC can lead to faster degradation of the GaN FETs and help quantify the effects of applying practical voltages on the devices' reliability—This is an ongoing research work.

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