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End-to-End Direct Digital Synthesis Simulation and Mathematical Model to Minimize Quantization Effects of Digital Signal Generation

PRANAV R. PATEL (Member, IEEE), AND RICHARD K. MARTIN

Department of Electrical and Computer Engineering, Air Force Institute of Technology, Wright-Patterson AFB, OH 45433, USA

CORRESPONDING AUTHOR: P. R. PATEL (e-mail: prpatel@ieee.org)This work was supported by Air Force Institute of Technology.

ABSTRACT Direct digital synthesis (DDS) architectures are becoming more prevalent as modern digital-to-analog converter (DAC) and programmable logic devices evolve to support higher bandwidths. The DDS architecture provides the benefit of digital control but at a cost of generating spurious content in the spectrum. The generated spurious content may cause intermodulation distortion preventing proper demodulation of the received signal. The distortion may also interfere with the neighboring frequency bands. This article presents the various DDS architectures and explores the DDS architecture which provides the most digital reconfigurability with the lowest spurious content. End-to-end analytical equations, numerical and mathematical models are developed to determine the location and power levels of spurs. Afterwards, the analytical equations, numerical and mathematical models are shown to be consistent with the experimental data. A developer can use the information to design a DDS architecture that meets their minimum requirements.

INDEX TERMS Direct digital synthesis, frequency synthesizers, DDS, signal synthesizer, digital synthesizer, FPGA, spurious emission, bandwidth, quantization, mathematical analysis, frequency spectrum.

I. INTRODUCTION

SIGNAL generation architectures have evolved from having an analog architecture to a digital architecture. The digital architecture provides the flexibility of signal generation that is limited with an analog architecture, and engineers have started to make the transition to such architecture [1]. Signal generation using an all-digital architecture is also called direct digital synthesis, and the DDS architecture has been adopted by various industries. Broadband communication systems, automatic test equipment (ATE), radar and jammers are some types of products using DDS architectures [2].

The DDS architecture has been used in various broadband communication applications. The architecture is being used in cable television (CATV) to transmit multiple types of content, such as video and data, over a fiber-optic network [3], [4]. Multiple channels of quadrature amplitude modulation (QAM) signals are produced to deliver content. The flexibility of the DDS also offers CATV operators the ability to have a single frequency translation from baseband to radio frequency (RF). On cellular networks, such as 4G long-term evolution (LTE), the DDS architecture is used to generate quadrature-based signals with multiple types of modulation [5]. This eliminates the need for frequency multipliers or separate I/Q channels, thus reducing the cost of the device [5]. Also, the DDS architecture is able to utilize beamforming capability by controlling the timing of the RF samples [6].

ATE also employs the DDS architecture in frequency generators or synthesizers [7], [8]. The architecture provides the capability of programmability of the output frequency by changing the rate of phase accumulation at a given sampling rate. This eliminates a need for additional analog circuitry to support high bandwidth of signal generation.

Radar systems require waveforms with high fidelity to be transmitted and received [9]. The systems use the DDS architecture to generate a linear frequency modulated (LFM) chirp signal. The programmability feature provides an additional benefit of configuring the waveform parameters without needing to redesigning the hardware. The DDS architecture

is also able to control the timing of the RF samples which provides beamforming capability [6].

Electronic warfare (EW) systems use the DDS architecture for electronic jamming and spoofing [10]. The DDS architecture is used to rapidly tune to a specified frequency and generate a sinusoidal signal. It can generate a wide-band signal to completely drown out the entire spectrum. Also, the architecture can rebroadcast a legitimate user's signal to provide a spoofing capability.

Using a DDS architecture with a high-speed DAC may provide the required flexibility for future-proof signal generation architecture [1]. DDS allows for digital control of frequency and phase in subnano-hertz and subnano-degrees, respectively. Even though DDS allows for precise control, analog components may introduce variations to the generated signal, such as frequency drift. Due to analog component aging, system calibration is needed to compensate for these variations. The DDS architecture reduces the number of analog components used. When used as a quadrature synthesizer, DDS eliminates the delays between the in-phase and quadrature (I/Q) channels. Finally, the entire DDS can be controlled digitally thus giving software-defined capability to the system. In an operational system, the ability to dynamically update signals may drastically reduce modernization costs and development time.

The contributions of this article are as follows. (i) A DDS simulation or numerical model is developed using a DDS architecture that provides the most software-defined flexibility with the least amount of generated spurs in the spectrum. The DDS simulation model incorporates phase and amplitude quantization. This section also compares the simulation model with the experimental data to determine consistency. (ii) A mathematical model is developed to explain any abnormal behavior caused by quantization of the DDS simulation model. A mathematical model is able to aid the developer in determining the location and power level of the spurs that can not be easily attained by analytical equations. (iii) Analytical equations for the phase quantization are formed to determine the location and power level of the spurs from the DDS simulation and mathematical models. (iv) The results from the analytical equations are compared with the phase quantized data from the DDS simulation and mathematical models. Thus, the four contributions form a chain of: numerical model $\rightarrow$ mathematical model $\rightarrow$ analytical equations $\rightarrow$ numerical and mathematical analysis. To the best of our knowledge, such modeling and analysis has never been performed for the DDS before.

This article is organized as follows. Section II summarizes the functionality and spur performance of various DDS architectures. Section III describes the modeling process. The section also elaborates on the technical limitation of the current generation of microprocessors and how software is able to overcome such limitations. Section IV describes the entire DDS simulation model with phase and amplitude quantization. Section V covers the entire mathematical model with phase and amplitude quantization. Section VI describes the analytical equations derived from the mathematical model. The analytical equations are used to determine the location and power levels of the in-band spurious emissions. Section VII compares the results from the analytical equations with the data from the DDS simulation model. Section VIII presents the conclusion.

II. SYSTEM MODELS

Various types of DDS architectures have been researched. The performance of each architecture differs in spectral purity. Lack of spectral purity would cause the desired signal to degrade in total power, the generation of in-band spurious content. This poses a problem for low power and timing applications such as global navigation satellite system (GNSS). Additional loss of total power of an already weak signal would cause acquisition problems for the receiver. The generation of in-band spurious content would cause correlation problems with the receiver because the spurs would be within the bandwidth of the signal.

There are six major types of DDS architectures: Pulse Output, Fractional Divider, Triangle Output, Sine Output, Phase Interpolation, and Wheatley Random Jittering Injection. The performance of each architecture varies and this will impact the spectral purity of the signal. Each architecture requires a combination of analog and digital components. Minimizing the amount of analog components in the architecture increases the software-defined capability of the overall system. For this reason, the Sine Output DDS architecture is the primary focus and is discussed further in current and later sections.

A. PULSE OUTPUT DDS

The Pulse Output architecture, as shown in Figure 1(a), is the simplest of the six DDS architectures [11] and the most versatile in generating different kinds of waves at a specific carrier frequency (f_c). It consists of an accumulator with j-bits of resolution. For every sampling clock frequency (f_s), ϕ_{step} is added onto the previous value. The Pulse Output architecture produces pulses, square, and sawtooth waves at f_c is described as

$$f_c = \frac{\phi_{\text{step}}}{2^j} \cdot f_s. \tag{1}$$

The square wave is generated by the most significant bit (MSB) of the output of the storage register. The sawtooth wave is generated by the resulting value of the accumulator [12]. The accumulator output is expressed by

$$R(n) = mod\left(\phi_{\text{step}} \cdot n, 2^j\right). \tag{2}$$

The pulses are generated by the overflow flag from the adder in the accumulator. The overflow flag is set when the value of the accumulator exceeds j-bits. Since there is an abrupt change in energy, high frequency content is generated thus causing large in-band spurious emissions to be generated [13], [14]. Out of all six architectures, the Pulse Output architecture has the most in-band spurious content and phase jitter [11].

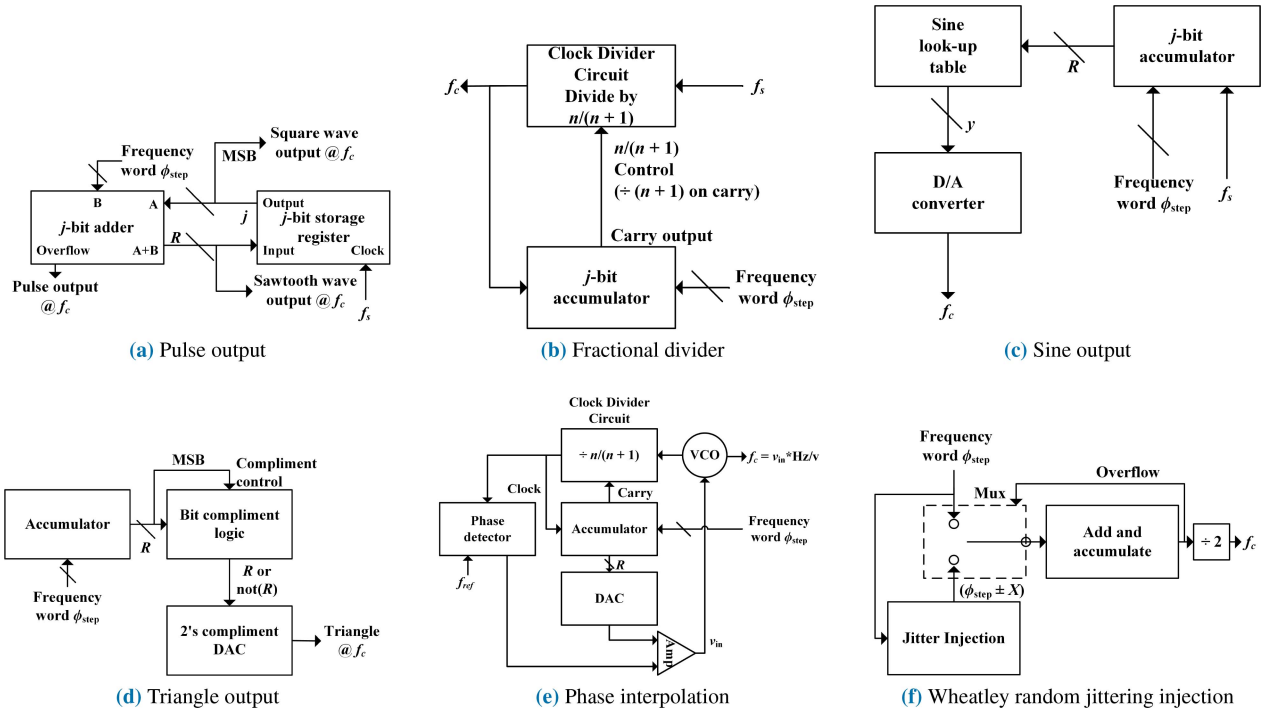


FIGURE 1. DDS architectures [11].

B. FRACTIONAL DIVIDER DDS

The Fractional Divider architecture, as shown in Figure 1(b), is a modified version of the Pulse Output architecture. The clock of the accumulator is controlled by a clock divider circuit. The clock divider circuit regulates the clock to determine when the accumulator will perform its addition process. The Fractional Divider architecture produces pulses at f_c and is described as

$$f_c = \frac{f_s}{n + \left(\frac{\phi_{\text{step}}}{2^j}\right)}. \tag{3}$$

Pulses are generated with this architecture. As a result, the amount of in-band spurious content is equivalent to the Pulse Output architecture, but the phase jitter is less due to being able have fractional control over the accumulator [11].

C. SINE OUTPUT DDS

The Sine Output architecture, as shown in Figure 1(c), produces a sinusoidal wave. The phase of the signal is produced from the accumulator and is described by

$$f_c = \frac{\phi_{\text{step}}}{2^j} \cdot f_s, \tag{4}$$

$$R(n) = mod\left(\phi_{\text{step}} \cdot n, 2^j\right). \tag{5}$$

The phase is used as an address for the sine look-up table (LUT) [15]. The quantized form of a sinusoidal wave is stored in the LUT [16]. As a result, a signal is produced which resembles the ideal form of a sinusoidal wave and described by [17]

$$y(n) = \sin\left(\frac{2 \cdot \pi \cdot R(n)}{2^j}\right). \tag{6}$$

Any quantization effects are caused by the bit resolution of the accumulator and the stored sinusoidal wave in the LUT. The quantization effects will vary the magnitude of the in-band spurious emissions, but the amount of phase jitter is the same as the Pulse Output and Triangle Output architectures.

This architecture relies on a LUT and DAC, and these two components are the cause of the quantization effects. The total number of values, and the size of the values govern the overall size of the LUT. The DAC restricts the maximum size of the values in the LUT. The phase resolution determines the number of values inside the LUT. The higher the phase resolution, the larger a LUT is required. In a microprocessor, microcontroller, programmable logic device (PLD), or application-specific integrated circuits (ASIC), memory resources are finite. Therefore, the dimensions of the LUT are constrained to what resources are available on the chip. This limitation causes the signal to be amplitude and phase quantized, thus causing in-band spurious emissions to be generated.

D. TRIANGLE OUTPUT DDS

The Triangle Output architecture, as shown in Figure 1(d), produces a triangle wave. Unlike the pulsed architectures, the Triangle Output architecture requires a DAC to convert digital values into an analog representation form. Like the prior architectures, the accumulator is used to calculate phase

of the signal. The MSB of the phase is stripped from the resulting value and used to determine if the remaining bits should be complimented. As a result, the values will gradually increase and decrease over time. The Triangle Output architecture produces a triangle wave at f_c where

$$f_c = \frac{\phi_{\text{step}}}{2^j} \cdot f_s. \tag{7}$$

Unlike the Pulse Output architecture, there is a gradual change in value. As a result, the in-band spurious emissions are less in magnitude, but the amount of phase jitter is the same as the Pulse Output architecture.

E. PHASE INTERPOLATION DDS

The Phase Interpolation architecture, as shown in Figure 1(e), uses external analog components such as voltage controlled oscillator (VCO) and a phase detector. The VCO is used as a phase lock loop (PLL) to provide feedback to the divider loop, which controls the clock to the accumulator. The phase detector allows for greater reduction in phase jitter and in-band spurious emissions compared to other architectures.

F. WHEATLEY RANDOM JITTERING INJECTION DDS

The Wheatley Random Jittering Injection architecture, as shown in Figure 1(f), uses a dithering technique to reduce the amount of in-band spurious content. The dithering technique injects uniformly distributed values from 0 to $\phi_{\text{step}} - 1$ into the signal causing the periodicity of the phase deviation patterns to be destroyed [18]. Since noise is being injected into the signal, the overall noise floor and phase jitter are increased.

III. END-TO-END MODELING OVERVIEW

The Sine Output DDS was selected because it produces the minimum number and power of spurs in the spectrum, and provides the most flexibility to incorporate software-defined capability. Using the Sine Output DDS architecture, a DDS simulation and mathematical models are developed in a simulation environment. The models help understand the quantization error caused by truncation of the phase and amplitude of a signal. Having both models in a simulation environment allows for a closer examination of the signal generation process. Reference [13] documents the results of the DDS simulation model, and it is comparable to the results from the experimental data from a hardware device using a DDS architecture. The noise floor of the test equipment is higher than the simulated model, therefore many low power signals will not be seen on the test equipment. The models developed in the simulation environment provide a better platform to analyze quantization error.

There are two sections in the DDS simulation model. The first section analyzes the effects of phase quantization of the signal. The second section analyzes the effects of amplitude quantization of the signal. The mathematical model analytically describes the entire DDS simulation model.

Designing a DDS simulation model with a 64-bit numerically controlled oscillator (NCO) on a system with a 64-bit Intel processor poses a problem because the model uses a combination of double-precision floating-point and 64-bit integer values. Traditionally, Intel-based processors use the IEEE-754 standard to represent a floating-point number. In the standard, the MSB is the sign bit of the number, while the next 11 bits are for the exponent. The final 52 bits least significant bits (LSBs) are the normalized mantissa [19]. The word size of the mantissa restricts the numerical precision of a number.

Software applications overcome this limitation by distributing the value into multiple registers on the processor. Each register is calculated independently and the outputs are added together [20]. This functionality is available in the Fixed-Point Designer toolbox of Mathworks MATLAB, but the implementation details are proprietary. For this effort, the NCO in the DDS simulation model will use the MATLAB toolbox. In the mathematical model, the signal generation of the cosine signal utilizes the MATLAB toolbox to provide precision beyond the IEEE-754 standard limitation.

IV. DDS SIMULATION MODEL

The DDS simulation model is a representation of the algorithm implemented in a hardware device. The simulation model allows for the developer to rapidly characterize the DDS architecture with phase and amplitude quantization.

A. PHASE QUANTIZATION

The NCO generates the phase of the signal. The NCO consists of a 64-bit accumulator ($j = 64$), and resolution of the NCO represents $\frac{1}{2^j}$ of a phase cycle of the signal. The step size of the accumulating rate generates the phase at a given frequency of the signal and is expressed by

$$\phi_{\text{step}} = \text{round}\left(2^j \cdot \frac{f_c}{f_s}\right), \quad \text{for } f_c \leq \frac{f_s}{2}. \tag{8}$$

The round operation minimizes the amount of phase error that is introduced, and the equation to determine the maximum phase error in radians is expressed by

$$\phi_{\text{stepError}} = 2 \cdot \pi \cdot 2^{-j-1}. \tag{9}$$

The resulting phase is expressed in cycles that is normalized from 0 to $2^j - 1$ and is expressed by

$$x_{\text{phase}}[n] = n \cdot \phi_{\text{step}}, \quad \text{for } 0 \leq n \leq 2^j - 1. \tag{10}$$

Afterwards, the phase is quantized to the appropriate word size (k = word size). The phase is right shifted until the top k bits are remaining. The floor operation truncates the value once it has been shifted. The resulting quantized phase wraps at 2^k for the read only memory (ROM), which will be discussed later, and is expressed by

$$x_{\text{qphase}}[n] = \text{mod}\left(\text{floor}\left(\frac{x_{\text{phase}}[n]}{2^{j-k}}\right), 2^k\right), \quad \text{for } j \geq k. \tag{11}$$

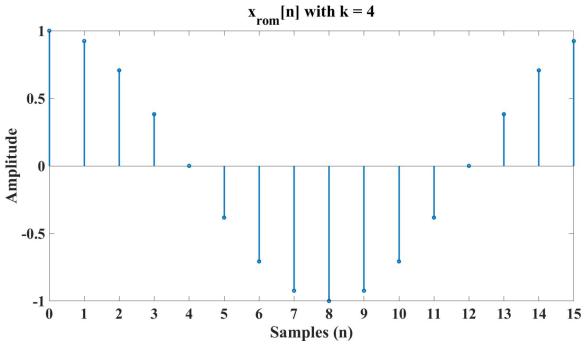


FIGURE 2. Stem plot of ROM of a single period cosine wave.

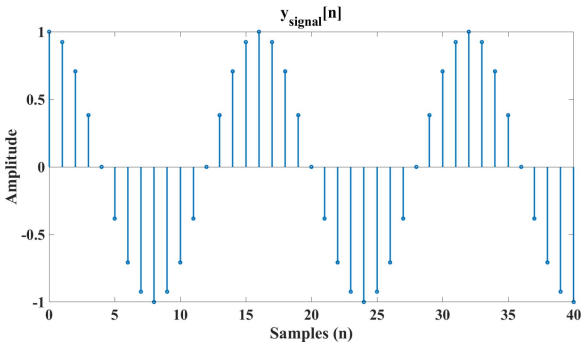


FIGURE 3. Stem plot of y_{signal} incrementing at $\frac{2\cdot\pi}{16}$ radians.

Using Equation (9) with the accumulator of the NCO being 64 bits ($j = 64$), the error in phase is minuscule. Therefore, Equation (11) is simplified to a close approximation form of

$$x_{\text{qphase}}[n] = \text{mod}\left(\text{floor}\left(\frac{2^k \cdot f_c \cdot n}{f_s}\right), 2^k\right), \quad \text{for } f_c \leq \frac{f_s}{2}, n \geq 0. \tag{12}$$

A ROM is used to store one period of a cosine signal with a sample length of 2^k. The period of the cosine signal is normalized and expressed by [21], [22]

$$x_{\text{rom}}[n] = \cos\left(\frac{2 \cdot \pi \cdot n}{2^k}\right), \quad \text{for } 0 \leq n \leq 2^k - 1. \tag{13}$$

Figure 2 shows the values from Equation (13), and these values are stored in a ROM.

The modulo operation in Equation (11) bounds the values within the sample size of the ROM, shown in Figure 2. The signal is generated by picking out points from Equation (13) by using Equation (11) as the index, and this is expressed by

$$y_{\text{signal}}[n] = x_{\text{rom}}[x_{\text{qphase}}[n]]. \tag{14}$$

Figure 3 shows y_{signal} over 40 samples (n) with the phase incrementing by a value of 1, which is equivalent to $\frac{1}{16}$ of a period or $\frac{2\cdot\pi}{16}$ radians. Figure 4 shows the phase incrementing twice as large, or at $\frac{4\cdot\pi}{16}$ radians, over the same number of samples as Figure 3.

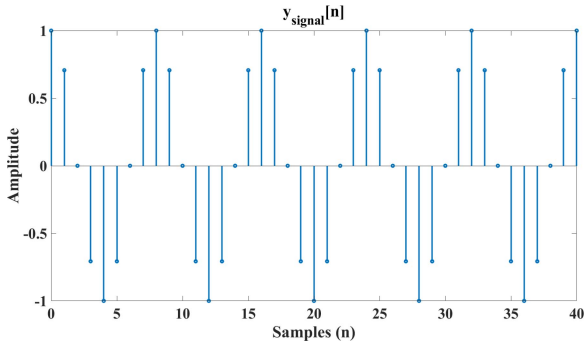


FIGURE 4. Stem plot of y_{signal} incrementing at $\frac{4\cdot\pi}{16}$ radians.

B. AMPLITUDE QUANTIZATION

The previous section did not consider the amplitude quantization of the values inside the ROM, Equation (13). In this section, the amplitude values of the signal are quantized or fixed-point, and the ROM consists of quantized values.

The type of number representation (s), number of integer bits (r) and number of fractional bits (q) define a fixed-point value. The type of number representation determines if the value is either unsigned or 2's complement. If the value is an unsigned number, 0 is used otherwise 1 is used. The total word size, stored in ROM, of the fixed-point value is

$$B = s + r + q. \tag{15}$$

The base-10 floating point cosine value from Equation (13) is converted to an integer form for storing in a ROM. First, the floating point value is converted to a base-2 or binary form. Next, the decimal point of the binary form is shifted right by the specified fractional bits (q). Finally, the value is rounded such that the signal is zero mean centered. This process is expressed by

$$x_{\text{qrom}}[n] = \text{round}\big(2^q \cdot x_{\text{rom}}[n]\big), \quad \text{for } q \geq 0. \tag{16}$$

The phase of the signal, which is wrapped at 2^k or $2 \cdot \pi$, is used to look up the amplitude of the desired in the ROM and is expressed by

$$y_{\text{qsignal}}[n] = x_{\text{qrom}}\big[x_{\text{qphase}}[n]\big]. \tag{17}$$

The signal, from Equation (17), is quantized in phase and amplitude. Quantization causes spurious content to appear in the spectrum. The spurious content may potentially cause intermodulation distortion to the desired signal. A mathematical model is useful to explain these types of unpredictable behavior, as shown in Figure 5.

V. MATHEMATICAL MODEL

A mathematical model is used to analytically explain the functionality of the DDS simulation model. Also, it allows for an easier explanation of any kind of unpredictable behavior in the signal generation process.

Equation (18) is used to generate a cosine signal in the continuous time domain. A scale factor (X_m) is used to scale

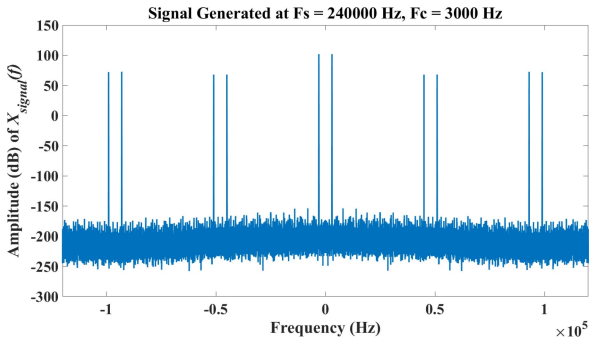


FIGURE 5. Spectral plot of signal with spurs.

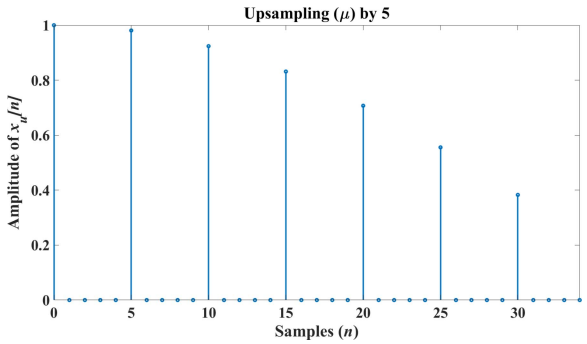


FIGURE 6. Upsampling of signal.

the cosine signal to the appropriate amplitude. f_c is the carrier frequency, and t is time. In the digital domain, each point in a cosine signal is generated at a specific interval. This specific interval is a sampling frequency (f_{sl}). The equations for the continuous and discrete signal generation of a cosine signal are

$$x(t) = X_m \cdot \cos(2 \cdot \pi \cdot f_c \cdot t), \quad \text{for } t \geq 0, \tag{18}$$

$$x[n] = X_m \cdot \cos\left(2 \cdot \pi \cdot f_c \cdot \frac{1}{f_{sl}} \cdot n\right), \quad \text{for } n \geq 0. \tag{19}$$

The phase resolution is restricted to the number of phase bits (k), therefore the values of the cosine signal must be increments of $\frac{1}{2^k}$. The sampling rate is expressed by

$$f_{sl} = f_c \cdot 2^k, \quad \text{for } k \geq 0. \tag{20}$$

Equation (20) is substituted into Equation (19) as expressed by

$$x[n] = X_m \cdot \cos\left(\frac{2 \cdot \pi \cdot n}{2^k}\right), \quad \text{for } n \geq 0, k \geq 0, \tag{21}$$

and the total energy in $x[n]$ is expressed by

$$e_{sl} = \sum_{n=0}^{N-1} |x[n]|^2. \tag{22}$$

The amplitude of the cosine signal is quantized by the total number of bits (B). The quantized sample is calculated by taking the base-10 number and converting it to a 2's complement binary number (**b**). The MSB is the sign bit (b_0), where the value is multiplied by a negative one. The remaining bits are multiplied by the power of two raised to the location i of the bit and summed together. Next, this result is added together with previous operation and multiplied with a scale factor. The result is a quantized sample base-10 number, and is expressed by

$$\tilde{x}[n] = X_m \cdot \left(-b_0 + \sum_{i=1}^{B} b_i \cdot 2^{-i}\right). \tag{23}$$

The cosine signal is quantized by adding the individual samples with an quanitization error offset, and the value is scaled by a scale factor (X_m). The quantization error offset takes the difference between the true sample from the quantized sample is expressed by

$$\epsilon_A[n] = \tilde{x}[n] - x[n],$$
$$\begin{cases} -\frac{X_m \cdot 2^{-B}}{2} < \epsilon_A \leq \frac{X_m \cdot 2^{-B}}{2}, & \text{for rounding.} \\ -X_m \cdot 2^{-B} < \epsilon_A \leq 0, & \text{for truncation.} \end{cases} \tag{24}$$

Once the quantization error offset is calculated it is added to the true samples, and is expressed by

$$x_A[n] = x[n] + \epsilon_A[n]. \tag{25}$$

For complete in-depth discussion on amplitude quantization, please see Reference [23].

Once the cosine signal is generated, and amplitude has been quantized, up and down sampling rates are calculated based on the phase resolution, sampling and carrier frequency parameters. This will adjust the cosine signal to the final sampling and carrier frequency. The upsampling (μ) to downsampling (ν) ratio is reduced to an irreducible fraction, and becomes sampling frequency at intermediate frequency (IF) (f_{sl}) and the sampling frequency at RF (f_{sh}) of the signal. This is expressed by

$$\frac{\mu}{\nu} = \frac{f_{sh}}{f_{sl}}. \tag{26}$$

Upsampling and downsampling the signal with the zero-order-hold (ZOH) operation mimics the phase quantization implemented in the DDS simulation model. The ZOH operation is used with the upsampling rate is applied to the cosine signal in two stages. The first stage is to insert zeros to the signal as expressed by Equation (27) and shown in Figure 6.

$$x_u[n] = \begin{cases} x_A[n/\mu], & n = 0, \pm\mu, \pm 2\mu, \ldots \\ 0, & \text{otherwise} \end{cases} \tag{27}$$

The total energy of the signal after being upsampled is the same as the original because upsampling inserts zeros in-between the samples. The second stage convolves an impulse response signal from Equation (28) with the upsampled signal from Equation (27). Figure 7 shows the resulting signal.

$$h_{\text{ZOH}}[n] = \text{rect}\left(\frac{n - 0.5 \cdot \mu}{\mu}\right) \tag{28}$$

$$x_{\text{ZOH}}[n] = x_u[n] * h_{\text{ZOH}}[n] \tag{29}$$

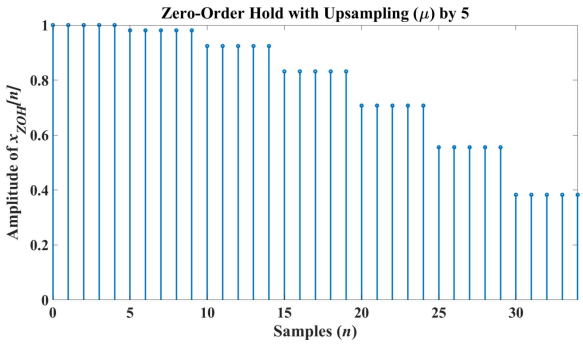


FIGURE 7. Zero-order hold of signal.

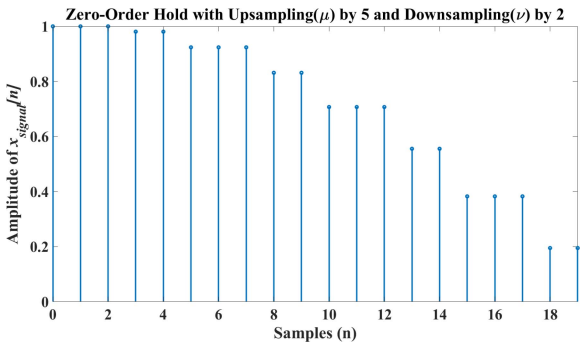


FIGURE 8. Downsampling of signal.

ZOH operation replicates the individual samples by μ causing an increase in total energy and is expressed by

$$e_{\text{ZOH}} = \mu \cdot \sum_{n=0}^{N-1} |x[n]|^2. \tag{30}$$

After the ZOH operation, the signal is downsampled without any kind of pre-filtering. It is expressed by Equation (31) and shown in Figure 8. The downsampling operation causes the step widths to become non-uniform, as shown in Figure 8. The total energy of the signal can be approximated by using Equation (32).

$$x_{\text{signal}}[n] = x_{\text{ZOH}}[n \cdot \nu] \tag{31}$$

$$e_s = \frac{\mu}{\nu} \cdot \sum_{n=0}^{N-1} |x[n]|^2. \tag{32}$$

VI. RESULTS OF DDS AND MATHEMATICAL MODEL QUANTIZATION EFFECTS AND MATHEMATICAL SOLUTION

Figure 9 shows the spectral plot of Equation (21). The total energy of the signal is focused on the carrier signal. When the signal is upsampled by using Equation (27), the new sampling frequency is the upsampled rate multiplied by the original sampling frequency. The results of the upsampling causes the spectrum to be replicated by multiples of the original sampling frequency. This causes spurs to be generated in the spectrum and is expressed by

$$x_{sup}[x_{si}] = x_{si} \cdot f_c \cdot 2^k, \quad \text{for } x_{si} > 0. \tag{33}$$

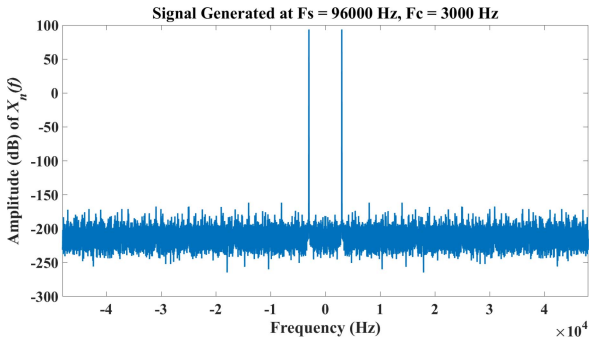


FIGURE 9. Spectral plot of baseband signal.

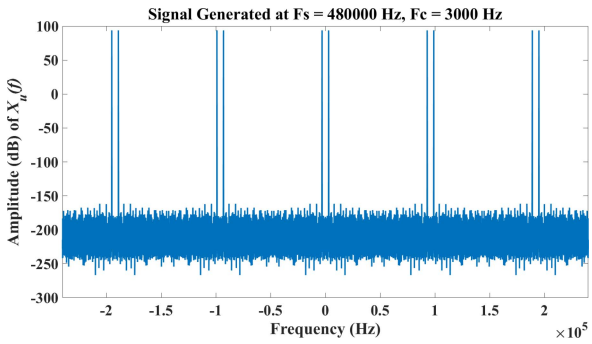


FIGURE 10. Spectral plot of upsampled baseband signal.

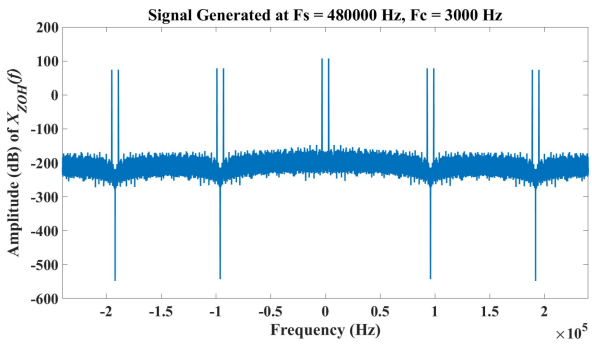


FIGURE 11. Spectral plot of ZOH signal.

where x_{si} is the index of the spur from 0 Hz, and shown in Figure 10. The mirror image is centered around the original sampling frequency, and the upsampling operation does not add any kind of energy of the signal. It can be calculated by taking the absolute value of the summed data points in the spectral domain, and the result value is divided by the total number of samples as expressed by

$$e = \frac{1}{N} \cdot \sum_{k=0}^{N} |X[k]|^2. \tag{34}$$

Afterwards, the signal is goes through a ZOH operation, where a rect function with the length of the upsampled rate is convolved with the incoming signal, as described in Equation (28) and Equation (29). The power of the spurs are reduced over frequency. The approximate location is expressed by Equation (33) and the power of each spur is

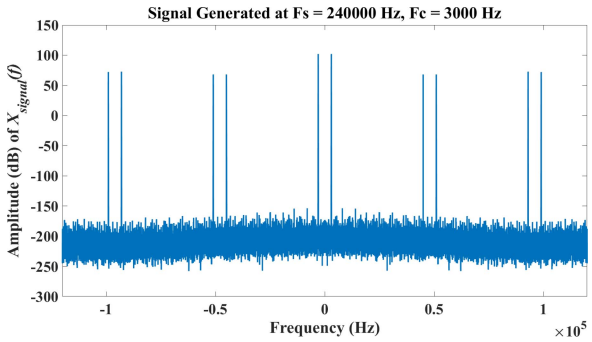
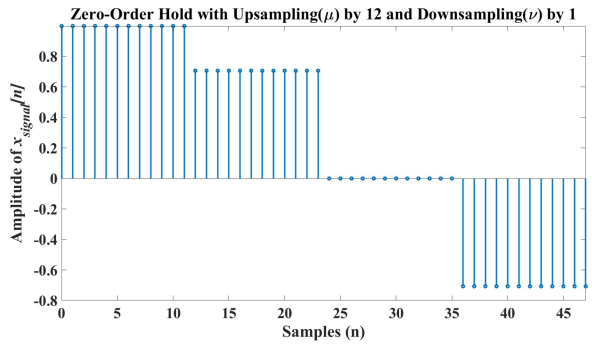
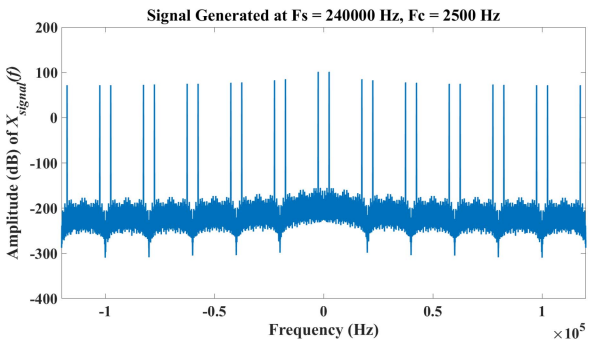


FIGURE 12. Spectral plot of downsampled ZOH signal.

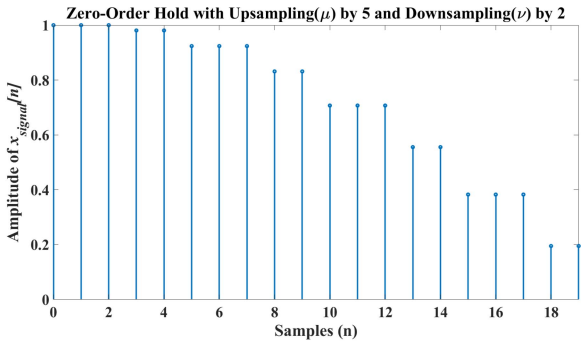


(a) Time plot

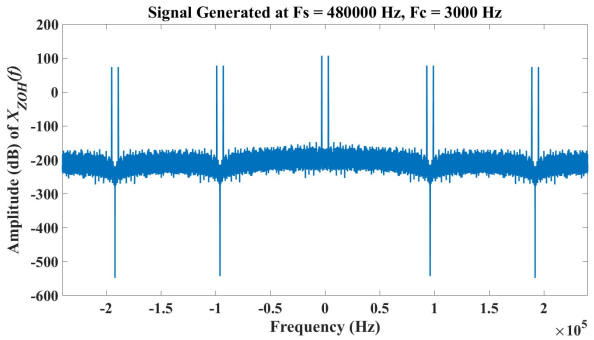


(b) Spectral plot

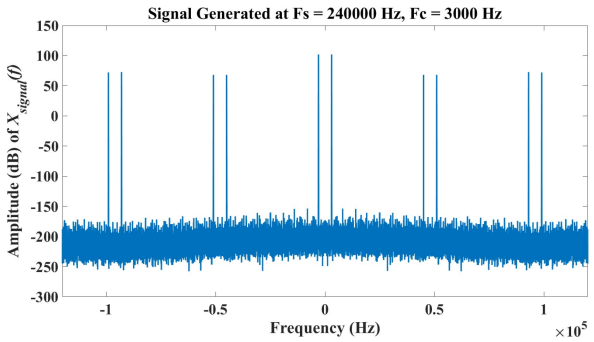
FIGURE 13. Example 1 of periodic signal.



(a) Time plot of non-periodic signal



(b) Spectral plot of periodic signal



(c) Spectral plot of non-periodic signal

FIGURE 14. Example 2 of periodic and non-periodic signals.

expressed by

$$p_{dBc}[x_{si}] = -20 \cdot \log10\Big(x_{si} \cdot 2^k\Big), \quad \text{for } x_{si} > 0. \tag{35}$$

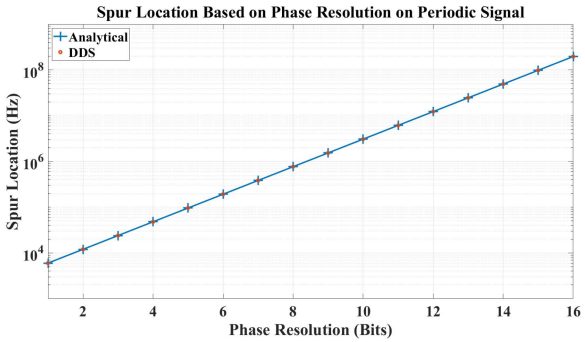
The downsampling operation is applied causing the signal to be irregular as shown in Figure 8. This irregularity causes additional in-band spurs to be generated as shown in Figure 12, and the location of each spur is expressed by taking the greatest common divisor (GCD) of f_{sh} and f_{sl} as shown in Equation (36).

$$x_{\text{sdown}}[x_{si}] = x_{si} \cdot \text{GCD}\Big(f_c \cdot 2^k \cdot \frac{\mu}{\nu}, f_c \cdot 2^k\Big), \quad \text{for } x_{si} > 0 \tag{36}$$

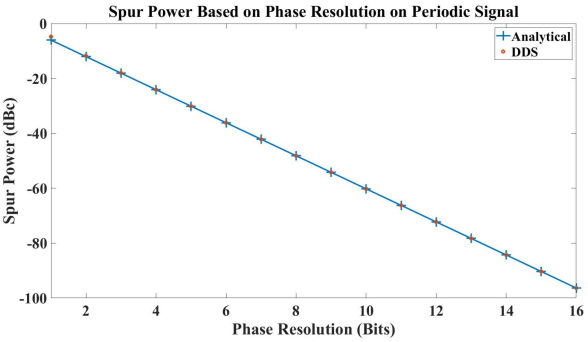
The power of the spurs is uncertain because of the irregularity of the signal caused by the downsampling operation. The power of the carrier, in milliwatts, can be approximated by

$$p_{\text{car}} = \frac{X_m^2}{2}. \tag{37}$$

Regularity of the signal is certain when f_s is divisible by $f_c \cdot 2^k$. Figures 13(a) and 13(b) show the time and spectral plots of a signal. The plots show periodicity which causes spurious emissions to be generated at every $f_c \cdot 2^k$ Hz with $k = 5, f_c = 2500$ Hz, and $f_s = 240,000$ Hz. Figure 14 shows when periodicity does not exist with $k = 5, f_c = 3000$ Hz, and $f_s = 240,000$ Hz. Before the downsample operation, Figure 14(b) shows the spur is present at $192,000$ Hz. After the downsample operation, Figure 14(c) shows the spur aliased to $48,000$ Hz. The downsample operation causes frequency folding to occur and the spur from the second Nyquist zone is aliased into the first.

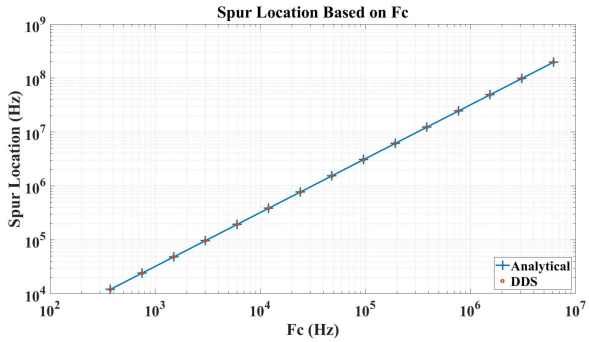


(a) Spur location based on phase resolution

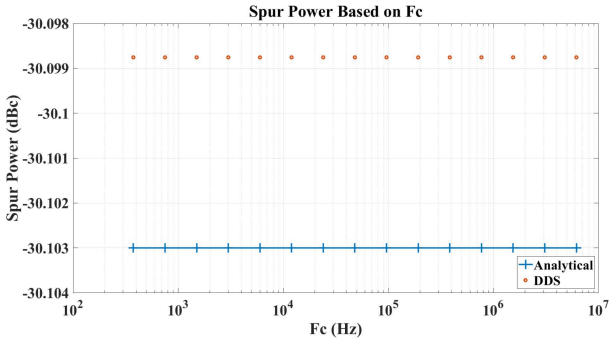


(b) Spur power based on phase resolution

FIGURE 15. Fixed f_C and varying phase resolution.



(a) Spur location based on f_c



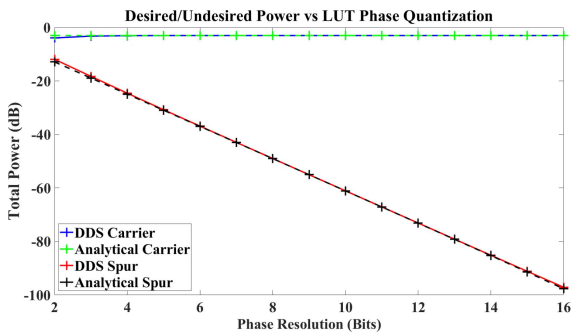
(b) Spur power based on f_c

FIGURE 16. Fixed phase resolution and varying f_C.

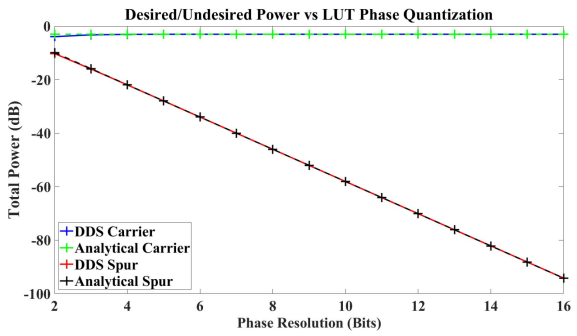
Figure 15 shows the results between the mathematical solution and the DDS simulation model. The phase resolution is varied between 1 and 16 bits, and the f_c is set to 3000 Hz for Figures 15(a) and 15(b). Figure 15(a) shows the location of the first spur with respect to the phase resolution. Figure 15(b) shows the amplitude of the first spur with respect to the phase resolution. The phase resolution is set to 5 bits and f_c is varied throughout the first Nyquist zone for Figures 16(a) and 16(b). Figure 16(a) shows the location of the first spur with respect to f_c. Figure 16(b) shows the amplitude of the first spur with respect to f_c. There are small discrepancies between the DDS simulation and mathematical models on Figures 15(b) and 16(b). This is because of numerical precision error of the computational program.

VII. QUANTIZATION ERROR EFFECT

Figures 17, 18, and 19 show the effects of quantization of phase and amplitude on the carrier signal and the spurious content. Figures 17(a) and 19(a) show the quantization error when the signal is periodic, and Figures 17(b) and 19(b) show the quantization error when the signal is non-periodic. The signal is periodic when f_s is divisible by $f_c \cdot 2^k$, otherwise the signal is considered non-periodic. Simulation models varied the phase and amplitude quantization range from 2 bits to 16 bits. The phase quantization figures are compared between simulation and mathematical models. The mathematical models are derived from equation from Section V. The amplitude quantization figures are compared between simulation and mathematical models from [24].



(a) Periodic signal



(b) Non-periodic signal

FIGURE 17. Phase quantization error.

Figures 17(a) and 17(b) show phase quantization effects on a periodic and non-periodic carrier signal between the DDS simulation and mathematical models. The figures show the sum of individual spur power throughout the entire spectrum

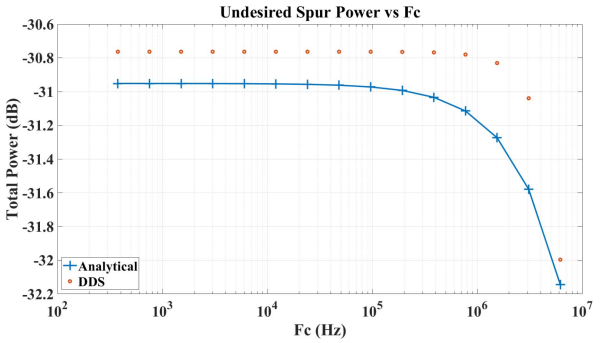
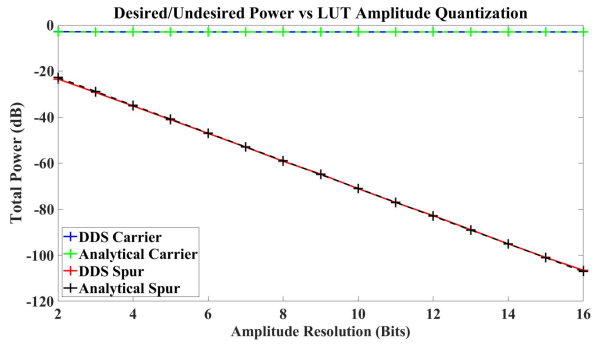
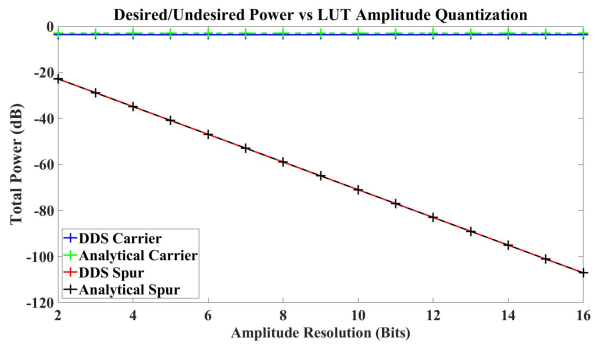


FIGURE 18. Total spur power between DDS simulation and mathematical models.



(a) Periodic signal



(b) Non-periodic signal

FIGURE 19. Amplitude quantization error.

for a specific phase resolution. Equations (35) and (37) are used to determine the mathematical model and to compare against the DDS simulation model. The increase in total power for the spurs could potentially cause intermodulation distortion [13]. Any small discrepancies between the DDS simulation and mathematical models are attributed to the numerical precision error.

Figure 18 shows phase quantization effects on the sum of the individual spur power throughout the entire spectrum across various frequencies for a specific phase resolution. Equations (35) and (37) are used to determine the mathematical model and to compare against the DDS simulation model. The DDS simulation and mathematical models are closely matched. Any small discrepancies between the DDS simulation and mathematical models are attributed to the numerical precision error of the computational program.

Figures 19(a) and 19(b) shows amplitude quantization effects on the periodic and non-periodic carrier signal and its spurs. The plots show that periodicity of the signal do not have an effect on the power of the spurs. Amplitude quantization affects the amplitude of the carrier and spurs. The carrier power still follows Equation (37). Equation (38) is used to determine the mathematical model of the spurs from amplitude quantization [24]. Any differences between the DDS simulation and mathematical models are attributed to numerical precision error.

$$p_{dB}[k] = 10 \cdot \log 10\left(\frac{2^{-k \cdot 2}}{12}\right), \text{ for } k > 0. \tag{38}$$

VIII. CONCLUSION

This article investigates the phase quantization effects numerically and mathematically for the Sine Output DDS architecture. Various DDS architectures are examined, and the Sine Output DDS architecture provided the most flexibility to incorporate software-defined capability. The architecture also provides flexibility in generating a wide variety of waveforms and controlling the number of spurious emissions in the spectrum. These spurious emissions may cause intermodulation interference with the generated signal. Being able to determine the location and power level of the spurious emission allows the developer to design an architecture that meets their minimum requirements.

The amount of control over the spurious emissions is limited by the number of resources available on a microprocessor, microcontroller, PLD, or Application-Specific Integrated Circuits (ASIC). Amplitude and phase quantization effects are generated by limiting the dimension of the LUT. The maximum size of the column for the LUT is restricted to the resolution of the DAC, and this restriction of size causes amplitude quantization. The number of rows in the LUT determines the resolution of phase and causes phase quantization.

A simulation model is used to replicate the implementation of the Sine Output DDS architecture inside a digital device. The mathematical model is developed to analytically explain the functionality of the simulation model. The developer can use both models to see the effects of signal generation by varying parameters. In this article, the mathematical model was used to derive analytical equations to determine the location and power of the spurious emissions.

Spurious emissions are generated by the DDS when phase and amplitude are quantized. Phase quantization depends on the carrier frequency and the phase resolution. The amount of spurious content is increased when the sampling frequency at RF and not divisible by the sampling frequency at IF because of frequency folding from other Nyquist zones. The mathematical model is used to determine the power level of these spurs before the frequency folding occurs. When the sampling frequency at RF and divisible by the sampling frequency at IF, the spurs appear at every multiple of the sampling frequency at IF, and the power of spurs is a multiple

of the phase resolution. This information can be used by the developer to minimize any kind of intermodulation distortion to the generated signal or in the neighboring bands.

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