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Feed Integration and Packaging of a Millimeter-Wave Antenna Array

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ABSTRACT A novel approach is presented and demonstrated for integrating a wideband vertically fed antenna array at Millimeter-Wave (mm-Wave) frequencies. Specifically, a novel cost-effective Antenna-In-Package (AiP) fabrication approach is presented, then a prototype operating from 55 GHz to 64 GHz is built while predicted performance is verified via measurements. The presented approach relies on separating fabrication into 1) the array and 2) the back-end feeding board. Assembly of the various components is achieved through several precision microfabrication steps utilizing a Ball-Grid-Array (BGA) technology with thermally stable conductive solder paste. The paper describes the realization of the final AiP aperture in terms of design tolerances, laboratory equipment, component placement and alignment, curing time duration and temperature ranges, and prototype on-the-go testing.

INDEX TERMS Antenna-in-package (AiP), ball-grid-array (BGA), millimeter-wave (mm-Wave), wideband antenna array.

I. INTRODUCTION

THERE is strong interest in low-profile, low-cost, low-weight, and low-power apertures [1]. Such arrays can ease the challenges associated with the highly fragmented and congested wireless spectrum [2], [3]. Presently, communication platforms (i.e., cell phones, GPS, vehicles, satellites) require access to many different and often widely separated bands of the spectrum. But having a separate Radio Frequency (RF) system for each of these applications and frequency bands is costly and inefficient.

Wideband antenna arrays enable high data throughput for Millimeter-Wave (mm-Wave) frequencies [4], [5], [6], [7] while providing a reduction in size and weight [8], [9], [10]. Additionally, electronic scanning removes the need for mechanical steering, eliminating large, heavy, and high-power actuators [11], [12]. One type of the most commonly used wideband antenna arrays are Tapered Slot Arrays (TSA). Among them, short and long Vivaldi Arrays have led to smaller aperture sizes over the past decade [13], [14], [15], [16], [17]. However, their end-fire layout and inherently non-planar orientation introduces challenges in realizing very low profiles above a ground plane, especially at higher frequencies. In contrast, patch antennas have shown a bandwidth of 20%. Stacked patch approach improves the bandwidth beyond 50%. However, realization of multi-layer stacked patch array at 64 GHz is quite challenging. It should be noted that the central idea of this manuscript is to introduce repeatable low-cost low-risk and outside the clean room fabrication and assembly techniques for scalable broadband apertures ($>$ 166% BW or 10:1) at mm-Wave regime. It is understood that the present aperture does not have such a large bandwidth as the focus is only on the fabrication and assembly of such scalable apertures. Indeed, we have been working for a while to create a successful fabrication recipe.

Typical antenna types for mm-Wave applications include reflectors, lens, and horn antennas. Although these antennas have high gain, they are less attractive for commercial mm-Wave applications as they are expensive, bulky, heavy, and cannot be integrated with solid-state devices [9]. To this end, we turn to inherently planar and wideband printed antenna arrays, such as Tightly Coupled Dipole Arrays

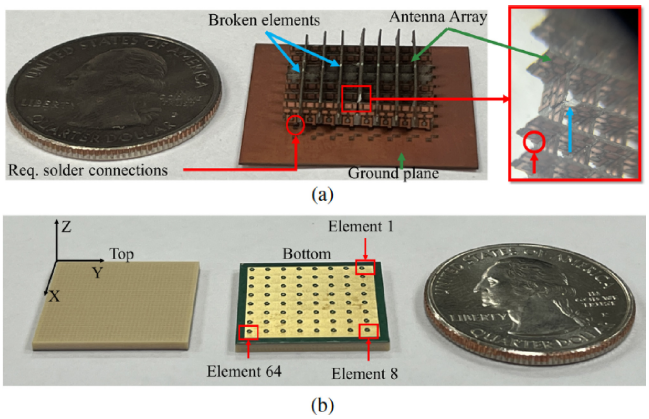

FIGURE 1. Antenna array prototypes realized in vertical and planar dipole orientations with a U.S. quarter shown for size comparison: (a) a non-planar antenna array assembly based on [48], with highlighted breaks and cracks due to the physical assembly challenges at mm-Wave tolerances. Notably 128 points need to be soldered. One is identified in figure, and (b) top and bottom views of the fabricated planar 8 × 8 antenna array (64 elements) as a single PCB before being integrated into an AiP stack-up.

(TCDAs) [18]. TCDAs are known for their large contiguous array bandwidths [18]. This bandwidth is due to the wave slow down [19] and the tight spacing between the coupled array elements. The latter leads to low angle scanning across their entire contiguous bandwidth. This is unique and the reason why TCDAs have been quite successful at nominal frequencies up to 18 GHz.

In this paper, we primarily focus on the mm-Wave fabrication of these arrays, and the challenges associated with their repeatable fabrication when the element-to-element separation is a tiny fraction of a wavelength. Still, feeding wideband arrays at mm-Wave frequencies presents numerous challenges due to the required tolerances and smaller footprints [20], [21], [22], [23]. Specifically, the typical wideband feed can no longer be connected to a set of coaxial cables due to insufficient space between the antenna array elements. Therefore, to feed a densely populated space, the antenna array elements must be properly aligned with the feeding structure [24], [25], [26], [27], [28] within the physically tight space.

At lower frequencies, of a few gigahertz, separate orthogonal components to form a complete array [29], [30], [31], [32], [33] can be used. However, at mm-Wave frequencies assembly tolerances can generate errors and inconsistencies in the resulting arrays. Specifically, thin and fragile boards are difficult to assemble, even with fine tweezers, precision soldering tips, and advanced binocular microscopes. As shown in Fig. 1, the usual assembly of separate orthogonal array elements [18], can lead to breaks and cracks due to physical assembly challenges at mm-Waves. Further, feeding an array via a microstrip or stripline feed network implies larger aperture space and higher losses, while, PCB fabrication techniques struggle with complex through plane feeds. With this in mind, our approach focuses on making the primary array feeding blocks using simple metallized vias.

The fabrication of an antenna array and feed circuit in a single step puts the approach within the context of Antenna-on-Chip (AoC) packaging [9], [20]. AoC solutions feature the integration of antennas together with other front-end circuits on the same chip using silicon technologies, such as Silicon-Germanium (SiGe). However, these solutions may experience low efficiencies due to their higher permittivity and low resistivity effects of silicon substrates (i.e., larger ohmic losses and surface waves) [25], [34], [35], [36]. By contrast, Antenna-in-Package (AiP) designs [26], [37], [38], [39] combine antennas with transceiver circuitry utilizing standard chip scale surface mount techniques, such as wire bonding [9]. AiP solutions often employ lower loss substrates, such as Low-and High-Temperature Co-fired Ceramics (LTCC and HTCC) [28], [29], [40], [41], [42], [43], [44]. AiP are also popular due to their compatibility with fine feature sizes. Still, the use of ceramic tapes, implies high dielectric constants ($\varepsilon_r > 6$) that can result in surface waves. These surface waves can be exacerbated across wideband applications. Furthermore, the expensive lamination process occurs at extremely high temperatures, resulting in active devices that must be packaged separately and connected after the firing process. To the contrary, our approach employs an AiP stack-up solution using low-loss connections between the feed circuitry and antenna array (secured at significantly lower temperatures). Additionally, the fabrication of the stack-up components employs low-cost PCB manufacturing methods [45], [46], [47], [48].

In this paper, we realize in-house a tightly coupled dipole antenna array prototype by utilizing vertical feeding through the use of a ball-grid-array (BGA) along with standard low-cost PCB manufacturing and assembly processes at mm-Wave frequencies (60 GHz region). By optimizing the BGA assembly, size, curing, paste composition, and attachment process, a repeatable array and feed layer mating was achieved. Indeed, this AiP integration enables significant aperture size reduction. Further, we avoid complications noted in previously fabricated 60 GHz antennas that employ Polytetrafluoroethylene (PTFE) materials or LTCCs. By contrast, the developed assembly process utilizes commercially available equipment and requires minimal setup while avoiding clean room conditions. As a result, the assembly process provides a durable and repeatable design and assembly process suitable across a wideband frequency range at remarkably low-cost. By following this process, we overcome the usual short-curing and spillover issues associated with BGAs at mm-Wave frequencies. In summary, our approach avoids fabrication errors and inconsistencies in the resulting arrays. The fabricated prototype is robust, electrically small and of very low cost as compared to previously published work. The realized AiP prototype operates from 55 GHz to 64 GHz. Measurements show agreement with simulation, providing for proof of concept.

In summary, the AiP approach and prototype is realized by first designing an 8 × 8 antenna array. The

design achieves: 1) fabrication with low-cost standard PCB methods, and 2) compatibility with vertical integration employing BGA solder sphere connections. After describing our assembly process, the feed board topology is discussed for integration in the AiP stack-up. This is followed by the AiP prototype and measurements verification. The proposed fabrication process is summarized as follows:

(1) Fabrication of the planar multi-layer antenna array and feed board, comprised of Isola Tachyon 100G substrates. Both utilize simple metallized vias of 6 mils diameter and optimized for efficient vertical feeding within a minimal footprint.

(2) Precision placement of thermally stable conductive solder paste and 500 μm diameter BGA solder spheres on 300 μm diameter signal pads. A 200 μm thick strip is etched around the signal pad to prevent its contact with the ground plane and 550 μm separate each BGA solder sphere from the adjacent.

(3) The Shuttle Star BGA Rework Station's (RWSV550) color optical alignment system is used to pick up, align, and place the mm-Wave array on the vertical BGA solder spheres.

(4) The conductive solder paste within the now stacked AiP aperture is cured (heated), following a reflow profile to ensure structural integrity and required electrical connections. A 'reflow profile' consists of exact times and durations with corresponding temperatures, so that the conductive solder paste is cured properly. A constant force of approximately 0.275 lbf was maintained during the curing process to hold the stack-up in place and secure for strong electrical connections.

The paper is organized as follows. Section II presents the AiP design process, detailing the antenna array, feed board, and assembly process. Section III focuses on fabrication, testing, and measurement of the final prototype. Concluding remarks are given in Section IV.

II. ANTENNA-IN-PACKAGE PROTOTYPE DESIGN

We adopt a layered approach design. First, we analyze the mm-Wave array aperture following the approach in [48]. The feed board is subsequently designed for vertical package integration. Thirdly, the assembly process for the Antenna-in-Package prototype is detailed.

A. MILLIMETER WAVE ARRAY DESIGN

The presented antenna array incorporates an 8 × 8 collection of individual dipole antennas arranged appropriately to induce capacitive coupling [49]. Each antenna array element is identical, and spaced $\lambda_{High}/2$ from each other (λ_{High} is the wavelength at 64 GHz, the highest frequency of operation). The antenna array employs three copper layers hosted by two Isola Tachyon 100G ($\varepsilon_r = 3.02$, $\tan\delta = 0.0021$) substrates, each of 18 mils thick. The fabricated 8 × 8 prototype can be seen in Fig. 1(b), and measures 17.2 mm × 17.2 mm × 1.18 mm.

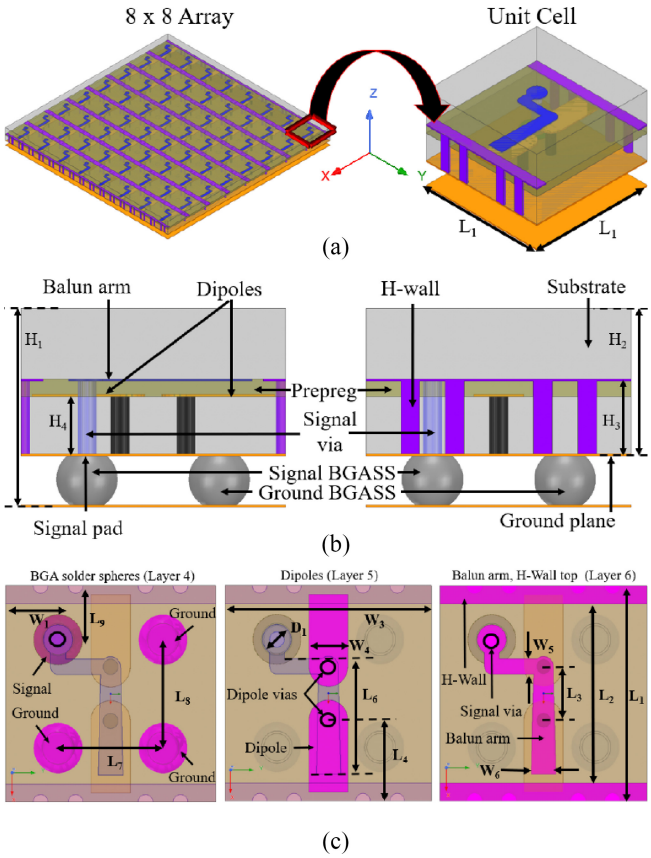

FIGURE 2. Design details of the developed mm-Wave array (top part of the AiP stack-up in Fig. 4). Specifically, (a) simulation models of the 8 × 8 array (left), and its unit cell (right), (b) side views of the unit cell in the XZ plane (left), and YZ plane (right) with design features labeled, and (c) top views of the antenna array unit cell simulation model with highlighted design features for clarity, and labeled design parameters, All vias have a diameter of 6 mils. As labeled: 'BGASS' refers to a BGA solder sphere. Layer details are shown in Fig. 4. Design parameter values can be found in Table 1.

An antenna array is intentionally designed to cover the commercial mm-Wave band of 55 GHz to 64 GHz. Simulations were completed assuming an infinite periodic array structure (unit cell) followed by a finite array analysis (see Fig. 2), using the Ansys High Frequency Structure Simulator (HFSS) software. The proposed design builds on previous work in [50]. Specifically, a balun that comprises a series open stub and a shunt short circuit is employed to feed the dipole. The folded open stub excites the dipoles with coupled vias acting as transmission line feeds. Due to the small unit cell size and through plane nature, simple twin-wire transmission lines were used for the feed. Space permitted, large groups of vias could be used to emulate a waveguide or coax cable feeding. We utilize a pair of vias labeled 'V_2' & 'V_3' to connect the dipole arms to the ground plane, thus creating the required short circuit. Similarly, a third signal via, labeled as 'V_1', is used to construct the folded open stub in Fig. 3. In turn, the folded open stub excites a balanced mode in the two vias connecting the dipole arms. In essence, the presented balun is a miniaturized version of the Marchand balun [50], implemented through vias. The balun arm travels over one dipole, crosses the dipole gap

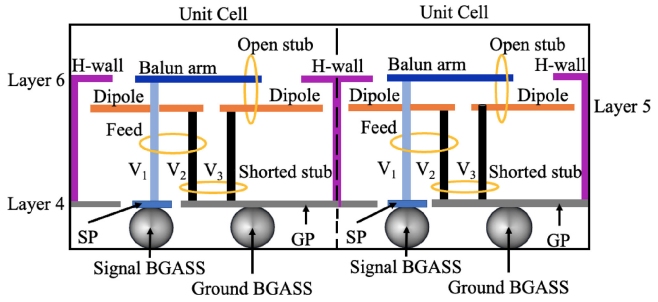

FIGURE 3. Illustration showing two neighboring unit cells of the mm-Wave array of Fig. 2 in side view (XZ plane), key design features and tuning elements (circled in yellow). Every unit cell is identical, and is roughly spaced $\lambda_{High}/2$ (where λ_{High} is the wavelength at the highest frequency of operation, 64 GHz). All vias have a diameter of 6 mils. As labeled: 'SP' refers to a signal pad (i.e., connection point for signal transmission from input port to the ballun), 'GP' refers to the ground plane, and 'BGASS' refers to a BGA solder sphere. Layer details are shown in Fig. 4.

and overlaps the adjacent dipole. Furthermore, vias forming an H-wall are positioned perpendicular to the dipoles at the edge of the unit cell to suppress cavity resonances occurring within the band [50]. The H-wall vias are connected across the top, generating a capacitive coupling mechanism among the adjacent dipoles cancelling the ground plane inductance. As such, the aperture impedance becomes real, increasing the operational bandwidth. The connection across the top of the H-wall also mitigates monopole-like radiation from the vias. Notably, fabrication tolerances align with standard practices discussed in [51] (i.e., via size, aspect ratio, pitch, pad size).

Simulation models of the 8 × 8 antenna array and the infinite antenna array unit cell are displayed in Fig. 2(a). Side views of the unit cell with labeled design features are shown in Fig. 2(b). For clarity, top view of the array unit cells with highlighted design features and labeled design parameters, are shown in Fig. 2(c). The final design parameter values can be found in Table 1. An illustration showing a side view of two neighboring array unit cells with key design features and tuning elements (circled in yellow) can be seen in Fig. 3. The authors note that simulations show a VSWR < 2 across the entire operational band (not shown for brevity). As labeled: 'SP' refers to a signal pad, 'GP' refers to the ground plane, and 'BGASS' refers to a BGA solder sphere. The AiP stack-up with substrate layers, material, and thickness details can be seen in Fig. 4.

The proposed antenna array differs from past published mm-Wave arrays [50], [52] in its feeding approach and improved low-cost stack-up. The array is intentionally optimized within the commercial 5G communication band (55 GHz - 64 GHz). Therefore, low-cost implementation is a key goal, leading to the stack-up proposed in Fig. 4. Specifically, we avoid very low dielectric constant Polytetrafluoroethylene (PTFE) materials that led to out-of-tolerance vias and shifted features. Costly buried and micro vias are also avoided. Further, the balun signal via is offset to achieve maximum BGA solder spheres population, ensuring sufficient grounding and necessary structural stability.

TABLE 1. Design parameter values of the final realized AiP prototype.

Parameter	Dimension (mm)	Parameter	Dimension (mm)
W_1	0.54	L_1	2.15
W_2	1.08	L_2	1.79
W_3	2.15	L_3	0.54
W_4	0.41	L_4	0.81
W_5	0.15	L_5	0.92
W_6	0.25	L_6	1.15
H_1	1.65	L_7	1.08
H_2	1.17	L_8	1.08
H_3	0.52	L_9	0.54
H_4	0.50	S_1	0.35
H_5	0.66	S_2	0.38
D_1	0.29	S_3	0.28
		S_4	0.34

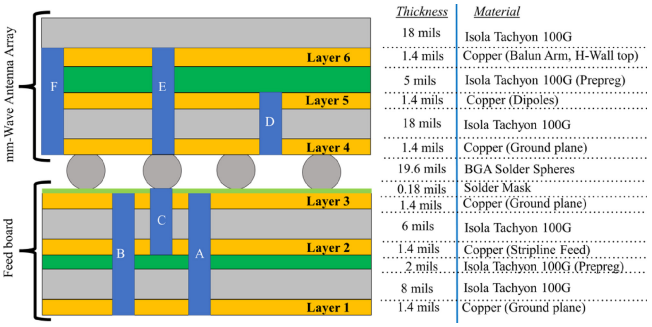

FIGURE 4. Illustration of the AiP stack-up. As labeled: ('A') microstrip to the stripline transition, ('B') shielding vias (via fence), ('C') feed board element signal via, ('D') dipole vias, ('E') balum arm via (antenna array element signal via), and ('F') H-wall vias. ('C') via transfers the signal from feedboard to the array element through ('E') via and a Signal BGA solder sphere (BGASS). Connection with the BGASS is achieved using Signal Pads (SP). Materials with corresponding thicknesses are also provided.

Each of the 8 × 8 antenna array elements is fed from beneath the signal BGA solder sphere by a 50Ω lumped port excitation as depicted in Fig. 4. The simulated broadside gain, radiation efficiency, and radiation patterns are presented in Figs. 5, 6, and 7 respectively. Notably, the broadside realized gain closely tracks directivity across the operational bandwidth (see Fig. 5). Further, a radiation efficiency of 97% is achieved across the operational band (see Fig. 6). A main beam realized gain value of 21.14 dBi is observed at 63 GHz, and is approximately 13 dB greater than the highest side-lobe level (see Fig. 7). It should be noted that while the antenna inter-element distance has been kept at $\lambda_{High}/2$ (λ_{High} is the wavelength at 64 GHz), some performance at the higher frequency end was sacrificed in order to achieve required fabrication tolerances and realize a repeatable, low-cost assembly process. Therefore, gain slightly drops above 63 GHz.

B. FEED BOARD DESIGN

A key aspect of the AiP stack-up is the feed board design. The developed fabricated feed board prototype is shown in Fig. 8 and measures 66 mm × 43 mm × 0.5 mm. As

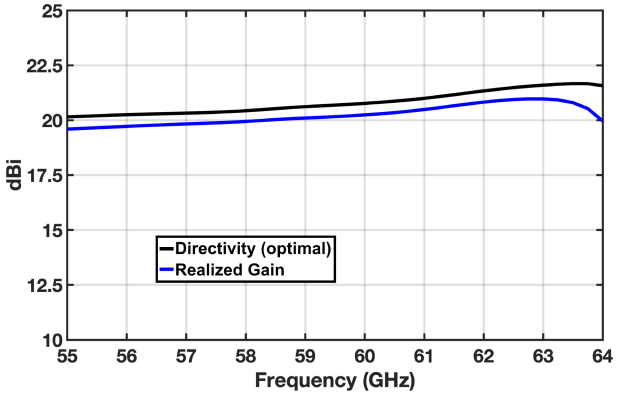

FIGURE 5. Simulated broadside gain of the 8 × 8 antenna array before integrating the BGA solder board connections and feed board.

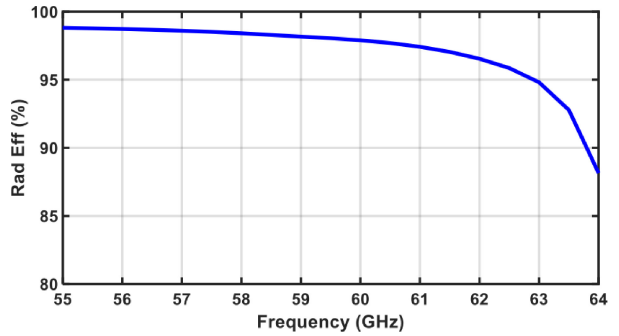

FIGURE 6. Simulated 8 × 8 antenna array radiation efficiency (%) before integrating the BGA solder board connections and feed board. An average radiation efficiency of 97% is observed across the operational band.

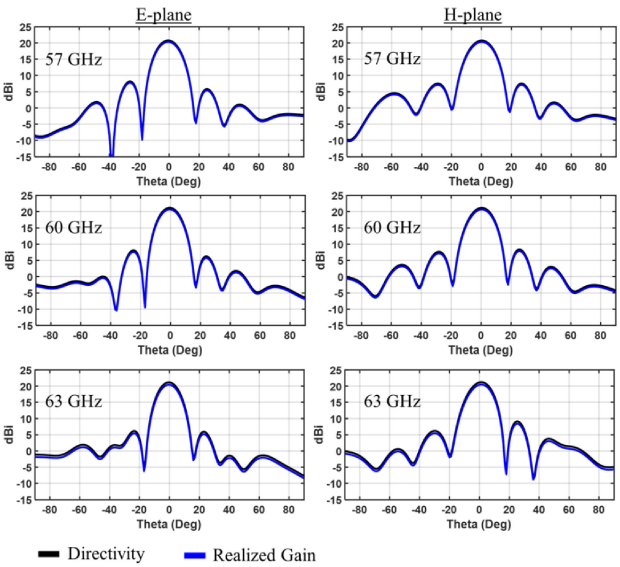

FIGURE 7. Simulated 8 × 8 antenna array radiation patterns before integrating the BGA solder board connections and feed board in the E-/H-planes at 57 GHz, 60 GHz, and 63 GHz.

labeled, 'AE' refers to the alignment edges, 'SP' labels the signal pad, and 'GPF' refers to the feed board top ground plane layer.

The feed board design must satisfy the restrictions to 1) be realized in a planar aperture using standard PCB methods,

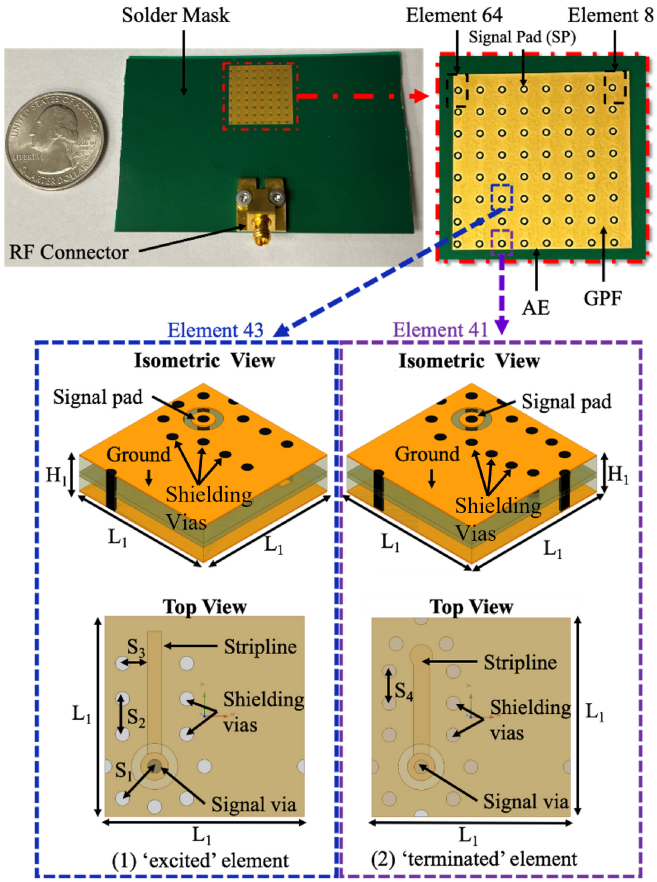

FIGURE 8. Top view of the fabricated feed board prototype (right below the BGA solder spheres (BGASS) in Fig. 4). The feedpad array at the top right is zoomed below to expose the shielding vias at the bottom of the figure. Two of the 64 feed board elements are detailed: (1) 'excited,' and (2) 'terminated.' The signal pad and the stripline feeding, shown at the bottom of figure, are protected by a 'metallic wall' of shielding vias. These feed board signal vias are represented by the letter 'C' in Fig. 4. Also the feed board shielding vias are represented by the letter 'B' in Fig. 4. All vias are shown as black in the 3D model for clarity. All vias are 6 mils in diameter and the signal pad is 300 μm in diameter. A 200 μm thick strip is etched around the signal pad to prevent its contact with the ground plane. Further layer details can be seen in Fig. 4 along with parameter values in Table 1.

2) concurrent excitation of as many antenna array elements as possible, 3) compatibility with BGA solder spheres connections, and 4) incorporation of high RF connector(s). To this end, the chosen top level feed board components include: 1) microstrip to stripline transition(s), 2) shielded stripline corporate feed network(s), and 3) an 8 × 8 element grid pattern mirroring the antenna array. The exact design of these components was not set until the capabilities of the assembly process was further investigated (discussed later). Notably, the proposed feed board structure provides compatibility with standard antenna array measurement practices, as well as the capability to implement multiple feed boards (consisting of various feed network designs).

Two different feed board elements are designed, an 'excited' feed element, and a 'terminated' feed element. In this manner, the feed board element grid configuration can be adapted for other feed networks. In other words, each of the 64 feed board elements can be modified ad-lib within

the simulation model to be either an 'excited' or 'terminated' element. Both feed board elements were modeled as a periodic unit cell model in an infinite array setup. The 'excited' feed element achieved a VSWR < 1.78 across the operational bandwidth, and the 'terminated' feed element is matched to 50Ω. Both the 'excited' and 'terminated' feed board elements are depicted in Fig. 8.

Each unit cell, matching the footprint of the corresponding antenna array element, consists of three copper layers hosted by two Isola Tachyon 100G ($\varepsilon_r = 3.02$, $\tan\delta = 0.0021$) substrates of 6 mils and 8 mils thickness (top and bottom layer) respectively. Shielding vias (forming via fences) were used to minimize losses through the feed network by confining RF fields [53]. The final design parameter values can be found in Table 1. Also, the AiP stack-up is provided in Fig. 4.

C. ASSEMBLY PROCESS FOR THE AIP INTEGRATION

To achieve the desired AiP stack-up, the antenna array is mated to the feed board using the Chipquick TS391LT thermally stable conductive solder paste (Sn42/Bi57.6/Ag0.4). The Chipquick BGA solder spheres were 500 μm in diameter (SMD2040-25000). Test trials were first completed to develop, optimize, and validate the assembly process.

The assembly was carried out in four phases:

Phase I: Place conductive solder paste on the antenna array and feed board at signal and ground BGA solder sphere positions. A 200 μm thick strip is etched around the signal pad to prevent its contact with the ground plane. If the conductive solder paste overflows, it could cause shorting upon curing. At the same time, if not enough conductive solder paste is used, the connection securing the BGA solder sphere will be brittle and fracture.

Phase II: The Shuttle Star BGA Rework Station (RW-SV550) is employed to pickup, align, and place the BGA solder spheres on top of the previously placed conductive solder paste on the feed board. The Rework Station, along with other key tools, can be seen in Fig. 9. During this process, the BGA solder spheres were placed precisely, and in a predefined order to avoid shorting with the ground plane and/or other BGA solder spheres. Each BGA solder sphere was only separated by approximately 550 μm in the x-, and y-directions.

Phase III: Once sufficiently populated, aligning, lowering, and securing the array on top of the feed board is achieved per the alignment tool and suction pad of the Rework Station. The alignment tool consists of a color optical system with functions of split vision, zoom in/out and micro-adjust. Notably, extreme care was taken during alignment to ensure precision placement. Also, a modest pressure of 0.275 lbf was maintained to hold the stack-up exactly in place and, thus, to secure strong connections during curing (see Fig. 10). It is important to note that if the suction pad is raised before the conductive solder paste has fully cured, the force from the released pressure will result in a shift, leading to possible shorted connections.

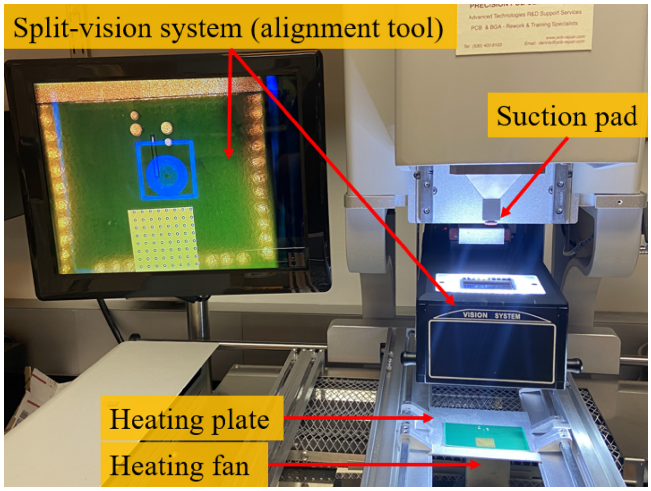

FIGURE 9. Assembly process for the AiP Integration: the Shuttle Star BGA Rework Station (RW-SV550) with key tools labeled.

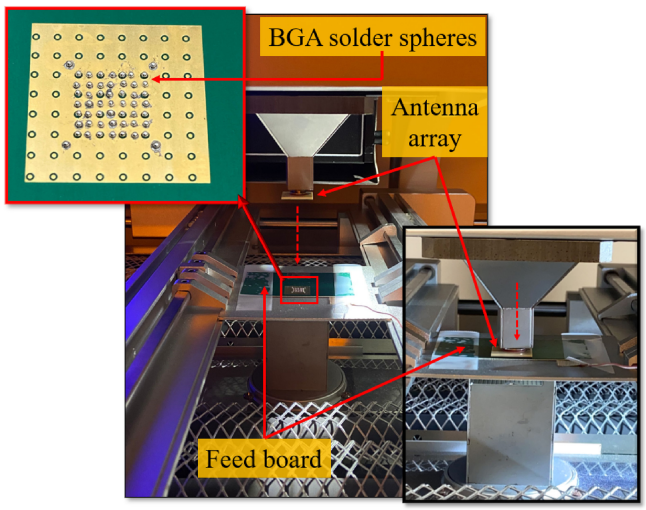

FIGURE 10. Assembly process for the AiP Integration: the antenna array being aligned, lowered, and mated to the feed board. The BGA solder spheres (BGASS) populated on the feed board element grid are also shown (top left).

Phase IV: A programmable heating fan was used to cure the conductive solder paste (causing it to harden like cement). In doing so, the feed board was mated with the antenna array, forming the realized AiP prototype, as seen in Fig. 11. The Rework Station programmable heating fan was positioned under the heating plate and the plate's temperature is monitored by a thermistor, per the reflow profile shown in [54]. This way, the solder paste is properly cured (see next Section). Trial test runs where the reflow profile was not followed, resulted in weak and half cured connections (i.e., degrading impedance matching performance and structural stability).

III. ANTENNA-IN-PACKAGE PROTOTYPE

Due to the manual process followed in a laboratory environment, we opted to feed only the central 4 × 4 array. Hence, only the center 16 feed board elements and corresponding

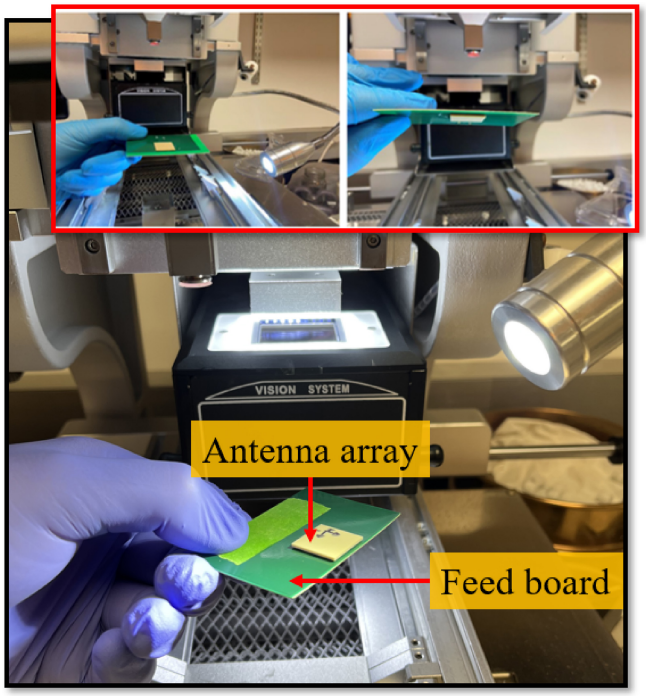

FIGURE 11. Multiple AiP prototypes assembled during initial trails. The AiP stack-up is also shown flipped upside down to display successful mating through BGA connections.

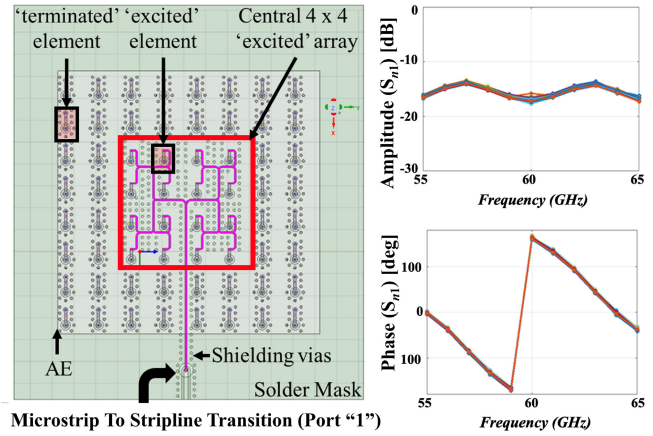

FIGURE 12. Illustration (not to scale) of the feed board with highlighted feed network signal paths (left). The microstrip to stripline transition via is represented by 'A' in Fig. 4. The letters 'AE' refer to the two sides of the feed board element grid that have additional solder mask to aid alignment during assembly. The transmission coefficients S_{n1} plots are shown to the right. S_{n1} refer to the S parameters from port 1 to each of the central 16 'excited' elements (namely n ports). The simulated curves at the top right indicate that the transmission losses are around 16dB for all elements. Also the phase transmission coefficients are same for all elements.

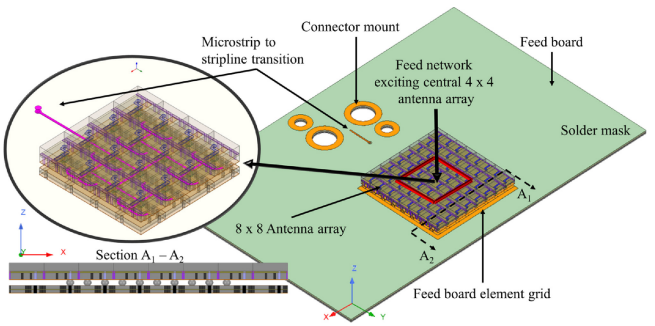

FIGURE 13. Simulation model of the partially populated 8 × 8 antenna array vertically integrated onto the feed board. A zoomed view of the center 4 × 4 AiP element stack-up, with the feed network highlighted is also shown. Shielding vias are not shown for clarity. A cross section side view of the 8 × 8 element AiP stack-up displays the absent outer element BGA solder spheres (BGASS).

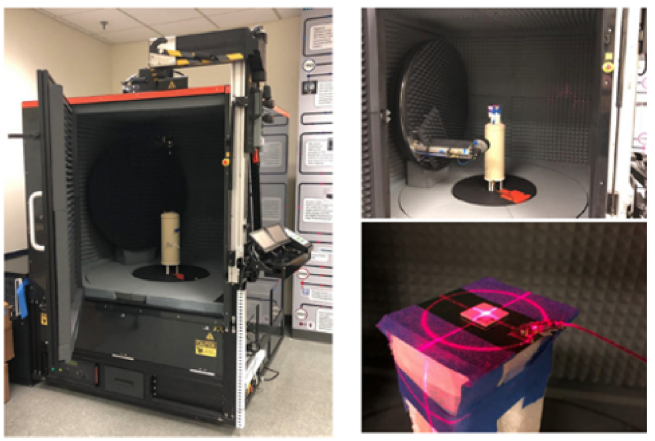

FIGURE 14. Millimeter-wave μ-lab chamber anechoic chamber with the AiP prototype during measurements.

ground connections were mated. The other 48 feed board elements are not populated with BGA solder sphere connections and therefore not mated to the antenna array. This trade-off does affects the antenna array's performance, but allows monitoring of select connections following standards and practices per [55]. Additionally, a partially populated element grid provided a more uniform heat distribution matching the required solder paste reflow profile seen in [54]. The reflow process is comprised of four 'zones': 1) preheating, 2) soak, 3) reflow, and 4) cooling. These steps are critical to ensure that sufficient solvents evaporate, flux is activated, thermal stresses are avoided and excessive flux oxidation/burning is suppressed [56], [57], [58]. Numerous brittle, fractured, and partially cured connections were seen during trials when the feed board was fully populated with BGA solder spheres. Also, minimizing temperature differences (i.e., hot and cold spots) on the feed board was essential, but difficult due to significant footprint differences between the heating fan, heating plate, and the feed board element grid. Nevertheless, assembly in a controlled industrial environment and with a well defined automated process is expected to be robust.

The optimized re-flow profile [59] that produced favorable results in our laboratory set-up is summarized as follows:

(1) The preheating zone brings the solder paste from 20 °C (68 °F) to 133 °C (266 °F) in 180 sec. The purpose of preheating is to allow the solvents to evaporate and activate the flux.

(2) The soak zone brings all board areas to an equal level. The temperature rises from 133 °C (266 °F) to 138 °C (281 °F) at 30 sec.

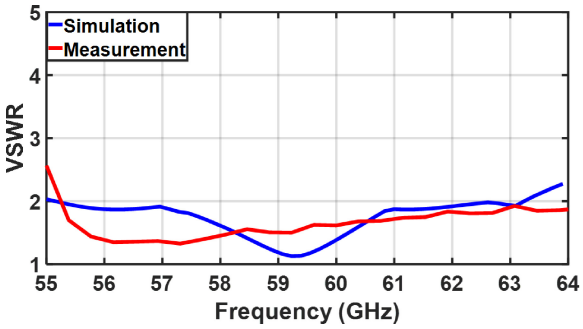

FIGURE 15. Measurements vs simulations of embedded VSWR curves for the final realized AiP prototype. Embedded results convey the performance of the antenna array (with the center 16 elements excited), BGA solder sphere connections (BGASS), and the feed board.

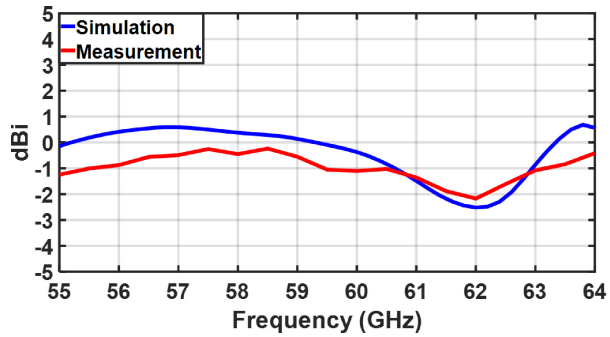

FIGURE 16. Measurements vs simulations of embedded broadside gain for the final realized AiP prototype. Embedded results convey the performance the antenna array (with the center 16 elements excited), BGA solder sphere (BGASS) connections, and the feed board.

(3) The reflow zone reaches a maximum temperature of 165 °C (329 °F). Lasting a total of 100 sec (from 210 sec to 310 sec), with the maximum temperature being held for 40 sec within that duration.

(4) The cooling zone, lasting from 310 sec to 600 sec to bring the temperature gently back to 20 °C (68 °F). Free air cooling was found to be sufficient.

Opting to feed only the central 4 × 4 array, leads to a fabricated feed board consisting of the following: 1) a single microstrip to stripline transition, 2) a shielded 1-to-16 stripline corporate feed network, and 3) an 8 × 8 element grid constructed from 16 central excited, and 48 outer terminated elements. Notably, each feed board element is oriented to mirror the antenna array's element grid pattern (i.e., aligning signal pads). The aforementioned microstrip to stripline transition connects a Rosenberger RF connector (01K80A-40ML5) to the feed network. This transition is a through via, and serves to verify that the RF connector is electrically connected to the feed board (labeled as 'A' in Fig. 4). The connector is mounted to the feed board using screws and dowel pins.

The fabricated feed board prototype, seen in Fig. 8, measures 66 mm × 43 mm × 0.5 mm. As labeled, 'AE' refers to the two sides of the feed board element grid that have additional solder mask, providing an alignment template during assembly. Remarkably, the feed board top ground plane layer is left mostly uncovered by solder mask within the 8 × 8 element grid footprint to allow for ground BGA solder sphere population. An illustration of the realized feed board model, with simulation, is provided in Fig. 12. The illustration is not to scale, and the feed network signal paths are highlighted, for clarity. Shielding vias (via fences), feed board element type ('excited' or 'terminated'), and the microstrip to stripline transition, are shown and labeled. The transmission coefficients S_{n1} plots are shown in Fig. 4. S_{n1} refer to the S parameters from port 1 to each of the central 16 'excited' elements (namely n ports). The simulated curves indicate that the transmission losses are around 16dB for all elements. Also the phase transmission coefficients are same for all elements.

Subsequently, the 8 × 8 fabricated antenna array is set onto the feed board, forming the AiP prototype. For comparison we simulated the finite array by removing the dummy elements from the model. The AiP simulation model, with a cross section side view of the 8 × 8 AiP stack-up can be seen in Fig. 13.

Measurements were carried out in a MVG μ-lab mm-Wave chamber, shown in Fig. 14. Simulation and measured impedance as well as broadside gain curves are given in Figs. 15 and 16, respectively. Radiation patterns are provided in Fig. 17. The simulated and measured results are embedded. That is, they provide the performance of the final realized AiP prototype that includes the antenna array, BGA solder sphere connections, and the feed board impact. The measured broadside gain (embedded) closely tracks simulations. A drop at 62GHz is seen for both the simulated and measured results. This is not due to the antenna itself but rather an effect of the feed board. This becomes clear after inspection of Figs. 5, 6. Notably, the array exhibits high efficiency (> 85%) across the whole band, including frequencies around 62 GHz. At the same time, neither the simulated gain of the antenna array (de-embedded simulated results) nor the VSWR deteriorate at 62 GHz. Thus, it can be inferred that the drop in the embedded gain is associated with radiation losses from the feeding board. The above does not contradict the very low VSWR, since the radiated power from the feed board is not delivered to the antenna elements and therefore is not added to the reflected power. Notably, the measured VSWR shows good agreement with simulations, achieving a VSWR < 2 across most of the operational band. Importantly, the measured radiation pattern agrees with simulations, verifying the AiP assembly. The slight variations in broadside gain and in the E-/H-plane radiation patterns are due to the asymmetric unit cell, and the non-automated conductive solder paste placement. The gain of the final simulated AiP prototype is found to be 0.59 dBi at 57 GHz. Certainly, this is lower than the simulated gain of the isolated 8 x 8 antenna array (see Fig. 5). This is mainly due to the losses of the stripline corporate feed network. Additional losses in the measured prototype are introduced by the solder paste. In fact, the stripline corporate feeding network was chosen to allow for low-cost

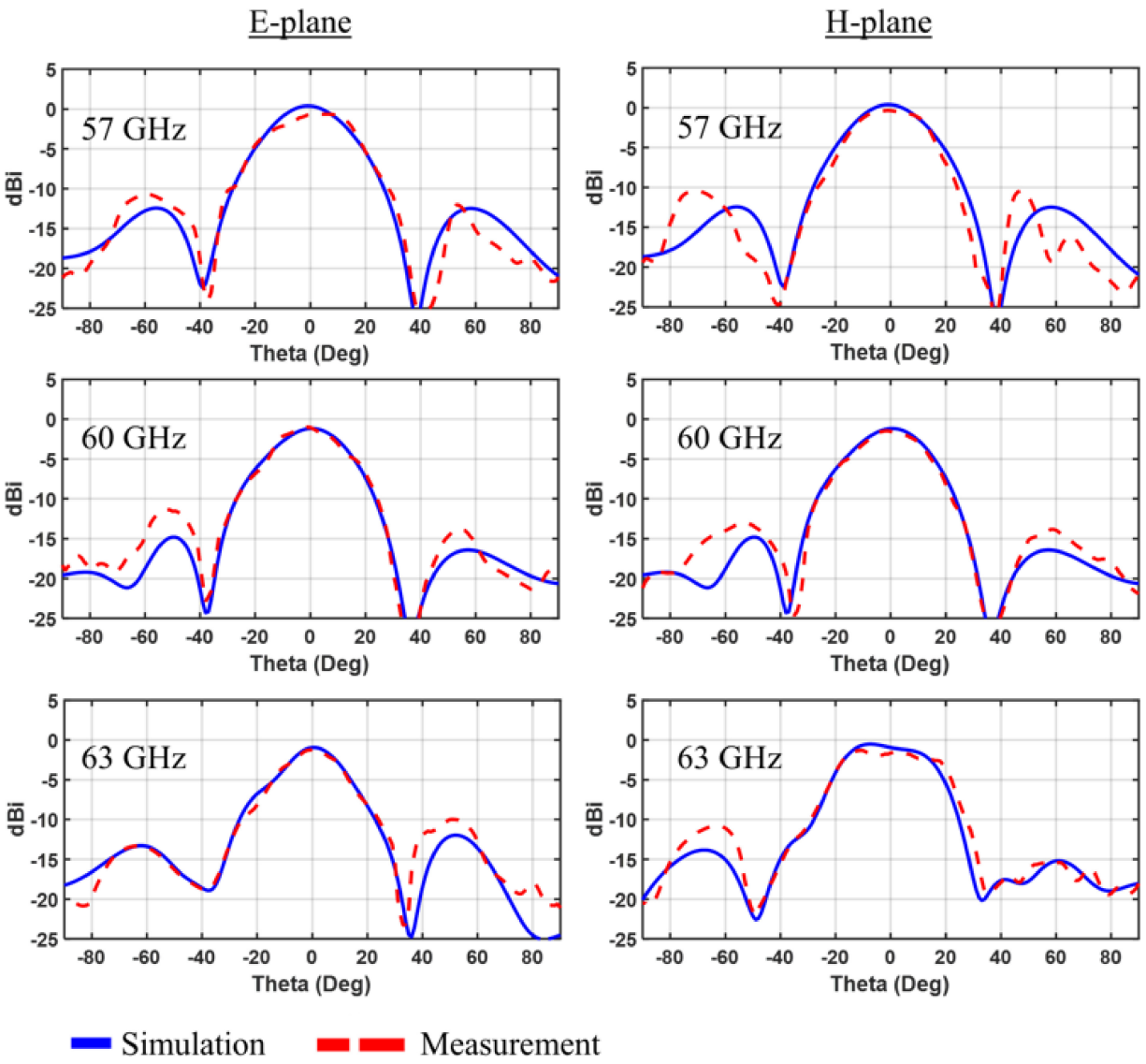

FIGURE 17. Simulated and measured embedded radiation patterns for the final realized AiP prototype, in the E-/ H-planes at 57 GHz, 60 GHz, and 63 GHz. Embedded results convey the performance the antenna array (with the center 16 elements excited), BGA solder sphere (BGASS) connections, and the feed board.

in-house assembly, validation, and measurement. Certainly, on-chip integration at an industrial level could reduce losses. Further, feed structure optimization could improve efficiency and bandwidth performance. This would allow for exploiting the wideband behavior of TCDAs to a greater extend. However, this is out of the scope of the presented work.

IV. CONCLUSION

A wideband mm-Wave antenna array in an AiP stack-up was presented. The AiP stack-up approach addressed the resolution and antenna fabrication challenges associated with feeding such tightly populated arrays. A Rework Station and an optimized curing process were employed to realize the AiP fabrication. The 16 center excited feed board elements were mated to the antenna array using conductive solder paste and BGA solder spheres. Measured performance agreed quite well with simulations. In all, this work leverages available wideband array designs to develop and verify an AiP fabrication process for mm-Wave apertures. The fabricated beamforming arrays included individually fed array elements using readily available low-cost equipment.

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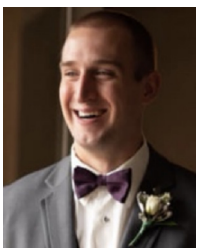

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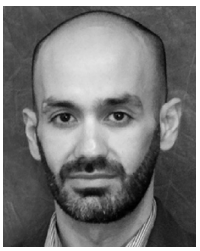

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