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Broadband D-Band Patch Antenna Array in Wafer-Level Package Based on BCB Process

XIAOCHENG WANG (Graduate Student Member, IEEE), GAOBIAO XIAO (Senior Member, IEEE), LIXUE YANG, HAO LI, AND QIHAO XU

Key Laboratory of Ministry of Education of Design and Electromagnetic Compatibility of High-Speed Electronic Systems, Shanghai Jiao Tong University, Shanghai 200240, China

CORRESPONDING AUTHOR: G. XIAO (e-mail: gaobiaoxiao@sjtu.edu.cn)

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ABSTRACT This paper presents a broadband stacked patch antenna array in wafer-level package based on benzocyclobutene (BCB) process for D-band wireless communications. The BCB material is not only used as a substrate for the antenna, but also as an interconnection layer, enabling low-loss interconnection with RFICs through vias and transmission lines. By introducing a BCB polymer-filled back cavity and carefully developing the feeding network, the designed antenna achieves a relative bandwidth of 18.9%. In addition, the 2 × 2 stacked antenna array features a stable high-gain broadside radiation pattern. The pairwise antiphase feeding technique is adopted to suppress the cross-polarization level. In order to acquire high-speed data transmission, a dual-polarization MIMO implementation is presented. The port isolations are greater than 35 dB across the whole operating band.

INDEX TERMS Antenna in wafer-level package, BCB process, D-band, patch antenna array, broadband performance.

I. INTRODUCTION

D-BAND (110 GHz-170 GHz) has a high potential for the coming 6G wireless communication systems due to its abundant spectrum resource and low atmospheric loss [1]. In recent years, several D-band transceiver chipsets with data transmission rates beyond 10 Gbit/s have been reported [2], [3], [4], in which the antenna plays an important and essential role. Since integrated antennas feature lower transmission loss compared with conventional discrete antennas [5], it is a momentous and challenging undertaking to integrate antennas and MMICs into a single system with high-quality performance. Antennas in these circumstances are required to provide wider bandwidth, higher gain, and preferably low-profile planar structures.

Integrated antennas mainly fall into two basic categories: antenna-in-package (AiP) and antenna-on-chip (AoC). Compared with AoC, AiP solution is more attractive due to its higher gain and efficiency, improved system performance, and reduced cost in sub-terahertz band [5]. In recent years, AiPs are mainly fabricated with low temperature co-fired ceramics (LTCC) [6], [7], [8], high-density interconnect (HDI) [9], [10], [11], and wafer-level package (WLP) [12], [13], [14], [15].

LTCC substrate is the most popular choice for AiP designs because of low sintering temperature, low dielectric loss, reliable thermal stability, and high mechanical strength. The multilayer structure allows for high design flexibility when it comes to packaging antennas and other passive components. Beyond 100 GHz, however, LTCC is less attractive due to the layer-to-layer alignment inaccuracy, shrinkage, and higher cost. In addition, antenna and RFICs are typically connected with standard wedge-to-wedge bonding wire or flip-chip method, which invariably results in a mismatch. More seriously, the interconnection loss has been reported to be as high as about 3 dB in D-band [16]. On the other hand, available high-frequency ceramic substrates typically have higher dielectric constant than organic materials, which is not suitable for dielectric-substrate-based antenna to realize broadband and low-profile performance.

HDI is based on the copper-clad laminates and associated buildup technology. Compared with traditional PCB technology, HDI can realize smaller vias, thinner traces,

more layers, and smaller components. Some organic materials, such as liquid crystal polymers (LCP) and Megtron 7N, have been proved to be suitable for HDI packaging solutions [9], [10], [11] at upper mm-wave band due to their stable dielectric constant and low dielectric loss. Although the mechanical strength of the integrated system can be enhanced with a core, the softness of the material may inevitably bring warpage when the antenna is integrated with active circuits, resulting in a misalignment of the multilayer structure. This influence will become more serious in D-band and may significantly affect the performance of the antenna.

WLP is to package components on the wafer-level. The die is placed on a carrier, and a thin-film redistribution layer (RDL) is employed as the routing layer to rearrange the pads of it. After that, it will be encapsulated with mold compound (MC) to form a new wafer. The antenna can be placed on the MC and connected to the die through vertical vias and microstrip lines. Compared with bonding wire and flip-chip, WLP can significantly reduce interconnection loss and improve overall system performance, especially in D-band. In addition, the thickness of the package can be greatly lowered, which contributes to improve thermal and electrical performance. However, the popular fan-out WLP process, such as embedded wafer level ball grid array (eWLB) technology [12], [13], [14], typically has restrictions on the design flexibility of antennas. It is a challenge to design a D-band broadband antenna in WLP process.

A few D-band antennas in wafer-level package have been proposed in recent years [12], [13], [14], [15]. Almost all the designed antennas suffer from narrow impedance bandwidth because of the limited space and fixed process flow. The 122 GHz antenna arrays in [12] have been realized through the eWLB process. Since there are just two RDLs employed in the design and not much space is left for antenna, achieving broadband performance is very challenging. A monopole and its array have been designed and fabricated by micromachining the low-resistivity silicon substrate, and two-layer BCB membrane is coated on the wafer [15]. To improve the antenna performance, a cavity is etched in the Si-wafer and filled with polymer. The single antenna and its array can achieve 9% (124-136 GHz) and 8.7% (126.5-138 GHz) relative bandwidth, respectively, which are relatively narrow.

In this paper, we propose a broadband low-profile stacked patch antenna array in wafer-level package based on BCB process for D-band wireless communications. Right below the antenna patch, a 60-μm-thick metal cavity is etched in the high-resistivity silicon wafer and is filled with BCB polymer. To isolate the high loss of silicon, a 4-μm-thick copper layer is electroplated as the ground, and then four BCB thin-films as interlayers are spin-coated on it. A 2 $\times$ 2 stacked patch array is designed, with a differential feeding network to suppress cross-polarization. In order to multiply the channel capacity and obtain high-speed data transmission, a dual-polarization system is implemented. Within the best of our knowledge, the broadband WLP antenna in D-band fabricating on four BCB layers is proposed for the first time. Part of the related work has been published in [17].

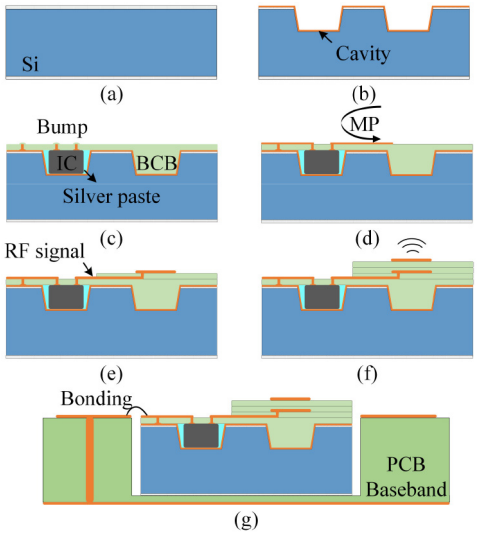

FIGURE 1. Integration process of the BCB package technology. (a) Prepared high-resistivity silicon wafer with two SiO_2 layers on both sides. (b) Etched SiO_2 windows with metal ground. (c) BCB polymer filled cavities and the embedded RFIC chip. (d) Mechanical polishing. (e) Interconnection between the antenna and RFIC on the second BCB layer. (f) Completed antenna structure. (g) Finished wafer-level package module.

The paper is organized as follows. Section II describes the BCB manufacturing process. In Section III, the designs of the D-band patch antenna array, the microstrip feeding network, and a dual-polarization MIMO implementation are presented. Section IV shows the *S*-parameters and radiation pattern measurements along with a discussion. Finally, a conclusion is presented in Section V.

II. ANTENNA FABRICATION PROCESS

BCB polymer (Cyclotene 3000 Series, Dow Chemical, 1980s) has been widely developed as spin-on dielectric materials in micro-electronic fabrication [18], [19], [20]. BCB has low dielectric constant (2.65), low dielectric loss (0.0008), and stable electrical characteristics in the mm-wave band. Fig. 1 briefly describes the fabrication process of the designed antenna in wafer-level package when connected to an RFIC.

Firstly, a 450-μm-thick high-resistivity silicon (3000-4000 Ω cm) wafer is prepared, two 2-μm-thick SiO_2 layers are deposited on both sides of the wafer by dry oxidation process (a). Secondly, the SiO_2 windows are etched to define the patterns of cavities through photolithography and buffered oxide etching process [20]. After that, the cavities are fabricated by wet or dry etching process, and the 4-μm-thick Cu is electroplated on the Si-wafer as the ground plane (b). Thirdly, the cavity for antenna is filled with BCB polymer and the surface needs to be polished. A RFIC chip is embedded and stuck on the bottom of the trench with silver paste. Next, the first BCB layer is spin-coated, and several bumps are prepared for the connection between the chip pads

and transmission lines (c). Fourthly, the flatness is improved by the mechanical polishing (MP) procedure (d). Fifthly, the second BCB layer is coated, and the interconnection between the antenna and RFIC is realized through metal blind-vias and transmission lines (e). Finally, another two BCB layers are coated one by one and the patterned parasitic patch is electroplated and then placed on the top (f). After that, the finished wafer-level package module is positioned in the bottom of the PCB cavity and connected with baseband module through standard bonding wire technique (g).

Taking account of the stability of the packaging system and the restrictions of the process, the thickness of each BCB layer has to be limited to 15 μm, and the maximum number of layers must be under 4. In addition, the dimensions of the cavity are as minimal as possible to prevent the BCB from fracturing.

III. ANTENNA FABRICATION PROCESS

A. STACKED PATCH ANTENNA ARRAY

Fig. 2 presents the configuration of the proposed patch antenna array in wafer-level package. To improve the antenna performance, a 60-μm-deep polymer cavity is formed in the Si-wafer through dry-etching process. Its perimeter and the top of the wafer are electroplated with 4-μm-thick Cu as the ground plane. Although increasing the height of the cavity is beneficial to the improvement of the antenna performance, it enhances the difficulty of processing. Furthermore, if the volume of the filled BCB polymer is too large, it can easily fracture. Therefore, instead of etching a single large cavity, two identical smaller cavities are etched below the antenna and filled with BCB polymer. Four BCB layers are spin-coated and served as the substrate, each with a thickness of 15 μm. The feeding network is on the B_1 layer and connected with the 2 $\times$ 2 square driven patch array placed on the B_2 layer through blind metal vias. The distance of the adjacent patches is 1.58 mm (0.74 λ_0, 140 GHz). In order to improve the operating bandwidth, an identical parasitic patch array is positioned on the top B_4 layer, while the B_3 layer is required and significant for improved matching of the stacked patch antennas [21]. The total dimensions of the package are 4.9 mm $\times$ 4.9 mm $\times$ (120 μm + 390 μm), consisting of the transition and Si-wafer. The profile of the package can be further reduced by wafer dicing process [22]. Therefore, the proposed WLP antenna can achieve a much lower profile performance compared with LTCC and HDI technology.

B. QUASI-COAXIAL VIA TRANSITION

A transition is required to convert the feeding network to the top layer so that the antenna can be measured on the probe station. As shown in Fig. 3(a), a grounded co-planar waveguide (GCPW) to stripline quasi-coaxial via transition is designed. To accommodate the probe pitch, the gap between the signal line (SL) and the ground is set to 50 μm. The width of the SL is set to 75 μm, achieving the port impedance close to 50 ohms in conjunction with the top and middle

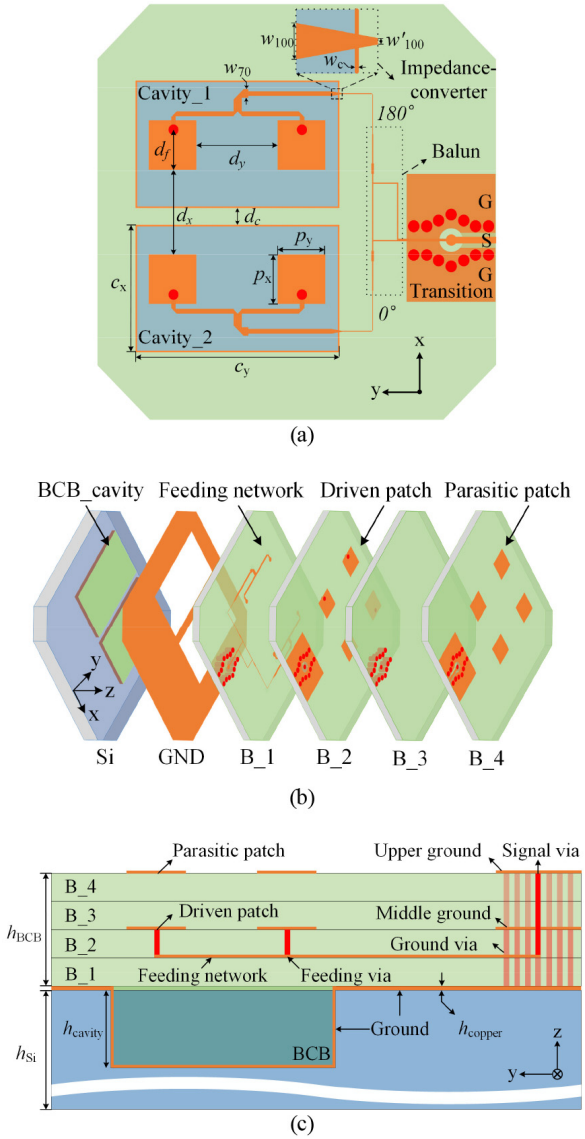

FIGURE 2. Schematic diagram of the structure of the antenna and its dimensions. (a) Top view. (b) 3D view. (c) Stack-up view. (Design parameters: w_{100} = 55, w'_{100} = 10, w_c = 4, w_{70} = 100, d_x = 1580, d_y = 1580, d_f = 470, d_c = 260, c_x = 1500, c_y = 2500, p_x = 580, p_y = 580, h_{BCB} = 60, h_{Si} = 450, h_{cavity} = 60, h_{copper} = 4. Unit: μm.).

ground layers. The ground vias play a key role in controlling the characteristic impedance of the transition and confining the field near the signal via. Their numbers and positions have to be carefully optimized in order to reduce the high-frequency transition loss and prevent unwanted parallel-plate modes by mitigating the via-plate coupling [23]. Due to the limitation of process capability, the radius of the signal-via and ground-vias are set to 65 μm and 70 μm, respectively.

The transition has been simulated and optimized using HFSS. The port impedance is normalized to 50 ohms for both port 1 and port 2. Fig. 3(b) shows the simulation results, which can be seen that a satisfactory matching is achieved and the transmission coefficient (S_{21}) is around -0.5 dB over a broad frequency range.

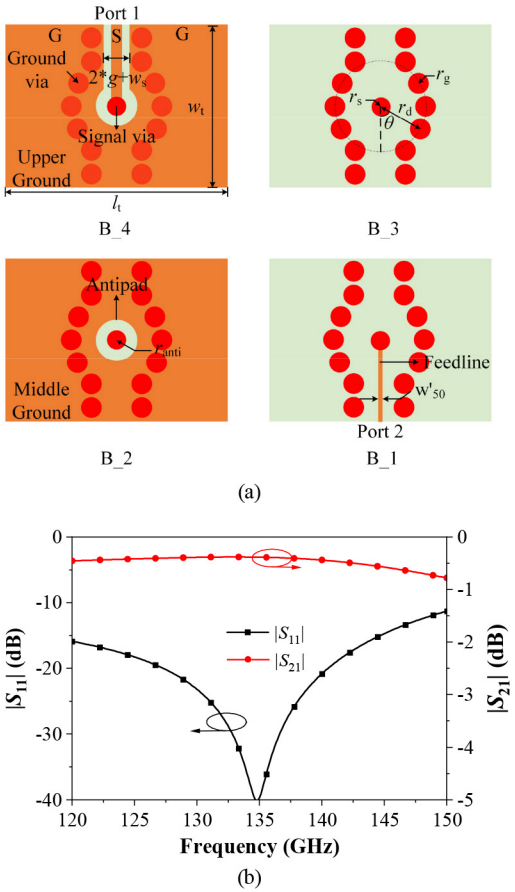

FIGURE 3. Details of the transition (a) and its simulation results (b). (Design parameters: $w_s = 75$, $g = 50$, $w_t = 1100$, $l_t = 1500$, $r_s = 65$, $r_g = 70$, $r_d = 310$, $r_{anti} = 140$, $w'_{50} = 30$, $\theta = 60$ deg. Unit: μm.).

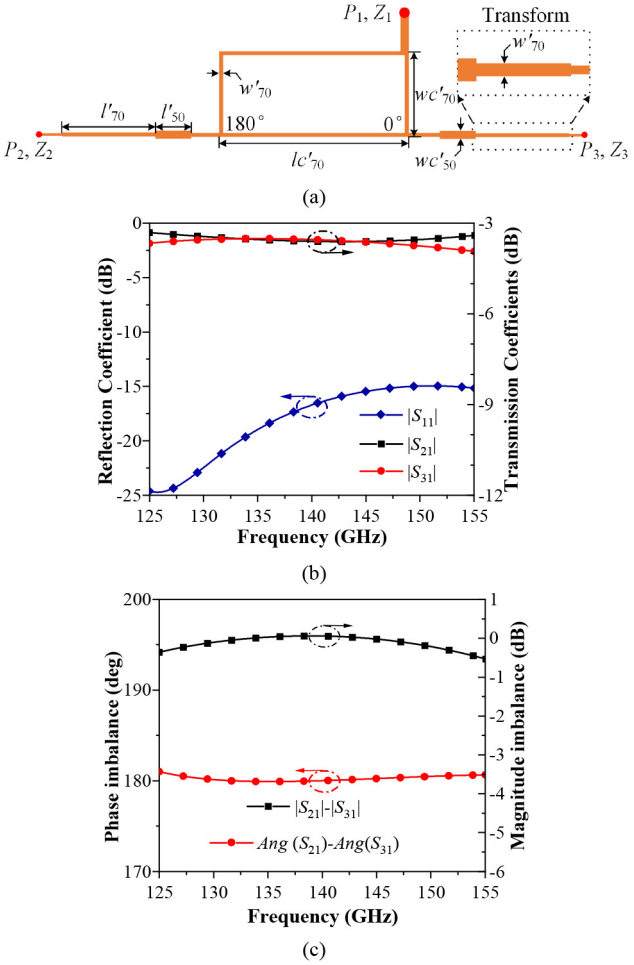

FIGURE 4. Details of the proposed balun and its simulation results. (a) Geometry and dimensions of the balun. (b) Simulation results of the *S*-parameters. (c) Simulation results of the magnitude and phase imbalance. (Design parameters: $lc'_{70} = 700$, $l'_{50} = 130$, $wc'_{50} = 30$, $wc'_{70} = 322.5$, $l'_{70} = 340$, $w'_{70} = 15$. Unit: μm.).

C. FEEDING NETWORK

Since the BCB polymer-filled cavity is positioned beneath the radiation elements, it is not possible to use a complete metal ground to shield the spurious radiation generated by the feeding network, as is the case in most antenna designs [10], [11], which is because the polymer-filled cavity will be shielded at the same time. The spurious radiation energy of the feeding network will inevitably affect the antenna pattern, especially deteriorating the cross-polarization. Therefore, the pairwise antiphase feeding technique is used to counteract the negative effects and suppress cross-polarization. The symmetry of the antenna pattern can also be improved [24].

As shown in Fig. 4(a), a balun is added to obtain two excitation currents with equal amplitude but antiphase [25]. P_1 is connected with the transition, and its port impedance Z_1 is equally 50 ohms. A $\lambda/4$ transform is used to ensure that the port impedance of P_2 and P_3 are 100 ohms. From the simulation results shown in Figs. 4 (b) and (c), it can be seen that the phase difference between the two outports of the balun maintains around 180 degrees over a wide frequency band. Meanwhile, imbalance of the magnitudes is small. The simulation results reveal that the proposed balun matches very well. As shown in Fig. 2(a), the height from the ground of the microstrip line (ML) on the right is only one-layer BCB, and its characteristic impedance is about 100 ohms. However, when the ML traverses the interface, the height from the ground will change and cause the characteristic impedance to be discontinuous, resulting in a serious mismatch and spurious radiation, especially in D-band. Therefore, we use the converter to smooth the impedance-transition and alleviate the potential influence of the discontinuity. Its dimensions are optimized and simulated. The simulated results are depicted in Fig. 5, we can observe that the converter shows a good performance and greatly improves the impedance matching.

D. DUAL-POLARIZATION MIMO IMPLEMENTATION

To multiply the channel capacity and obtain high-speed data transmission, dual-polarization MIMO (DP-MIMO) system has been utilized in several on-chip millimeter-wave transceivers [26], [27], [28]. Two orthogonally isolated polarizations can enable the simultaneous transmission of

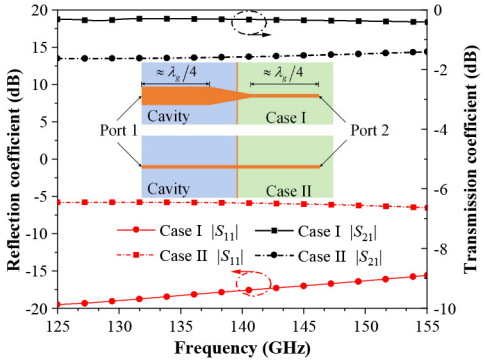

FIGURE 5. The converter and its comparison of simulation results.

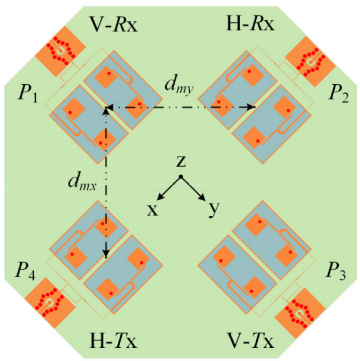

FIGURE 6. Top view of the MIMO system composed by the proposed antenna array. (Design parameters: $d_{mx} = 5$, $d_{my} = 5$. Unit: mm.).

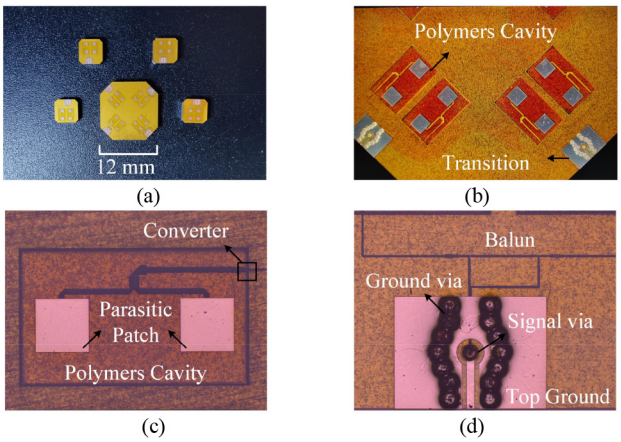

FIGURE 7. Physical diagrams of the antenna. (a) Under ordinary lens (b) DP-MIMO implementation under the microscope. (c) Partial enlarged view of antenna. (d) Transition and balun under the microscope.

two independent information channels on the same carrier signal, thereby doubling the channel capacity [26], [27]. In this application scenario, the two orthogonal antennas or dual-polarization antenna play very important roles. However, there is little research available to discuss the isolation of D-band DP-MIMO antenna arrays. In addition to broadband performance, compliant port-to-port isolation and cross-polarization discrimination (XPD) are also important

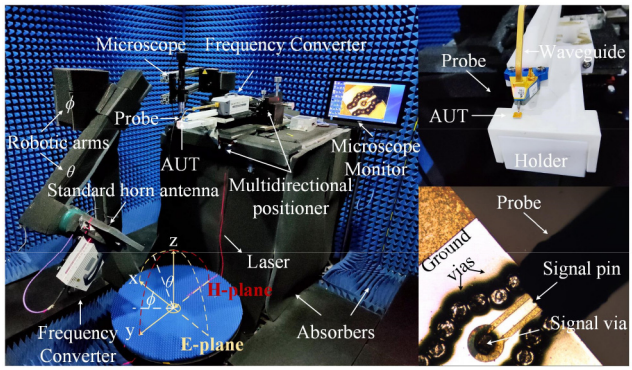

FIGURE 8. The quasi-in-air-based antenna measurement setup.

and necessary to realize well-functioning multiplexing schemes for DP-MIMO systems.

In this section, we propose a DP-MIMO implementation scheme based on the designed stacked patch array. As shown in Fig. 6, two orthogonal antennas are used for two polarized TXs or RXs. A dual- polarization antenna occupies much less package area. However, it is very challenging to realize satisfactory port-to-port isolations with the process of wafer-level package, especially in D-band. The main reason is that, in the case of extremely restricted space, it is difficult to isolate the horizontally and vertically polarized feeding networks from each other without a complete metal plane, which results in an extremely strong coupling and severely degrades isolation. In order to improve the isolation, they are deliberately separated by a predetermined distance, and the polarization of the adjacent radiation units is made perpendicular. Furthermore, the XPD is improved benefiting from the pairwise antiphase feeding technique. The simulation and measurement results of this DP-MIMO system will be shown in the next section.

IV. EXPERIMENTS AND DISCUSSION

The proposed antenna and its DP-MIMO implementation are fabricated by the BCB process mentioned in Section II, and their physical diagrams are shown in Fig. 7. To verify the design, the impedance characteristics of the antenna were measured on the probe station, and the far-field radiation performance were passively measured through quasi-in-air method.

A. QUASI-IN-AIR MEASUREMENT SETUP

Both the proposed antenna and its DP-MIMO implementation were measured through quasi-in-air method. The arrangement is depicted in Fig. 8, and a detailed description has been published in [29]. It is worth mentioning that, due to the great difficulty of testing multi-port devices, while testing MIMO antennas in anechoic chamber, one port is fed and the other ports are open rather than connected to matched loads, which may result in some inaccuracies. The influence on the far-field results can be ignorable because

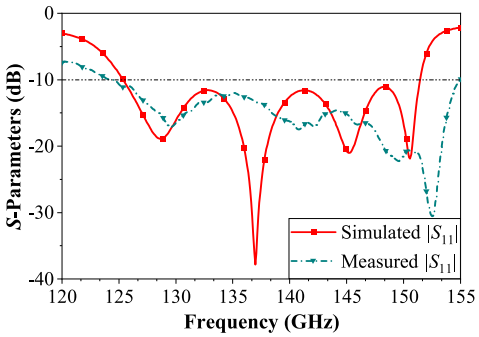

FIGURE 9. Simulated and measured *S*-parameters of the proposed antenna in wafer-level package.

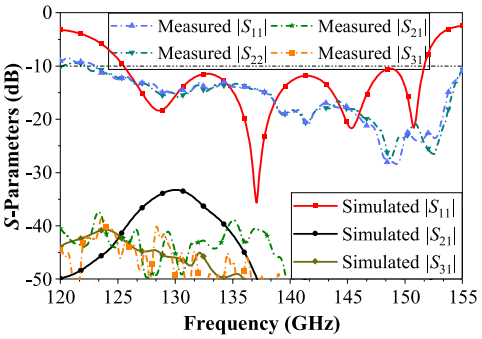

FIGURE 10. Simulated and measured *S*-parameters of the DP-MIMO system.

of the improved port isolation and the loss characteristics of the feeding network.

To accurately measure the far-field performance of the antenna, a pair of standard D-band horn antennas are required. Firstly, one standard horn antenna is served as the receiving antenna, and the other one with known maximum gain G_0 is utilized as the transmitting antenna. The power of the signal received from the vector network analyzer (VNA) is P_0. After that, the antenna under test (AUT) will take over as the transmitting antenna, and the received power is P_A. Therefore, considering the loss P_L of the D-band probe, the gain of the AUT can be calculated by the following formula:

$$G = G_0 + (P_A - P_0) + P_L \tag{1}$$

In addition, the receiving horn antenna can be rotated for different polarizations.

B. S-PARAMETERS

The measurement and simulation results of the proposed antenna in wafer-level package are compared in Fig. 9. The errors are mainly caused by the fabrication process and the measurement. The additional losses caused by metal surface roughness of the feeding network are difficult to be justified in the simulation. This may be the main reason that the measured S_{11} has a lower level and a larger bandwidth than the simulated results [30], [31]. The simulated and measured bandwidths (−10 dB) of the antenna are 18.9% (125.3-151.5 GHz) and 22.2% (124-155 GHz) respectively.

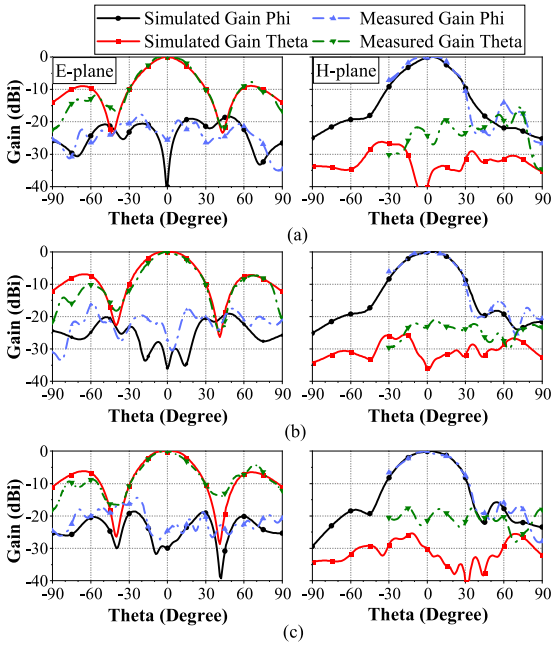

FIGURE 11. Simulated and measured results of the antenna pattern in E and H plane. (a) 135 GHz. (b) 140 GHz. (c) 145 GHz.

The main benefits are as follows: firstly, the advanced 4-layer BCB packaging technology brings a higher degree of flexibility to the antenna design compared with other wafer-level package process [12], [13], [14], [15]. Secondly, the BCB polymer-filled back cavity increases the thickness of the substrate. Thirdly, the feeding network is carefully developed.

The *S*-parameters of the DP-MIMO system are shown in Fig. 10. Since the entire topology of the antenna exhibits complete rotational symmetry, only one port is presented for the sake of brevity. It can be seen that the reflection coefficient is similar to the single-port array because of the low coupling among the ports. The port isolations between adjacent ports are higher than 35 dB in almost the entire operating frequency band.

C. FAR-FIELD RADIATION PERFORMANCE

The normalized radiation E and H plane patterns at 135 GHz, 140 GHz, and 145 GHz are shown in Fig. 11. The radiation patterns of proposed single-port antenna array and its DP-MIMO system were both simulated and measured, only the patterns of the DP-MIMO system are shown here since they are very similar. Benefit from the pairwise antiphase feeding technique, the cross-polarization is significantly suppressed in the maximum radiation direction of the antenna. From the measurement results, we can observe that the main lobe curve agrees well with the simulated results. The left side of the E-plane patterns shows a slight distortion, which may be caused by the radiation of the probe. However, the measured cross-polarization of the antenna is not as good as predicted. The main reason is that the cross-polarization level is extremely low and is easily influenced by the parasitic radiation of

TABLE 1. Performance comparison among existing works.

Ref.	Package	Antenna type	Package size	Profile h/λ	Impedance BW (S_{11}<-10)	Peak gain (dBi)	3-dB Gain BW	Radiation eff.
[6]	LTCC	Grid antenna array	5.68 λ_0 ×5.68 λ_0	0.23	137-147 (7%, S_{11}<-5)	17.6 146 GHz	140-149 (6.2%)	65% 145 GHz *
[7]	LTCC	Slot array	14.7 λ_0 ×9.19 λ_0	0.38	130.3-145 (10.7%)	20.5 138 GHz	130-145 (10.9%)	59.2 % 138 GHz
[10]	HDI	Grid antenna array	4.89 λ_0 ×4.89 λ_0	0.38	136-157 (14.3%)	14.5 146 GHz	143-148 (3.4%)	N.A.
[11]	HDI	Patch array	2.05 λ_0 ×2.05 λ_0	0.18	135-155 (13.8%)	14 143 GHz	132.2-155 (15.9%)	71% 145 GHz *
[14]	WLP	CPW patch array	3.03 λ_0 ×2.10 λ_0	N.A.	130-150 (14.3%)	10 140 GHz	130-150 (14.3%)	N.A.
[15]	WLP	Patch array	0.79 λ_0 ×0.79 λ_0	0.076	126.5-138 (8.7%)	8.66 130 GHz	125-140 (11.3%)	83.5% 135 GHz **
This work	**WLP**	**Patch array**	**2.26 λ_0 ×2.26 λ_0**	**0.059**	**124-155 (22.2%)**	**10.96 140 GHz**	**129-148 (13.7%)**	**65% 140 GHz**

λ_0 is the wavelength at center frequency of the operating band.
* Average efficiency.
** Simulation results

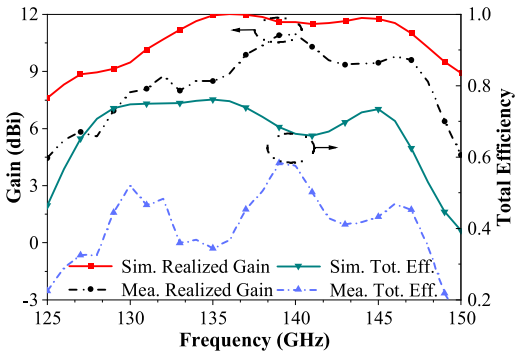

FIGURE 12. Far-field performance of the proposed antenna.

the probe during the test [32] and the bottom noise of the measurement system.

Fig. 12 shows the radiation performance of the antenna. Several factors are responsible for the discrepancies between the simulation and measurement results. Firstly, the metal surface roughness causes additional loss in the feeding network [30] and reduce the antenna gain. Secondly, the error in the relative permittivity of the BCB material causes the frequency deviation, just like in other dielectric-substrate-based antennas [10], [11]. Thirdly, some errors were introduced during the fabrication and measurement process. The simulated total efficiency in the middle of the working band is around 70%, while the efficiency on both sides of the band falls off significantly, as the feeding network limits the radiation performance of the antenna. The maximum gain of 12.0 dBi appears at 136 GHz. The measured maximum gain is 10.96 dBi at 140 GHz and the average radiation efficiency during 3-dB gain bandwidth is 48%.

D. COMPARISON AND DISCUSSION

Table 1 summarizes the main performance of several D-band packaged antennas published in recent years. Compared with LTCC and HDI technique, the packaged antennas based on WLP process has lower profiles, especially the proposed 2 × 2 antenna array. In particular, the antenna has an impedance bandwidth of 22.2%, which is higher than the majority of published designs. The proposed antenna also has a reasonable radiation efficiency and a higher gain. In addition, the 3-dB gain bandwidth of this designed antenna can reach 13.7%.

V. CONCLUSION

A broadband patch antenna array and its DP-MIMO implementation in wafer-level package for D-band wireless communications are proposed and fabricated with the advanced 4-layer BCB packaging technique. By introducing a back cavity and carefully developing the feeding network, the antenna achieves an impedance bandwidth up to 18.9%. The antenna adopts wafer-level package and can be directly connected to the RFICs through vias and transmission lines, which greatly reduces the interconnection loss and the profile. Moreover, the utilization of pairwise antiphase feeding technique can effectively suppress the cross-polarization and reduce the impact of feeding network on the radiation pattern of the antenna. The antenna can realize a gain of 10.96 dBi. The above properties make the proposed antenna suitable for application in dual-polarization MIMO communications.

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