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A Review of Design and Integration Technologies for D-Band Antennas

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ABSTRACT This article reviews the current state-of-the-art of millimeter-wave (mm-wave) antennas for communication and sensing applications in the D-band between 110 and 170 GHz. The most popular design techniques, including Antenna-on-Board (AoB), slotted waveguides, Antenna-in-Package (AiP) and Antenna-on-Chip (AoC), are described using relevant examples from scientific literature. Potential benefits and limitations of integration technologies, such as specialized packaging, chip post-processing steps and interconnects, are listed as well. The reported performances of all listed designs are compared against each other, taking the antenna size relative to operating frequency into account. This novel comparison indicates that small-scale integrated AiP and AoC designs can achieve competitive performance levels with short and low-loss interconnects.

INDEX TERMS Antenna-in-Package, Antenna-on-Board, Antenna-on-Chip, D-band, millimeter-wave.

I. INTRODUCTION

THE PURSUIT of increased performance and the limited available bandwidth in the radio frequency (RF) spectrum has pushed the development of wireless devices towards the millimeter-wave (mm-wave) band between 30 and 300 GHz. For example, the fifth generation (5G) mobile network includes sections of the Ka-band (26.5-40 GHz) to achieve high-speed and low-latency radio access [1]. Highly integrated communication and sensing devices are promising applications for the 60 GHz industrial, scientific and medical (ISM)-band [2]–[5]. In automotive radars, the 77 GHz band has enabled better accuracy and resolution performance with smaller device sizes compared to the 24 GHz band [6].

The trend of increasing operating frequency is expected to proceed beyond 100 GHz into the D-band (110-170 GHz). Numerous examples of short-range sensing devices operating in the 122 GHz ISM-band can already be found in literature [7]–[11]. Furthermore, the D-band's high-speed data transfer capability over short ranges as demonstrated in [12] and [13] could fulfill the future requirements of beyond-5G dense communication networks [14]–[16]. Potential applications are not limited to short ranges: a data link across 60 km was demonstrated with an adapted commercial 122 GHz radar transceiver in [17]. A 150 GHz long-range automotive radar was proposed in [18], and mid-range operation was concluded to be feasible throughout the mm-wave band.

A wireless system at D-band must be designed with sufficient effective isotropic radiated power (EIRP) to overcome the relatively high path loss. However, the difficulty and cost of generating high-power RF rise with frequency, and so do power losses in substrates and interconnects. Optimizing the radiation efficiency and limiting interconnect losses are therefore key challenges in mm-wave antenna design.

D-band antennas can be small enough to be implemented within the same package or even on the same die as the front-end electronics (FEE), limiting interconnect losses. Such a combined module with a monolithic microwave integrated circuit (MMIC) and an integrated antenna can be smaller and cheaper to assemble compared to a similar system consisting of separate components. Moreover, its interface can be limited to baseband or intermediate frequency (IF) signals and power supply, limiting high-performance materials and high-complexity mm-wave design to within the module. This translates into cost savings, improved efficiency, and

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TABLE 1. Overview of D-band Antenna-on-Board and slotted waveguide designs and reported performance from literature.
^{S}: Simulated result. ^{E}: Dimensions (partially) estimated based on published images.

Antenna Type	Size [mm^2]	Substrate	Interconnect (loss [dB])	Gain [dBi]	BW [%]	BW@ f_c [GHz]	Year	Ref
8-element series-fed patch	-	130 μm RO3003	WGL (0.7)	6	4	5@124	2009	[19]
Differential patch	2×0.6	130 μm RO3003	WB (-)	8^S	9.2	$12@131^S$	2016	[20]
4×8 slotted-SIW array	10×9.4^E	254 μm RO4350B	WGL (-)	16.3	12.2	15@122.5	2019	[21]
8-element differential series-fed patch	13.9×1.1	170 μm RO3003	WGL (1.63)	13	5.7	7@123.5	2019	[22]
Y-shaped microstrip	2.2×2	250 μm TLY-5	WB $(3.1)^S$	13.6^S	16	20@125	2019	[23]
8×14-element series-fed patch array	20×11.5^E	- μm Astra MT77	WB $(4)^S$	18^S	0.8	1@123	2020	[24]
8-element series-fed patch	10×1.1^E	127 μm Astra MT77	WB $(2.5)^S$	13.6	6.9	10@145	2020	[25]
4×4 patch array	4.3×4.3	127 μm Megtron 7N	- (-)	14	13.8	20@145	2020	[26]
20 dBi gain horn launched from PCB	20×20^E	127 μm RT5880	WB+ WGL (≥5)	≈10	32.9	48@146	2014	[27]
2×2 slotted gap waveguide array	2.85×2.85^E	-	- $(0.2)^S$	14^S	20	$28@141^S$	2019	[28]
16×16 slotted gap waveguide array	26×26^E	-	- (-)	32^S	10	$14@141^S$	2019	[29]
32×32 slotted waveguide array	67×67	2.4 mm copper laminate	WGL (1)	39.1	11.8	15@127	2014	[30]
64×64 slotted waveguide array	134×134	2.4 mm copper laminate	WGL (3)	43	11.5	14.5@126	2014	[30]

faster time to market when implemented in a base station, radar array, mobile phone or automobile for example.

Given the large number of potential mm-wave applications, the interest in low-cost and highly integrated devices is expected to grow. This publication reviews the state-of-the-art (SoA) design techniques for D-band antennas based on scientific literature published throughout the last decade. The aim is to provide an overview supported by relevant examples. As a novel contribution, a comparison is presented of the reported gain levels, bandwidths and sizes of the discussed antenna designs. This comparison illustrates the competitive performances achieved by integrated antennas.

The remaining sections are organized as follows: Section II lists and discusses published D-band antenna designs in 'conventional' printed circuit board (PCB) and waveguide technologies. Sections III and IV compare relevant design techniques of published Antenna-in-Package (AiP) and Antenna-on-Chip (AoC) designs, respectively. Section V provides a comparative overview and proposed future prospects of mm-wave antenna design, and Section VI concludes this paper. An Appendix has been included to list and define all abbreviations used throughout this text and in the presented tables and figures.

II. PCB AND WAVEGUIDE ANTENNAS

PCB-based microstrip antennas and waveguide-based aperture antennas are popular choices for a wide range of applications and operating frequencies. Antenna-on-Board (AoB) designs are comparatively cheap, small, and simple to design and manufacture with commonly available PCB technologies [31]. Their versatility makes them attractive for a variety of omnidirectional, fixed-beam and beam-steering mm-wave-applications. These use-cases include multiple-input multiple-output (MIMO), automotive radars and active beamforming arrays for 5G base stations [32]–[34].

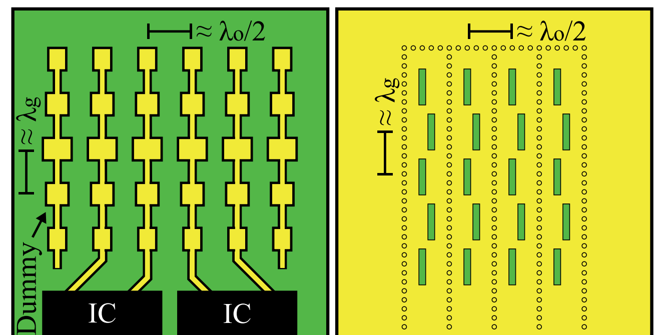

FIGURE 1. Schematic depictions of PCB-based 4 × 5 series-fed patch (left) and slotted SIW (right) antenna arrays, based on [25] and [21]. Approximate array dimensions are given in terms of guided (λ_g) and free-space (λ_0) wavelengths.

Waveguide antennas are applied mainly for their high gain and low-loss properties. Their standardized dimensions and flanges offer a high degree of modularity between off-the-shelf components such as filters and gain horns [27]. However, the use of waveguides in commercial applications has remained limited due to their large size and weight. These main downsides are reduced at mm-wave frequencies, and the low losses are promising for highly integrated 5G devices, for example [35]. The performances of published D-band AoB and waveguide designs are listed in Table 1.

A. ANTENNA-ON-BOARD

The most common AoB design found in Table 1 is the series-fed patch, a schematic example of which is depicted as a 4×5 array in Fig. 1. Series-fed patch arrays form a fan-like radiation pattern that enables wide-angle steering around one axis, making them a popular choice for automotive radars and MIMO arrays. Out of the typical examples listed in Table 1, it is evident that the series-fed patch designs achieve the narrowest bandwidth (BW) relative to the center frequency

(f_c). A symmetric corporate-feed patch array as presented in [26] may achieve a higher bandwidth without frequency scanning or squinting behavior, at the cost of a larger distribution network [31]. These properties make corporate feeds a popular option in fixed-gain and beam-steering arrays for point-to-point backhaul and point-to-multipoint base-station use-cases, respectively.

Slotted substrate-integrated waveguide (SIW) antennas produce a gain and radiation pattern comparable to series-fed patch antennas, whilst achieving a wider input bandwidth as demonstrated in [21]. From the schematic depiction of a PCB-based slotted SIW array shown in Fig. 1, it can be seen that the dimensions are similar to series-fed patch arrays.

The main benefits of AoBs, the low development cost and high degree of design freedom, diminish in the higher mm-wave frequencies. Most standard PCB materials are too lossy for mm-wave circuits, so high-performance laminates such as Rogers RO3003 and Isola Astra MT77 are used. Still, substrate and surface roughness losses in feed lines and distribution networks have been reported in the order of decibels per centimeter, limiting the practically feasible array size [21], [25], [57]. Additional losses due to wire-bond (WB) transitions from chip to PCB can amount to several decibels as reported in [23]–[25].

Advanced PCB-manufacturing technologies such as semi-additive processing (mSAP) and High-Density Interconnect (HDI) any-layer laser-via technology must be applied to achieve manufacturing tolerances of around 10 μm, which can still be significant in the mm-wave domain [58], [59]. For example, reported shifts of 3-4 GHz from the designed center frequencies were attributed to over-etching in [25], [26]. Although the deviations are only in the order of some percents, they can prove critical to narrow-band antennas.

Whilst antenna size and array spacing are based on the operating frequency, MMIC dimensions do not necessarily scale accordingly. The required half-wavelength spacing for D-band steering arrays is around one millimeter, whilst the dimensions of single, dual and quad-channel D-band MMIC dies described in [24], [25], and [27] are in the order of 2×2 mm^2 or larger. Considering standard encapsulating surface-mounted chip-packages measure in the order of several square millimeters as well, densely spaced AoB arrays may require fan-in networks as depicted in Fig. 1. This results in additional substrate losses, limiting the achievable gain from large PCB-based array sizes.

B. WAVEGUIDES

Waveguide transmission lines achieve lower losses compared to PCB traces and can transfer higher powers than coaxial cables at mm-wave frequencies, enabling larger arrays with relatively low distribution losses. Centrally-fed fixed-gain slotted-waveguide arrays with 32×32 and 64×64 elements operating in the D-band were presented in [30], and their reported performance has been included in Table 1. Antenna efficiencies of over 50% were achieved despite the corporate distribution networks spanning several centimeters.

Gap-waveguide technologies may achieve even lower losses than conventional waveguides, as simulated results in [28] and [29] indicate efficiencies of up to 95%. Gap-waveguides use periodic metal structures to form magnetic boundary conditions which guide a propagating electromagnetic wave between unconnected parallel metal plates [60].

Insertion losses of PCB-based waveguide launchers (WGLs) at D-band have been reported in the range of 0.7-3.6 dB in [19], [22], [61]–[63], which are similar to the WB transitions listed in Table 1. However, waveguide transitions may be considered too large for dense antenna arrays. Moreover, an additional lossy bondwire is still required between a PCB-based WGL and chip such as in [27]. A package- or chip-based WGL structure as demonstrated in [64] is an attractive solution to limit these losses.

III. ANTENNA-IN-PACKAGE

The development of AiP technology, which implements one or multiple antennas with the radio or radar die in a single surface-mounted package, was driven by a demand for integrated single-chip devices [65]. The earlier AiP design examples include single-chip radio modules at 5.7 and 60 GHz, presented in [66] and [67] respectively. Nowadays AiPs can be found in a wide range of mm-wave applications, such as tile-based scalable phased arrays, 5G communication, automotive radars and sensing devices [68], [69].

An overview of reported performances from AiP designs published in scientific literature is given in Table 2. Not all designs were characterized as assembled module: some were measured by probe from a microstrip line (MSL) or co-planar waveguide (CPW). In other designs such as [41], a dummy MMIC was used as probe location to include the WB or flip-chip (FC) interconnect in the measurement.

A. INTEGRATED SUBSTRATE TECHNOLOGY

Several of the earlier designs in Table 2 are printed microstrip antennas manufactured using PCB technologies on substrates small enough to fit in conventional packages [36]–[41]. Due to the small size and single purpose, a specialized low-loss substrate with suitable dielectric constant (ε_r) such as alumina and liquid-crystal polymer (LCP) or a flexible material such as polyimide can be selected at low overall cost. High performance MMIC-molding compounds as characterized in [70] may be attractive options for a package-based antenna substrate as well. However, the etching tolerances of PCB technologies can lead to mismatches between designed and measured performance as reported in [41].

Substrate loss reduction has been demonstrated with coupled pairs of antennas or parasitic elements, to suppress TM_0 surface waves and increase the antenna efficiency (η) to simulated values beyond 75% [36]–[38], [41]. Such designs with a relatively large area achieve a fixed gain of around 10 dBi and are better suited as standalone antennas rather than in densely-spaced wide-scanning arrays.

The 4-element differential patch antenna design in multi-layered ball-grid array (BGA) technology as presented

TABLE 2. Overview of D-band Antenna-in-Package designs and reported performance from scientific literature. ^{S}: Simulated result. ^{E}: Dimensions (partially) estimated based on published images.

Antenna Type	Size [mm^2]	Technology & Substrate	Inter-connect	Gain [dBi]	η [%]	BW [%]	BW@f_c [GHz]	Year	Ref
2 folded dipoles + 4 parasitic patches	2.3×2	Integrated substrate 127 μm Alumina	CPW	10.9	-	20.4	25@122.5	2011	[36]
2×2 patch array	1.8×1.7		CPW	9.9	80^S	3.9	5@127.5	2012	[37]
2 folded dipoles	2×2^E	Integrated substrate Polyimide film	FC/RDL	9.7	80^S	14.2	18@127	2013	[38]
Quasi-Yagi-Uda	1×0.9^E	Integrated substrate 50-100 μm LCP	Balun	6	89	13.8	20@145	2015	[39]
50-element grid array	7.2×6.5		FC	14.5	61.8	5.5	8@145	2016	[40]
Patch + parasitic patches	3×3^E		WB	4.8	-	17.4	21@120	2016	[41]
2×2 circular differential patches	2.2×2.8^E	4-layer BGA / Unspecified	FC	8.8^S	-	12.5	20@160^S	2014	[42]
2×2 aperture-coupled patch array	2.5×3.4	HDI BGA / 260 μm Mitsubishi CCL-HL972	FC	7.8	55	24	30@125	2017	[43]
Aperture-coupled stacked patch	2.5×2.5	LTCC / 320-530 μm DuPont 9K7	WB	7.8	-	20.4	25@122.5	2016	[44]
	3×3^E		WB	10.1	86^S	11.2	14@125.3	2018	[45]
6×6 aperture-coupled MEBG array	2.3×2.3		CPW	12.3	≥80^S	7.5	9@120	2019	[46]
18-element grid array	5.3×5.0	LTCC / 250 μm Hirai CS71	FC	15	83^S	4.6	6@128	2013	[47]
4×4 slotted-SIW array	5.8×5.6	LTCC / 480-820 μm Ferro A6M	WGL	16.2	54^S	15.6	22@141	2013	[48]
240-element grid array	12×12		WB	17.6	65	2.7	4@147	2015	[49]
4×4 cavity-backed patch array	6×5.9		SIW	19.2^S	-	6.2	8.8@141^S	2017	[50]
8×8 cavity-backed patch array	12.5×11.8		WGL/ SIW	21.8	38.3	6.9	9.8@141.6	2019	[51]
41-element grid array	5.5×5^E	LTCC / 70-300 μm ESL 41110	FC	8	-	5.1	7@138.5	2016	[52]
2-element series patch	2.8×0.9^E		MSL	10.6	-	3.59	4.3@120	2019	[53]
8-element rhombic	3.9×2.7^E	eWLB	FC/RDL	11	-	31	37@119^S	2017	[54]
Bow-tie	2×2		FC/RDL	5.8	85^S	19.6	25@128^S	2018	[55]
43-element rhombic	13.7×4.9^E		FC/RDL	15.5	75^S	9.9	12@121^S	2018	[56]

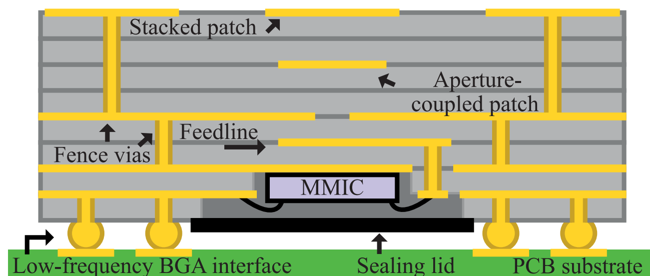

FIGURE 2. Schematic cross-section of an LTCC-based aperture-coupled stacked patch antenna, based on [44].

in [42] demonstrates a direct impedance match with the FEE and over the air output power combining. Its simulated results outperform the measured gain of another 4-element patch array in BGA-technology, presented in [43], indicating that a higher interconnect efficiency was achieved due to the closer integration and direct matching.

B. MULTI-LAYER LTCC

Low-temperature co-fired ceramics (LTCC) was the first technology to enable the large-scale production of AiP designs [69]. The ceramic-tape process enables multi-layer structures with vertical interconnects similar to PCB technology within the volume of a surface-mounted package, as depicted in Fig. 2. The material and stack-up can be selected specifically for the AiP and feed structure. The variety of available material options with different permittivity values offers a high degree of design freedom. Even ferrite-loaded ceramics exist, which enable miniaturization and improved performance of integrated magnetic components [71].

The aperture-coupled stacked patch antennas presented in [44] and [45] are good examples of LTCC-based AiP designs. The multi-layer feed allows for a compact device: as depicted in Fig. 2, the MMIC can be encapsulated within an air cavity directly below the radiators. Furthermore, laser-drilled plated vias increase the total device efficiency by shielding feedlines and forming a cavity around the stacked patches to prevent surface waves. Both stacked-patch designs in Table 2 demonstrate good gain performance for non-array designs.

LTCC technology enables the design of three-dimensional radiators, such as mushroom electromagnetic bandgap (MEBG) structures and SIW horn antennas [46], [72]. Sufficiently large packages can be designed to accommodate multiple antenna elements for a high fixed gain, such as the slotted SIW array presented in [48] and the 240-element grid array in [49]. Good radiation efficiencies were reported from LTCC-based grid arrays in [47] and [49], and even better gain performance and bandwidths were reported from similarly-sized cavity-backed patch arrays in LTCC packages [50], [51]. The multi-layer distribution networks and antenna designs demonstrated in these designs can be a cost-effective solution compared to AoB designs, as the requirement of high performance laminates can be limited to within the volume of the package.

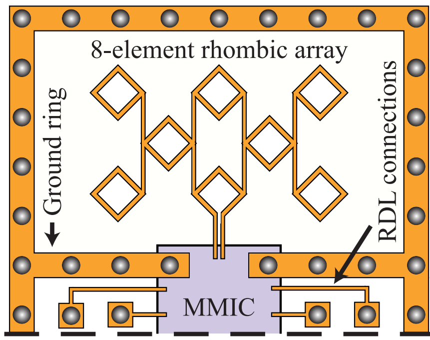

FIGURE 3. Schematic depiction of a rhombic antenna array in eWLB technology, based on [54].

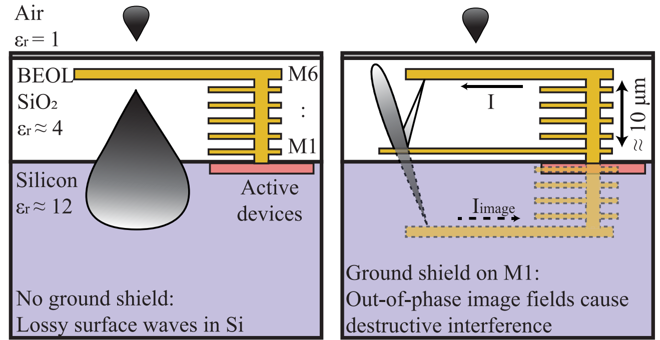

FIGURE 4. Schematic cross-section of an antenna in the top-metal layer of a standard (Bi)CMOS BEOL without (left) and with (right) ground plane reflector. Based on [95].

LTCC shares a drawback with PCB technologies, as copper tolerances can lead to performance variations. Moreover, LTCC is prone to planar shrinkage of up to 10%, making it challenging for robust mass production [71]. Zero-shrinkage substrates do exist, which can significantly improve the quality of manufacturing as demonstrated in [53].

Although the close integration between antennas and FEE contributes to lower path losses, the WB or FC interconnect with compensating network between the encapsulated MMIC and antenna can still contribute to decibel-level losses. Self-matching half-wavelength WBs as used in [45] negate the need for such a matching network, but limit the bandwidth.

C. EWLB TECHNOLOGY

A high-density redistribution layer (RDL) without lossy WB connections can be realized in thin-film embedded wafer level ball grid array (eWLB) technology. This RDL can accomodate antennas with a direct connection to the MMIC, as illustrated in Fig. 3. The thin film used in eWLB is most suitable for planar antennas without a supporting substrate.

The manufacturing accuracy can be higher than LTCC-based antennas, since eWLB films do not suffer from significant shrinkage. The absence of a lossy substrate below the antenna, combined with the low-loss FC interconnect between the MMIC and RDL, is expected to enable highly efficient and scaleable AiP designs. However, as the technology is planar, the achievable compactness is limited compared to multi-layer LTCC packages. Moreover, the absence of dielectric substrate prevents antenna miniaturization.

Most eWLB antennas are balanced wire-style designs such as dipoles, rhombic antennas and bow-ties. Differential patch antennas and CPW-fed slots can be designed in eWLB as well. The BGA connections with the PCB can act as spacers, achieving a few hundred micrometers of separation between the antenna and a PCB-based reflector. A small form factor bow-tie antenna with excellent simulated efficiency was presented in [55]. Rhombic antenna arrays of several sizes have been presented in [54] and [56]. These designs demonstrate good gain and bandwidth performance compared to LTCC-based grid arrays in [40], [47], [52].

IV. ANTENNA-ON-CHIP

Antennas designed in the back end of line (BEOL) of standard integrated circuit (IC) technologies allow for the closest possible integration with the FEE. No lossy WB interconnect is required for an AoC, and the device size and assembly costs can be reduced further compared to AiP designs [39]. Although chip surface area is relatively expensive, the size of a D-band antenna can be in the order of a square millimeter. An overview of published D-band antennas designed in complementary metal-oxide semiconductor (CMOS) or Silicon Germanium (SiGe) BiCMOS technology is shown in Table 3.

Standard (Bi)CMOS technologies present severe hurdles to overcome in the design of efficient on-chip antennas. The high permittivity of the silicon bulk, at approximately 11.9, confines the majority of the radiated RF in surface waves and limits the radiation into free space as shown in Fig. 4. Moreover, the low substrate resistivities of tens to a few hundred Ω-cm lead to high dissipation losses and additional gain degradation [94]. Particularly the earlier D-band AoC designs in Table 3 achieve limited gain: sub-zero-dBi designs were considered highly efficient at the time [73], [74].

A. SHIELDING OF THE SUBSTRATE

An on-chip ground plane at the bottom metal layer can isolate the radiation from the lossy bulk substrate. However, distance between the top and bottom metals in the BEOL layer does not provide enough separation. At a few μm the distance is only a small fraction of a D-band wavelength, leading to destructive interference from the reflected back-radiation and dissipation losses from the image currents as illustrated in Fig. 4 [94]. The close proximity of the ground plane affects the antenna impedance due to near-field coupling. The small separation is insufficient for wide-band SIW antennas and limits the efficiency of patch antennas [74].

In [75], additional metal layers within a spin-coated Benzocyclobutene (BCB) top-layer were manufactured above a standard BiCMOS BEOL to more than double the separation. The resulting patch antennas achieved significantly

TABLE 3. Overview of D-band Antenna-on-Chip designs and reported performance from scientific literature. ^{S}: Simulated results. ^{E}: Dimensions (partially) estimated based on published images. ^{H}: Half-gain bandwidth, ^{1}: 1-dB gain bandwidth.

Antenna Type	Size [mm^2]	Height & technology	Design feature	Gain [dBi]	η [%]	BW [%]	BW@f$_c$ [GHz]	Year	Ref
Tapered dipole	0.12×0.12^{E}	- μm SiGe	Very small size	-20	0.3	1.2	2@164	2008	[73]
Cavity-backed slot	1.2×0.6	275 μm SiGe	SIW between M1-M6	-2^{S}	-	5	7@140^{S}	2011	[74]
Slotted SIW	2×0.6	275 μm SiGe		0^{S}	-	3.6	5@140^{S}	2011	[74]
E-shape patch	0.7×0.7	275 μm SiGe	M1 as ground plane	-2^{S}	-	7.1	10@140^{S}	2011	[74]
Patch	2×2.2	750 μm SiGe	BCB above BEOL	3.4	50^{S}	4.1	5@123	2013	[75]
2 zigzag dipoles	1.2×0.65^{E}	100 μm CMOS	AMC structure	2.5^{S}	62^{S}	19.2	27@145^{H}	2019	[76]
Bondwire dipole	1.2×0.59	- μm CMOS	Height: 500 μm	4.4^{S}	69^{S}	-	-@120	2014	[12]
Bondwire	0.8×0.75	- μm SiGe	Height: 450μm	8^{S}	-	14.6	23@158	2018	[77]
Folded dipole	0.54×0.16	250 μm CMOS	Ion-irradiated Si	-2.7	-	6.3	9@143	2015	[78]
Dipole	1.2×0.9	150 μm SiGe	Tuned Si height Ground reflector	4	-	21	28@133^{H}	2014	[79]
2 folded slots	3.3×3.2	140 μm CMOS	Thin membrane above Si	6.3^{S}	89.5^{S}	27.6	45@163	2012	[80]
Cavity-backed monopole	1.8×1.8	750 μm CMOS	BCB BEOL & polymer cavity	6.7	93.9^{S}	4.6	12@130	2012	[81]
Quasi-Yagi-Uda	1.17×0.95	400 μm glass	IPD process	5.2^{S}	85^{S}	7	8@119^{S}	2013	[82]
Patch	2.2×2.2	400 μm glass		1.6^{S}	70^{S}	8	10@125^{S}	2014	[83]
Dual folded dipole	1.6×1.6	700 μm SiGe	LBE below antenna	8.4	60^{S}	26.7	40@150	2012	[84]
Quasi-Yagi-Uda	2×2	300 μm SiGe		5.1	76	20	30@150	2014	[39]
Folded Dipole	1.36×1.38	185 μm SiGe		3	45^{S}	≥6.1	≥10@165	2019	[85]
Dual folded dipole	1.8×1.1	200 μm SiGe	Selective LBE at radiating edges	6	54	14.3	18@126	2017	[11]
Patch	1×1	200 μm SiGe		6	≥60^{S}	5.2	8@154	2019	[85]
Differential patch	0.8×0.75	200 μm SiGe		7	60^{S}	1.9	3@158^{S}	2019	[86]
4×4 dipole array	5.5×5.5	- μm SiGe	Quartz superstrate	13.5^{S}	45^{S}	7.3	8@110^{S}	2013	[87]
Shorted patch + quartz resonator	1.3×0.8^{E}	- μm SiGe	Quartz superstrate + parasitic patch	6^{S}	50^{S}	7.5	9@121^{S1}	2012	[88]
	0.65×0.35^{E}	200 μm SiGe		4.2^{S}	69^{S}	-	-@160	2018	[89]
Stacked DRA's	0.8×0.9	- μm CMOS	2 alumina DRA's	4.7	43^{S}	11	14@130	2012	[90]
Cavity slot-fed alumina DRA	0.7×0.9	- μm CMOS	TE$^{x}_{\delta 11}$ mode	3.7	62^{S}	13	18@135	2014	[91]
	0.7×0.9	- μm CMOS	TE$^{x}_{\delta 15}$ mode	7.5	42^{S}	7	9.5@135	2014	[91]
2 frustum DRA's	2.5×0.8	338 μm CMOS	LBE DRA's in high-resistivity Si	12.2^{S}	82^{S}	5.7	10@173^{S}	2018	[92]
2 cavity slot-fed alumina DRA's	2.2×0.4	- μm CMOS	TE$^{x}_{\delta 13}$ mode, 0.65λ spacing	7	-	10.6	14@132	2019	[93]

better gain and efficiency than the E-shaped patch reported in [74].

Artificial magnetic conducting (AMC) structures can be designed in the BEOL metal layers below the antenna to achieve in-phase reflection, increasing the radiation efficiency. However, the achievable fractional bandwidth of a CMOS-based AMC structure at D-band is limited to around 4%, according to a model presented in [96]. In [97], an AMC structure was designed below a dipole pair by loading the BEOL dielectric with capacitive tiles. This enabled tuning of the generated TM0 surface waves for loss minimization and reshaped the antenna input impedance for wide-band matching. This design was implemented in a CMOS-based 145 GHz radar IC in [76].

On-chip bondwire antennas such as presented in [12] and [77] do not suffer from the low BEOL height. A half-loop bondwire is placed above a ground plane, where image currents complete the full-loop magnetic dipole. The ground plane shields the antenna from the silicon bulk as well. The relative simplicity in design and standard manufacturing technique make the bondwire antenna an attractive option when the added height on top of the chip is allowed. As the peak radiation of such a loop antenna is directed parallel to the chip surface, it is well-suited for wireless communication between co-planar ICs but not for a broadside scanning array.

B. MODIFYING THE SILICON BULK

The key to an efficient antenna design in (Bi)CMOS technology, as demonstrated by most designs in Table 3, is the prevention of substrate losses. Alternatively to a shielding ground plane, several design and manufacturing techniques exist to limit losses within the silicon bulk. In [78] for example, the low resistivity of silicon was increased locally using ion-irradiation. Although this process resulted in an inhomogeneous resistivity throughout the silicon, a gain enhancement of 5 dB was reported due to reduced substrate losses. Still, a peak gain of only −2.7 dBi was achieved by the published design.

A reduction of the bulk thickness from a few hundred μm can reduce the losses due to surface waves as well. In [79] the substrate thickness of an on-chip reflector-backed dipole was tuned to an approximate quarter-wavelength to maximize the gain, leading to a 4 dBi design in SiGe technology without any non-standard manufacturing techniques.

Micromachining of the silicon bulk to improve efficiency was demonstrated in [80], where excessive substrate removal led to even better wide-band performance than expected

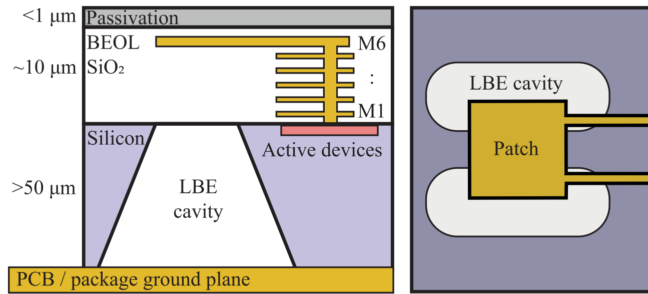

FIGURE 5. Schematic cross-section (left) and top view (right) of a differential patch antenna on the top metal layer in a (Bi)CMOS BEOL, as described in [86]. LBE cavities have been formed below the radiating antenna edges.

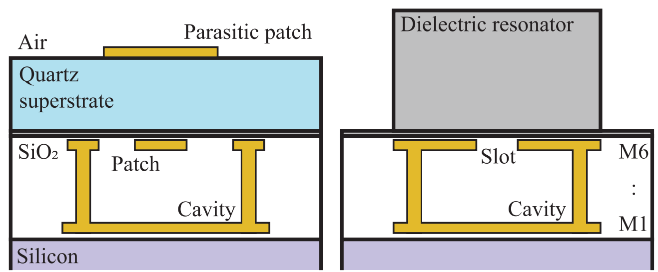

FIGURE 6. Schematic cross-sections of a parasitic patch on quartz superstrate (left), and a dielectric resonator antenna (right) based on [89] and [90], respectively. Both antennas are glued on top of a standard (Bi)CMOS BEOL.

from design simulations. In [81], a polymer-filled and metal-lined cavity was constructed directly underneath the antenna. Another option is to remove the silicon substrate altogether and replace it with low-loss glass in a substrate transfer process [98]. As demonstrated in [82] and [83], glass-substrate antennas realized with Integrated Passive Device (IPD) technology can achieve high efficiencies. Although the design techniques described in [80]–[83] achieve excellent efficiency and gain performance, the potential for close integration is limited as co-production with IC-electronics with standard techniques is currently unfeasible for all four designs.

The most-listed efficiency improvement technique in Table 3 is localized back-side etching (LBE). Rather than removing or thinning the entire silicon bulk, selected sections below can be etched away in a relatively simple and low-cost post-processing step. By etching a cavity directly below a radiator as illustrated in Fig. 5, leakage into the substrate can be limited without affecting surrounding components. LBE is particularly well-suited for on-chip patch antennas and reflector-backed antennas, as the remaining silicon can act as a supporting spacer between the radiator and PCB-based ground plane [84], [85]. An end-fire quasi-Yagi-Uda design presented in [39] also achieved a good efficiency due to LBE, as the lossy substrate modes were significantly reduced.

In [11], [85], and [86], LBE was applied selectively around or underneath sections of the radiating element as illustrated in Fig. 5. This solution limits coupling to the silicon bulk at critical locations, such as underneath the radiating edges of a patch antenna, whilst retaining better mechanical stability than a cavity below the entire antenna.

C. SUPERSTRATE AND DIELECTRIC ANTENNAS

The same phenomenon that pulls the RF energy towards the high-permittivity silicon can be used to guide the energy towards free space. In [87], [88], and [89], the radiation from an AoC is guided away from the silicon by a quartz superstrate. A secondary resonating element on top of the superstrate, as illustrated in Fig. 6, radiates into free space. Although an extra assembly step is required to glue the superstrate to the chip, this may be preferred to non-standard wafer processing such as LBE. The single-element designs published in [88] and [89] achieve radiation efficiencies above 50%, and [87] demonstrates the scalability of this concept to achieve a simulated gain of 13.5 dBi.

Similar gain and efficiency performances can be achieved with smaller surface areas using a dielectric resonator antenna (DRA) design. Similar to the superstrate antennas, a DRA is a piece of low-loss high-permittivity dielectric that is glued to the top of the BEOL. The shape of the DRA facilitates a resonant cavity mode and allows for efficient radiation into free space. Cuboid-shaped DRAs designed for different cavity modes were presented in [90], [91], and [93]. The designed modes resulted in varied gain pattern, efficiency, and bandwidth performances. A schematic cross-section of a DRA on CMOS is shown in Fig. 6. Lastly, excellent gain and efficiency performance from a pair of high-resistivity silicon DRAs was reported in [92], although co-production with active electronics is unfeasible on the undoped silicon.

D. III-V TECHNOLOGIES

The majority of published AoC designs in Table 3 are SiGe chips, which allow for high volume production at relatively low cost [99]. However, the maximum output power of BiCMOS-based electronics in the D-band range is limited due to the low breakdown voltage of silicon compared to III-V compound technologies such as Gallium Nitride (GaN) and Gallium Arsenide (GaAs). In mm-wave systems where high linearity, very low noise or Watt-level performance is required, III-V MMICs are already enabling factors [100]. Given the ongoing developments on high-power mm-wave power amplifiers, III-V technologies are expected to play a significant role in future D-band applications as well. High power outputs have been demonstrated by Indium Phosphide (InP) devices throughout the D-band, as shown in Fig. 7, and future GaN devices are expected to reach even higher powers due to the high breakdown voltage of the material [101].

Given the relatively high price per watt of III-V MMICs, decibel-level losses due to off-chip antenna interconnects can be considered expensive. However, the high substrate resistivities enable more efficient antenna designs compared to silicon-based AoCs. For example, a 60 GHz InP-based cavity-backed slot antenna presented in [102] achieved a simulated efficiency of over 90%. In [103] and [104],

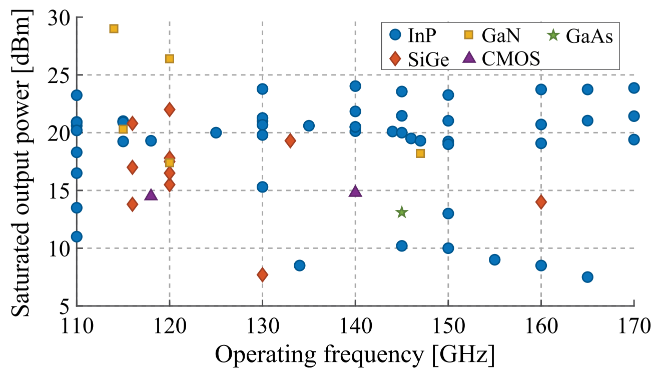

FIGURE 7. Reported saturated output power and operating frequency of several published D-band power amplifiers in III-V and (Bi)CMOS technologies. Adapted from [105].

low-loss WGL have been demonstrated on InP and GaAs technologies, respectively. The more efficient antenna and interconnects can lead to fewer amplifier stages for a specified power output. This leads to reduced power consumption, thermal dissipation, and device surface area which may justify the cost of III-V AoC designs in high-performance applications.

V. DISCUSSION & OUTLOOK

A. PERFORMANCE COMPARISON

The reported performances of antenna designs from the past decade, as listed in Tables 1–3, have been visualized in Figs. 8 and 9. The achieved antenna gain is compared to the physical antenna size in Fig. 8, and a linear fit was performed on the data to illustrate the expected gain increase with surface area of all four antenna types. The expected gain of an ideal aperture antenna is included as a reference.

Waveguide antennas achieve the highest reported gain levels depicted in Fig. 8, as the low distribution network losses enable efficient large-scale array designs. The higher losses associated with AoB designs are reflected by the lower rate of gain increase with size. Based on the presented works, a waveguide-based array with distribution network is expected to significantly outperform a similarly-sized PCB-based array in terms of efficiency and gain.

None of the realized AoB and waveguide antennas in Fig. 8 measure below two squared wavelengths, whilst the majority of AiP designs is smaller than this size. The gain levels of AiPs scale better with size compared to AoBs, with several of the larger designs matching or exceeding the trend of AoBs. This indicates lower losses are achieved by the larger AiP designs, which can be attributed to closer integration with the FEE and the selection of specialized mm-wave technologies such as LTCC and eWLB. However, the challenges of substrate shrinkage and limited resolution remain for repeatable mass-manufacturing of multi-layered LTCC devices [71].

Most published AoC designs are smaller than a squared wavelength, as the chip manufacturing costs are directly linked to the surface area. Although this limits the achievable gain, several of the AoC designs outperform the reference aperture antenna by several dBs and demonstrate that the SoA of efficient on-chip radiators has advanced well beyond negative gain levels. Out of the efficiency improvement techniques discussed in the previous section, LBE seems particularly attractive due to the relative simplicity of design and manufacture. Superstrate or DRA designs are promising solutions as well, especially in cases where wafer-level post-processing is unfeasible or undesired.

Besides being well-suited to low-power and small-scale applications, integrated AiPs or AoCs can be regarded an attractive option for steerable phased arrays and MIMO applications. Within multi-channel tile-modules, these integrated antenna elements could demonstrate competitive performance compared to conventional on-board array designs, thanks to a low-loss IF distribution network and cost-effective use of high-performance materials. For high-EIRP applications where a single-feed antenna with a high fixed gain is desired, or for passive high-power combiners, low-loss waveguide and gap-waveguide structures seem most attractive.

In Fig. 9, the reported bandwidth performances of the designs have been depicted. A wide range of bandwidths, from narrowband up to about 30%, is achieved by in-package and on-chip designs. Electrically small antennas are limited in bandwidth due to the inverse Chu-limit of quality factor. As a result, the smallest antenna designs and AoCs in particular show a trend of increasing bandwidth with size. The highest bandwidths are achieved by AiPs and AoCs of around a squared wavelength in area, although high power losses can result in a widened input reflection bandwidth as well. The larger-area array antennas are generally band-limited by their distribution networks, leading to the downward trends with respect to area for AoB, AiP and waveguide designs.

B. D-BAND INTERCONNECTS

Implementing on-chip or in-package antennas close by the FEE can lead to very short interconnects with low losses. However, the close proximity may also cause undesired coupling effects. Circuit components in the near-field can affect the antenna impedance and radiation pattern, and radiated fields may couple into the circuit and lead to interference and deteriorated stability. In this regard, the antenna and circuitry of highly integrated mm-wave systems cannot be considered entirely separate components. Closer integration is expected to lead to closer collaboration between antenna and IC designers throughout the development process.

Designing the integrated antenna alongside the FEE enables the choice of a more optimal interface than the conventional 50 Ω impedance. In the ideal case, radiators and FEE are co-designed to interface directly without the need of a matching network. This reduces the size and cost of the device, and is expected to provide a better wide-band match with minimized interconnect losses [106]. Such a direct-matched power amplifier with slot antenna has

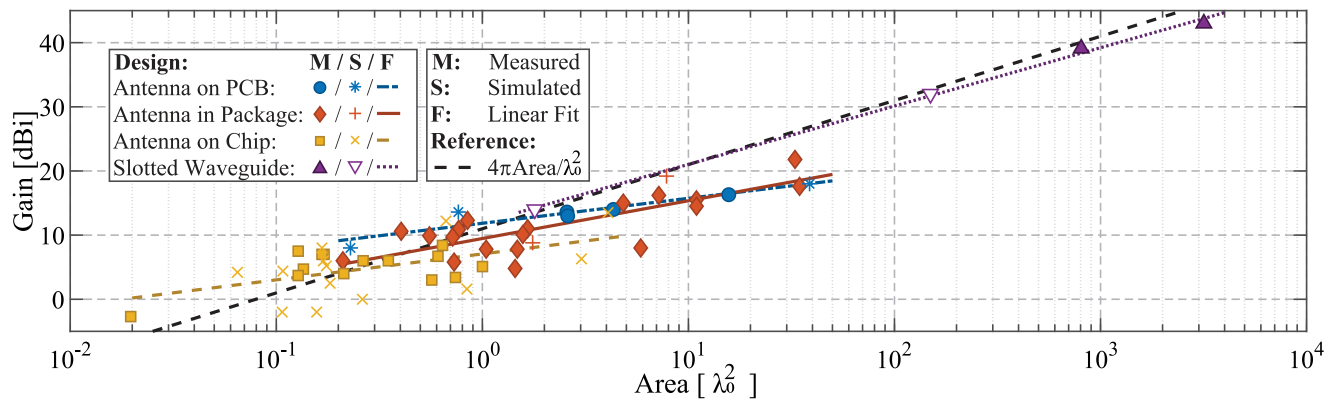

FIGURE 8. Gain performances versus the physical sizes of the D-band antenna designs discussed in this work, summarized from published literature since 2011. Reported results based on simulations are depicted separately from measurements.

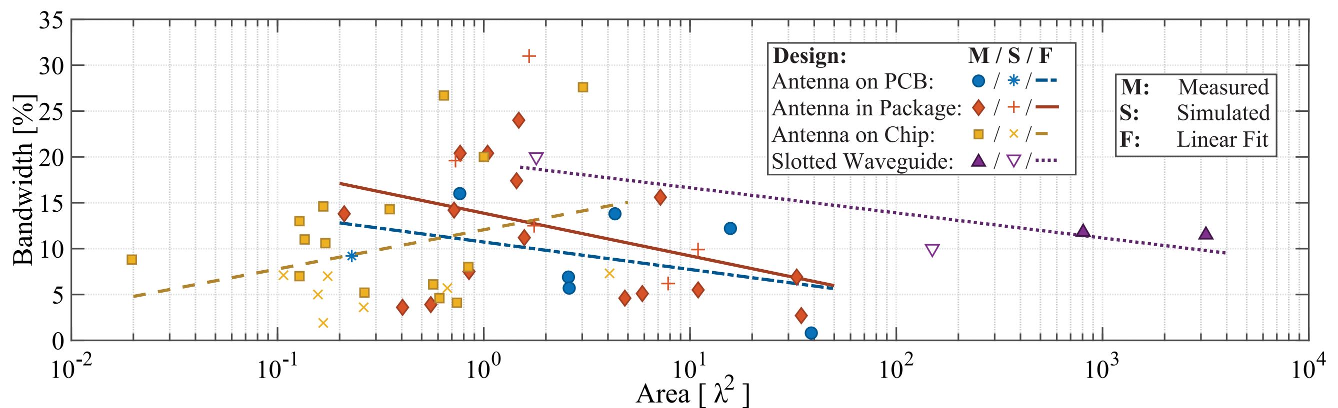

FIGURE 9. Reported input-reflection ($|S_{11}| < -10$ dB) bandwidths of the D-band antenna designs discussed in this work, summarized from published literature since 2011. Data based on simulations are depicted separately from measurements.

been demonstrated at K-band in [107], and the BGA-based patch array presented in [42] featured a direct match to the electronics as well. On-chip and eWLB antennas seem particularly suitable for wide-band direct matching as no WB is required.

When a close integration of a D-band antenna with the FEE is not possible, waveguides are the transmission line of choice. However, the PCB-based WGLs discussed in Section II are relatively large and require an additional WB interconnect between the chip and launcher. As small-footprint and low-loss WGL designs are expected to find use in many D-band applications, a direct transition from the chip can be regarded as a promising concept for future system designs.

Several direct chip-to-waveguide transitions at D-band have already been presented in published literature. In [108] for example, a DRA-based WGL on top of a CMOS die achieved an insertion loss of 2-3 dB over an approximate 15% bandwidth at 140 GHz. A bondwire E-probe presented in [109] achieves a maximum of 1.1 dB insertion loss throughout a bandwidth spanning nearly the entire D-band.

C. OUTLOOK

A large variety of D-band antennas has been developed throughout the last decade, as attested by the publications discussed in this work. As ongoing developments of next-generation sensors and communication systems explore increasingly higher frequencies, the D-band is expected to receive more attention in the upcoming years. This may lead to new and innovative antenna designs where efficiency enhancement techniques such as LBE, parasitic elements, metasurfaces and dielectric loading are applied. Beyond these described technologies, new strategies for antenna design may also be enabled through the continuous development of manufacturing technologies for semiconductors, PCBs and chip packages.

New and improved production technologies such as laser-vias, low-shrinkage and low-loss laminates and additive manufacturing could lead to fewer process variations, more accurate optimization and mass-scale production of in-package modules. Particularly high-volume markets with strict performance and process requirements, such as the automotive industry, may drive these developments in the pursuit of high-performance and low-cost integrated sensors. In a similar way, compound semiconductor manufacturing is already advancing to larger production quantities and lower unit costs, driven by the widespread use of commercial GaN MMICs in 5G base stations [110].

Highly integrated wireless systems at D-band present multi-faceted challenges beyond the antenna design. As

described earlier in this section, the close integration of chip-based circuitry with an antenna can lead to coupling effects that require circuit knowledge from the perspective of an antenna engineer. Similarly, RF design considerations may be entwined with the mechanical structure and rigidity of a chip or package, as was observed in LBE and multi-layer LTCC packages. For dense arrays with closely-spaced electronics and distribution networks, thermal dissipation is another challenge an antenna designer may face. A resulting antenna element may be designed in conjunction with a cooling solution, or be part of a heat spreading system itself. As multi-disciplinary systems are integrated together on a smaller scale, it may become increasingly difficult to tell where one discipline ends and another begins. As a consequence, multi-physics design tools and cross-disciplinary design flows will become important assets in the mm-wave antenna engineer's toolbox.

VI. CONCLUSION

This publication provides an overview of the current SoA in D-band antenna design and integration. This topic is expected to become increasingly relevant in the development of beyond-5G communication devices and high-resolution sensors for healthcare, industrial and automotive applications.

Highly integrated antennas and electronics can achieve very low interconnect losses and small form factors compared to PCB-based or waveguide antennas. Specialized packaging technologies such as LTCC and eWLB provide a high degree of design freedom for wide-band and high-gain AiP designs. Integrated antennas on CMOS and SiGe chips have demonstrated excellent gain performances with radiation efficiencies above 50% with relatively simple post-processing steps such as LBE and glued-on superstrates.

Integrated on-chip waveguide launchers and efficient antennas on III-V MMICs are regarded as promising next steps to achieve high power at D-band with minimized device size and interconnect losses. And lastly, the close collaboration required to design highly integrated systems for future applications may lead to even more efficient and wide-band interconnects than can be achieved with standardized interfaces.

APPENDIX
LIST OF ABBREVIATIONS

5G	5th generation mobile communications
AiP	Antenna-in-Package
AMC	Artificial magnetic conductor
AoB	Antenna-on-Board
AoC	Antenna-on-Chip
BCB	Benzocyclobutene
BEOL	Back end of line
BGA	Ball-grid array
BW	Bandwidth
CMOS	Complementary metal-oxide semiconductor
CPW	Co-planar waveguide
DRA	Dielectric resonator antenna
EIRP	Effective isotropic radiated power
η	Antenna efficiency
eWLB	Embedded wafer level ball grid array
f_c	Center frequency
FC	Flip-chip
FEE	Front-end electronics
GaAs	Gallium Arsenide
GaN	Gallium Nitride
HDI	High-density interconnect
IC	Integrated circuit
IF	Intermediate frequency
InP	Indium Phosphide
IPD	Integrated passive device
ISM	Industrial, scientific and medical
LBE	Localized back-side etching
LCP	Liquid crystal polymer
LTCC	Low-temperature co-fired ceramics
MEBG	Mushroom electromagnetic bandgap
MIMO	Multiple-input multiple-output
MSL	Microstrip line
MMIC	Monolithic microwave integrated circuit
mm-wave	Millimeter-wave
mSAP	Semi-additive processing
PCB	Printed circuit board
RDL	Redistribution layer
RF	Radio frequency
SiGe	Silicon Germanium
SIW	Substrate-integrated waveguide
SoA	State-of-the-art
WB	Wire-bond
WGL	Waveguide launcher.

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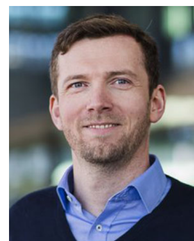

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