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Ultra-Wideband Phased Antenna Array Time Delay Unit Architecture Optimization in Presence of Component Non-Idealities

DANIEL A. RAMIREZ [1,2] (Member, IEEE), W. JOEL D. JOHNSON [1] (Senior Member, IEEE), AND GOKHAN MUMCU [2] (Senior Member, IEEE)

[1] Space and Airborne Systems, L3Harris Technologies, Palm Bay, FL 32905, USA

[2] Electrical Engineering Department, University of South Florida, Tampa, FL 33620, USA

CORRESPONDING AUTHOR: D. A. RAMIREZ (e-mail: daniel.a.ramirez@l3harris.com)

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ABSTRACT Recently reported time delay unit architecture (TDU-A) optimization method based on integer linear programming is investigated for the first time, for practical implementation of ultra-wideband (UWB) phased antenna arrays (PAAs). Specifically, the method is considered for linear UWB PAAs and their feed networks which include non-idealities when practical implementations of their circuit components are pursued. These non-idealities are shown to cause additional time delay errors that were unaccounted for in prior work. The errors are induced by frequency dependent variations in power divider isolation and load mismatch, component VSWRs, and dispersion. Proper modeling of these errors in the TDU-A optimization leads to a TDU-A that has the necessary delay range required to steer the beam towards the desired wide scan angles. For experimental verification, a 16 element linear PAA TDU-A is optimized for operating from 5-30 GHz by modeling the non-idealities of the feed network that is implemented to steer the beams towards boresight, 25°, and 50°. Simulation and measured performances demonstrate the UWB operation with stable radiation patterns.

INDEX TERMS Phased antenna array, true-time delay, integer programming, broadband, ultra-wideband.

I. INTRODUCTION

MILITARY and commercial applications continue to drive antennas to service broader frequency bands with requirements of multiple beams and/or fast beam steering which necessitates the use of phased antenna arrays (PAAs) with true time delay systems [1], [2], [3], [4], [5], [6]. True time delay systems require the use of time delay units (TDUs) to control the phase excitation of each element and have stability over frequency [7]. Fig. 1(a) demonstrates a TDU circuit consisting of n bits which can switch between a reference and a delay state. An amplifier is typically included to compensate for the loss incurred by the bits. Ultra-wideband (UWB) phased antenna array designers are often required to distribute the time delay to multiple division levels within the RF-fanout due to space constraints at the element level [8]; thereby creating a TDU architecture (TDU-A). Fig. 1(b) shows an exemplary (but also the optimal as discussed in Section II) TDU-A for an $M = 16$ element linear PAA with $D = 4$ division levels. $L = 2$ TDU layers are distributed between the $d = 1$ division level (TDU_1) and the $d = 4$ division level (TDU_2) of the RF-fanout. This TDU-A is one configuration out of many possible variations. The number of variants grows exponentially as the number of elements increases. In our recent work [9], it has been demonstrated that there exists an optimal TDU-A which can be found by a system architect using integer linear programming. However, despite its comprehensiveness, the optimization model introduced in [9] focuses on ideal implementations of feed networks such as with the assumptions of perfectly matched and isolated power dividers with ideal transmission lines. This also seems to be the approach taken in the

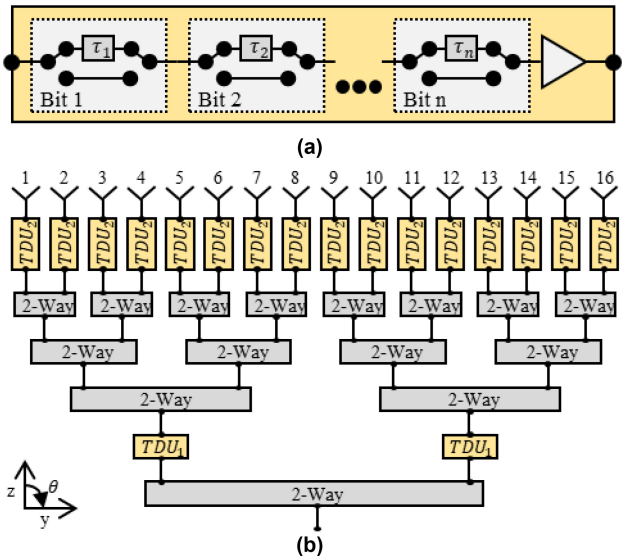

FIGURE 1. (a) A TDU block diagram with n bits, each with τ_n of delay capability; (b) An example TDU architecture for a 16 element PAA (which is also the optimal for the PAA and its requirements considered in this manuscript).

existing literature. Even though different approaches for designing TDU-As are presented [7], [8], [9], [10], literature does not provide a consideration of the impact of non-ideal responses of the circuit components that form the TDU-A in its practical implementation. In practice, the designs of the circuit components within a TDU-A are typically carried out independently by different engineers in a way to meet a set of requirements imposed by the TDU-A system architect. Although these requirements can be strict, they are far from being ideal (e.g., return loss (RL) >15 dB vs RL $>\infty$ across the UWB). The major circuit components in the TDU-A shown in Fig. 1(b) are the 2-way power dividers, TDUs, and antennas. The non-idealities in the network responses of these components and their frequency dependent variation lead to time delay errors. Therefore, it is of interest to account for these non-idealities in the optimization model of [9]. If these errors are left unnacounted for, radiation pattern degredations that cannot be resolved with PAA calibration occur due to the unavailibility of required delay lengths within TDUs. This is especially pronounced at the wider scan angles as shown in Fig. 2.

This manuscript offers three major contributions to the literature. The first is the transfer equation derivation through signal flow diagram of key components within the physical TDU-A implementation and relating the transfer equation into time domain in order to account for delay ripple when ports of the components are not terminated with idealistic perfectly matched impedances. The second is to incorporate these non-idealities (i.e., delay ripples), for the first time, within the optimization model of [9] to obtain the best TDU-A. The final contribution is the first experimental demonstration of the TDU-A designed based on the optimization results and thereby closing the modeled to measured loop. Some non-idealities in the responses of the feed network components may be specific to the particular feed network implementation technology and associated with fabrication and/or component tolerances. On the other hand, there are three major prevalent time delay errors that are not limited to a particular implementation or component. This manuscript focuses on these three major time delay errors that are associated with the frequency dependent phase ripples arising from the imperfections in 1) component VSWR, 2) power divider isolation and load mismatch, and 3) transmission line dispersion. The approach presented in this manuscript can be further extended by the designers to include the time delay errors that will be coming from specific implementation technology and/or manufacturing tolerances.

To demonstrate the validity of the presented algorithm, a TDU-A is designed for an $M = 16$ element linear PAA consisting of Vivaldi antenna elements operating from 5 GHz to 30 GHz. By using fixed length delay lines to represent the TDU states within the TDU-A, three feed networks and PAAs are designed and fabricated to investigate the performance of radiation patterns steered towards 0°, 25°, and 50° scan angles. It is important to note that, although the manuscript considers stationary beam steering for the ease of implementation, the optimization method is directly applicable to the electrically steered PAAs that incorporate integrated circuit controled TDU devices.

II. TIME DELAY ERRORS IN LINEAR PAAS

Time delay error terms stem from the non-idealities of the components within the feed network that is designed to implement the TDU-A for practical use. These errors must be modeled and included in the total delay requirement of the TDU-A before proceeding with the optimization. Previous work [9] determined the delay range and resolution of a TDU-A only by the geometry of a uniform plane wave intersecting with the PAA which results in a progressive phase across the array [8]. Different than this, there are three pervasive time delay error terms considered for the first time in this manuscript that stem from non-ideality of the TDU-A components: delay variation by phase ripple due to divider isolation and load mismatch (τ_{div}), delay variation by phase ripple due to VSWR (τ_{VSWR}), and dispersion in the transmission lines (τ_{disp}). Many of the components in a TDU-A, such as the TDU itself, cannot be designed prior to architecting the TDU-A. The requirement imposed by the system architect establishes the worst-case performance acceptable for each component. Consequently, the TDU-A is designed without *a priori* knowledge of performance across frequency. Hence, TDU-A design must assume the worst-case delay error that can arise from the components.

Sections II-A–II-C address each time delay error term individually. As a primer, their performance effect is demonstrated in Fig. 2. The array factor (AF) patterns in Fig. 2(a) are generated by three separate phase excitations to a $M = 16$

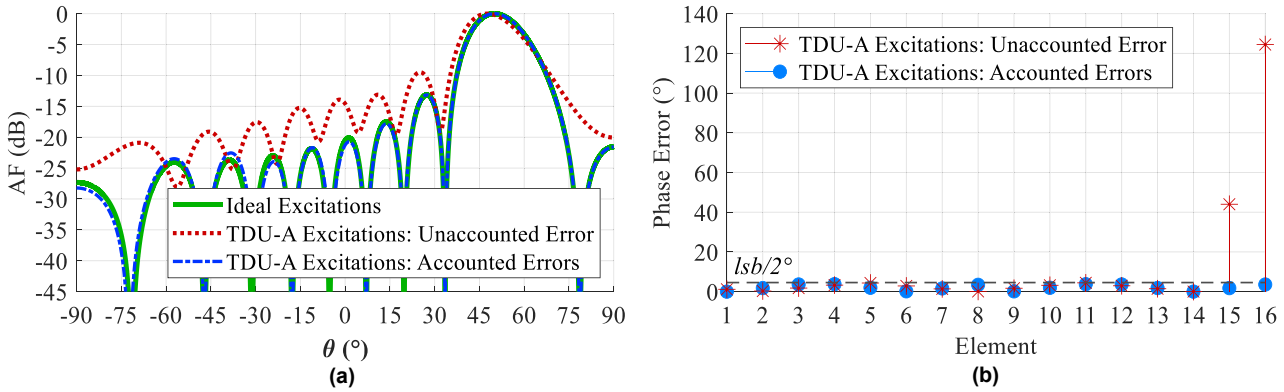

FIGURE 2. Effect of time delay errors from component non-idealities for the TDU-A shown in Fig. 1(b) at $f_c = 17.5$ GHz: (a) Array factor (AF) patterns with ideal excitations, excitations from the TDU-A when optimized with the time delay errors accounted or not; (b) Absolute value of the phase error across antenna elements.

element PAA at $f_c = 17.5$ GHz (i.e., center frequency of the 5 GHz – 30 GHz operation band). The PAA exhibits an element spacing $e_p = 0.5$ cm which is half wavelength at $f_{max} = 30$ GHz. Its beam is steered towards the maximum desired scan angle of $\theta_{max} = 50°$. The architecture shown in Fig. 1(b) was designed with the optimization method in [9] for the case when time delay errors are unaccounted or accounted as detailed in Section II-E. It is observed that the radiation pattern generated by the TDU-A optimized without accounting the time delay errors of the feed network components shows degraded sidelobe levels when compared to the patterns generated by the ideal excitations and by the TDU-A optimized with accounting the time delay errors. The degraded side lobe levels (SLLs) are caused by the lack of delay range required to compensate for the delay errors generated by the TDU-A components. In both cases, a bit search is conducted that aims to minimize the delay error between the TDU bit selected and the ideal phase at each element. However, as shown in Fig. 2(b), the phase error at the 15th and 16th elements of the PAA, when compared to an ideal progressive phase excitation, falls significantly outside the quantized error bound ($lsb/2° = 4.5°$) when the TDU-A is optimized without accounting for the component delay errors. This occurs because the required delay to steer the 15th and 16th elements is simply not available by the TDU-A and selecting different states cannot overcome this fundamental deficiency. Conversely, when the TDU-A is optimized by accounting the component delay errors, the architecture is capable of fully generating the desired time delays and the phase distribution errors fall below the desired quantization error. The quantized error bound results from the *lsb* which is found through the optimization in Section II-E.

A. DIVIDER ISOLATION AND LOAD MISMATCH

Imperfect divider isolation and load mismatch introduces frequency dependent phase ripple to the signal through path. A divider is a 3-port network as shown in Fig. 3. Based on Mason's rule [11] and the signal flow diagram in Fig. 3(b),

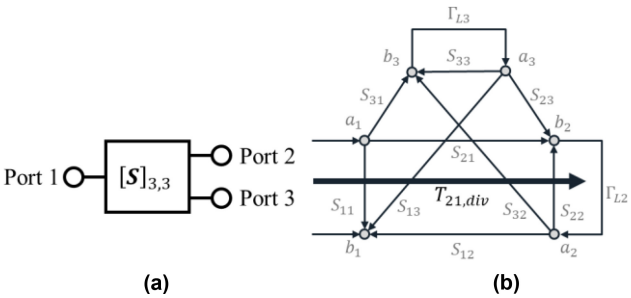

FIGURE 3. (a) 3-port S-parameter network and its (b) signal flow graph representation when ports 2 and 3 are terminated with loads.

the transmission from port 1 to port 2 is

$$T_{21,div} = \frac{S^D_{21} - S^D_{21}S^D_{33}\Gamma_{L3} + S^D_{31}\Gamma_{L3}S^D_{23}}{1 - (S^D_{22}\Gamma_{L2} + S^D_{33}\Gamma_{L3} + S^D_{23}\Gamma_{L2}S^D_{32}\Gamma_{L3}) + S^D_{22}S^D_{33}\Gamma_{L2}\Gamma_{L3}} \tag{1}$$

where S^D_{ij} are the complex S-parameters of the divider, Γ_{L2} and Γ_{L3} are the load reflection coefficients at ports 2 and 3, respectively. Note that when all loads are perfectly matched, $T_{21,div} = S^D_{21}$. From (1), $T_{21,div}$ is clearly dependent on Γ_{L2}, Γ_{L3} and isolations (i.e., S^D_{23} and S^D_{32}). The phase delay error at a frequency f is

$$\phi_{21,div}(f) = \angle\left(T_{21,div}\right) - \angle\left(S^D_{21}\right). \tag{2}$$

This phase delay error (in degrees) is typically less than 360° for a well-matched divider and can be converted into time to obtain the time delay error due to the isolation and load mismatch as

$$\tau_{21,div} = \frac{-\phi_{21,div}}{f\ 360}. \tag{3}$$

Equations (2) and (3) show that when $\tau_{21,div}$ is a negative number, the signal takes less time to propagate from port 1 to port 2 than the baseline S^D_{21}, whereas a positive number corresponds to a signal that takes more time. Positive value is the primary concern leading to a lack of TDU range since a negative delay error will still fall within the range

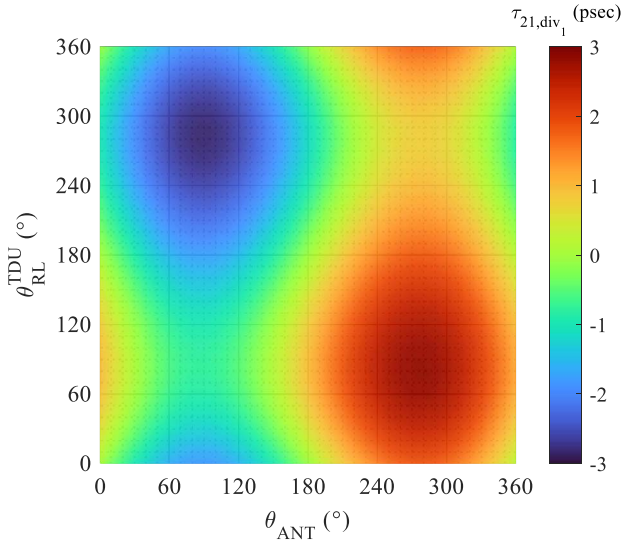

FIGURE 4. Time delay variation at 5 GHz when the divider is terminated with $\Gamma_{L2} = \Gamma_{L3} = 0.178\ e^{-j\theta_{RL}^{TDU}}$ and $\angle(\Gamma_{L2})$ and $\angle(\Gamma_{L3})$ are swept independently.

of the TDU-A optimized without regarding component non-idealities. Therefore, the single worst-case delay error for all frequencies which must be accommodated in the TDU-A is

$$\tau_{e,div} = \max\left(\tau_{21,div}(f)\right). \tag{4}$$

Using (1)–(4), we proceed with calculating the time delay error from the divider to be designed for the $M = 16$ element PAA. The design requirements that will be imposed on the reciprocal divider are RL $\geq$ 10 dB (i.e., $S_{11}^D,\ S_{22}^D,\ S_{33}^D \leq 0.316e^{-j\theta_{RL}^D}$), isolation (ISO) $\geq$ 15 dB (i.e., $S_{32}^D \leq 0.178\ e^{-j\theta_{ISO}^D}$), and insertion loss (IL) $\leq$ 1 dB (i.e., $S_{21}^D,\ S_{31}^D \leq 0.631e^{-j\theta_{IL}^D}$). Based on the RF fan-out shown in Fig. 1(b), the output ports of the dividers can be loaded in three different scenarios, by: 1) TDUs with an imposed requirement of RL $\geq$ 15 dB (i.e., $S_{11}^{TDU} \leq 0.178\ e^{-j\theta_{RL}^{TDU}}$), 2) input ports of the subsequent power dividers, or 3) antenna elements which are to be designed with a $VSWR \leq 3{:}1$ requirement, implying $S_{11}^{ANT} \leq 0.5\ e^{-j\theta_{ANT}}$. The delay values for each of the three load cases are calculated independently using equations (1)–(4). For each case, the loads are swept independently from 0° to 360° in 5° steps while the magnitudes are held constant at the worst-case value. The S-parameter amplitudes of the divider are taken as worst-case values and the phases (i.e., $\theta_{RL}^D,\ \theta_{ISO}^D,\ \theta_{IL}^D$) are modeled as ideal. Among these S-parameters, the most dominant factor in (1) is the stand-alone S_{21}^D term in numerator due to not being multiplied with a load reflection coefficient, however $\angle S_{21}^D$ is strictly bounded in the divider design (e.g., $\sim 90°$ for a standard single stage Wilkinson power divider). Sweeping phases of the other S-parameters in (2) does not provide new information since they are multiplied with load reflection coefficients that are already being swept in phase. Fig. 4 depicts the result of the sweep for the first power divider termination scenario when the ports 2 and 3

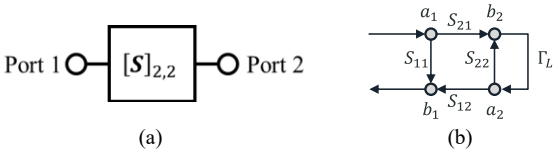

FIGURE 5. (a) 2-port S-parameter network and it's (b) signal flow graph representation when port 2 is terminated with a load.

are connected to TDUs at 5 GHz, implying $\Gamma_{L2} = \Gamma_{L3} = S_{11}^{TDU} = 0.178\ e^{-j\theta_{RL}^{TDU}}$. The maximum delay happens at 5 GHz as expected from (3) and leads to $\tau_{e,div_1} = 2.8$ psec. This is due to the fact that the consideration of (2) as in Fig. 4 is frequency independent until the last step where the phase values get converted into time domain using (3) to generate the y-axis of Fig. 4. Hence, the largest error is observed at the lowest frequency.

The phase sweeps of load reflection coefficients lead to worst case errors of $\tau_{e,div_2} = 5.1$ psec, and $\tau_{e,div_3} = 8.2$ psec when the output ports are connected to power dividers (scenario 2, $\Gamma_{L2} = \Gamma_{L3} = S_{11}^D = 0.316e^{-j\theta_{RL}^D}$) and antenna elements (scenario 3, $\Gamma_{L2} = \Gamma_{L3} = S_{11}^{ANT} = 0.5\ e^{-j\theta_{ANT}}$), respectively.

B. TDU VSWR

Non-ideal components such as TDUs introduce frequency dependent phase ripple on the through path due to the finiteness of their VSWR. A generic 2-port S-parameter network as shown in Fig. 5(a) can be used to model these components. From the signal flow diagram shown in Fig. 5(b), using the Mason's rule [11], the transmission from port 1 to port 2 can be determined as

$$T_{21,VSWR} = \frac{S_{21}^{TDU}}{1 - S_{22}^{TDU}\Gamma_L} \tag{5}$$

where S_{ij} are the complex S-parameters and Γ_L is the load impedance at port 2. As was the case for the divider, the deviation from the baseline phase can be calculated as

$$\phi_{21,VSWR} = \angle T_{21,VSWR} - \angle\left(S_{21}^{TDU}\right) = -\angle\left(1 - S_{22}^{TDU}\Gamma_L\right) \tag{6}$$

which shows that the only dependence is on the return loss specification of the TDU and the load which it is connected to. This is converted to time to obtain the delay error as

$$\tau_{21,VSWR} = \frac{-\phi_{VSWR}}{f\ 360}. \tag{7}$$

Since positive value of $\tau_{21,div}$ is the main concern as explained in previous section, the worst-case delay error that must be accommodated by the TDU-A is

$$\tau_{e,VSWR} = \max\left(\tau_{21,VSWR}(f)\right). \tag{8}$$

Using (5)–(8), we proceed to calculate the time delay error for the $M = 16$ element PAA. The TDU ($S_{22}^{TDU} \leq 0.178\ e^{-j\theta_{RL}^{TDU}}$) has two possible load terminations: 1) power

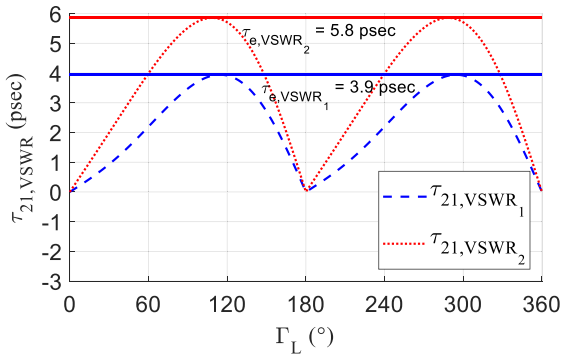

FIGURE 6. Time delay variation of TDU at 5 GHz when terminated with $\Gamma_L = S_{11}^D = 0.316\, e^{-j\theta_{RL}}$ (VSWR$_1$) and $\Gamma_L = S_{11}^{ANT} = 0.5\, e^{-j\theta_{ANT}}$ (VSWR$_2$).

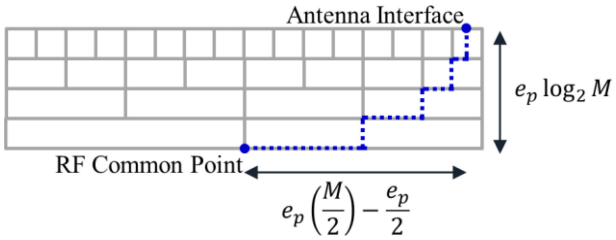

FIGURE 7. Illustration of the allowable area for the corporate feed network implementation pursued for the $M = 16$ element PAA. The dashed path represents the reference distance to the antenna interface.

divider with an imposed requirement of RL $\geq$ 10 dB (i.e., $S_{11}^D \leq 0.316e^{-j\theta_{RL}}$) and 2) antenna elements which are to be designed with a $VSWR \leq 3{:}1$ requirement, implying $S_{11}^{ANT} \leq 0.5\ e^{-j\theta_{ANT}}$. Sweeping the phase possibilities independently across the frequency range in (5)–(8), we find the worst-case time delay errors as $\tau_{e,\ VSWR_1} = 3.9$ psec and $\tau_{e,\ VSWR_2} = 5.9$ psec as shown in Fig. 6.

C. MICROSTRIP LINE DISPERSION

The time delay error caused by dispersion is due to the change in the effective dielectric constant over frequency and the length of microstrip line in the RF-fanout and TDU-A. Reference [12] provides a method for calculating dispersion of the microstrip line. Following this method for the selected printed circuit board (PCB) substrate (see Section III) provides that the effective dielectric constant, ϵ_{eff}, over the frequency range from 5 GHz to 30 GHz increases monotonically concave up from 3.26 to 3.31, respectively. Hence, the time delay variation over frequency is found by calculating the total delay through the RF-fanout at the highest and lowest frequency due to the extremes of the effective dielectric constants. The total microstrip line length through the RF-fanout is due to the combination of three lengths associated with maximum time delay needed to scan the beam towards θ_{max} (d_{scan}), a reference time delay needed to provide a connection from RF common feed point to the antenna element at the edge of the PAA (d_{ref}), and time delay through the power dividers (d_{pd}). It should be noted that the TDUs for this demonstration are delay lines on the PCB. The maximum delay that must be provided by the TDU-A for the linear PAA is calculated based on element spacing and maximum scan angle as

$$d_{scan} = (M-1)\ e_p\ \ \sin(\theta_{max}) \tag{9}$$

where e_p is the element spacing. d_{ref} represents the length of transmission line from RF common port to an antenna element when all TDUs are set to a reference state of 0 (i.e., the array is pointing to boresight). This reference length can be approximated by assuming that the area required at each division level, as defined in [8], has a vertical length of e_p and a horizontal length that starts at e_p at the element level and doubles for each division level moving from the antenna to the RF common feed point. This is demonstrated in Fig. 7 where the boxes represent the area for each division level of the RF-fanout and the dashed line is the reference path distance calculated as

$$d_{ref} = e_p\big(\log_2 M + M/2 - 1/2\big). \tag{10}$$

The length of the microstrip lines within the dividers depends on the design requirements and implementation choice. The 5 GHz to 30 GHz bandwidth requirement pursued in this manuscript necessitates a three stage microstrip line Wilkinson power divider. Since each stage is quarter wavelengths at the center frequency of $f_c = 17.5$ GHz and there are $\log_2 M$ levels of these dividers, total length of the power dividers becomes

$$d_{pd} = 3\big(\log_2 M\big)\left(\frac{c}{4f_c}\right) \tag{11}$$

where c stands for speed of light. Sum of (9), (10), and (11) provides the longest length of the microstrip line required as

$$d_{tot} = d_{scan} + d_{ref} + d_{pd}. \tag{12}$$

For the $M = 16$ element linear PAA and $e_p = 5$ mm (i.e., half wavelengths at 30 GHz), equations (9)–(12) provide $d_{scan} = 5.75$ cm, $d_{ref} = 5.75$ cm, $d_{pd} = 5.14$ cm, and $d_{tot} = 16.63$ cm. Hence, the effective length of the microstrip line becomes

$$d_{eff}(f) = d_{tot}\sqrt{\epsilon_{eff}(f)} \tag{13}$$

with maximum and minimum values attained at the edges of the operation band as $d_{eff} = [30.0,\ 30.3]$ cm. This distance is subsequently converted into time delay as

$$\tau_{eff}(f) = \frac{d_{eff}(f)}{c} \tag{14}$$

which leads to a delay of $\tau_{eff} = [1001,\ 1009]$ psec. The maximum variation in time delay across the bandwidth is therefore found as $\tau_{disp} = \tau_{eff}(f_{low}) - \tau_{eff}\big(f_{high}\big) = 8$ psec.

D. TOTAL DELAY ERROR

The total time delay error that must be utilized in optimization algorithm can simply be an additive combination of the worst-case situations determined in the previous section and summarized in Table 1. This will yield a total time delay error

TABLE 1. Time delay errors.

Error Variable	Interval (psec)	Number of Occurrences[a]	Variable Type
τ_{e,div_1}	±2.8	1	Random
τ_{e,div_2}	±5.1	2	Random
τ_{e,div_3}	±8.2	1	Random
$\tau_{e,VSWR_1}$	±3.9	1	Random
$\tau_{e,VSWR_2}$	±5.9	1	Random
τ_{disp}	8	1	Known

[a] When tracing from the common point to an antenna.

of 31 psec. However, this is an unlikely occurrence since the errors are function of frequency and their exact values are not known *a priori*. As an alternative approach for approximating total time delay error, they are considered random and distributed uniformly between their respective $\pm\tau_e$ (i.e., a uniformly distributed probability density function (PDF)). This assumption can be made because the performances of the individual components are bounded by the requirement, but the actual performance remains unknown until design is completed. Once the design is completed, the actual error may be located anywhere within the specified bound, justifying a uniform distribution assumption. As an example, the requirement for the antenna element discussed in this manuscript is $VSWR \leq 3{:}1$ as stated above; however, the exact value of S_{11}^{ANT} may be at any point within the 3:1 VSWR circle on Smith Chart over frequency, for example a VSWR of 2:1 is achieved at 15 GHz at 50° scan based on simulations. If two random variables are independent, then the PDF of their sum is equal to the convolution of their PDFs. Convolving the PDFs of the random variables in Table 1 the number of times each occur when tracing a path from the common point to an antenna result in a Gaussian distribution of random errors with a standard deviation of 13.4 psec. As compared to 25.9 psec (excluding dispersion), 13.4 psec is much smaller and can be used to avoid implementation of unnecessary longer states in the TDUs. There is a potential risk when using this approach that a situation may arise that once again the TDU-A does not have the delay range required to steer the beam at extreme angles. However, the probability has been lowered dramatically and it is preferred to use the least amount of delay possible to minimize loss and complexity in the RF-fanout. It is ultimately up to the architect to assess the and determine how much time delay error to include in the TDU-A from the Gaussian distribution. We selected the standard deviation for this manuscript. Unlike the others, the time delay error due to the dispersion is not random. It is additively combined with the other errors. Therefore, the total time delay error is found as $\tau_{error} = 13.4 + 8 = 21.4$ psec.

E. TDU-A OF A PAA INCLUDING DELAY ERRORS

In [9], it is demonstrated that the TDU-A optimization problem can be placed into the standard integer linear programming (ILP) form. Key steps of the process are summarized here to show how the time delay error calculated in previous section can be introduced into the optimization, however, previous understanding of [9] will be required to fully comprehend the following derivations. Specifically, τ_{error} is added in equation (17) of [9], which denotes the maximum time delay needed from the first TDU layer TDU_1, as

$$\tau_{max1} = \frac{h_{scan1}}{c} + \tau_{error} \tag{15}$$

where h_{scan_1} is the scan distance [9, eq. (16)] of TDU_1. Following the remainder of the method outlined in [9, Sec. III] the performance matrix $\boldsymbol{A}$ [9, eq. (10)] is filled out for each architecture variant

$$\boldsymbol{A} = \begin{bmatrix} \boldsymbol{a}_{\varphi e} & \boldsymbol{a}_{1_{msb}} & \boldsymbol{a}_{2_{msb}} & \boldsymbol{a}_{3_{msb}} & \boldsymbol{a}_{4_{msb}} \end{bmatrix} \tag{16}$$

where $\boldsymbol{a}_{\varphi e}$ is the quantization phase error for each architecture variant, and $\boldsymbol{a}_{d_{msb}}$ are the most significant bit (*msb*) (i.e., the longest time delay bit) of the TDUs at each division level d for each architecture variant where $D = \log_2 M = 4$ is the total number of divisions. The optimization requires constraints for each vector in the $\boldsymbol{A}$ matrix. As explained in [9], the maximum root mean squared (RMS) quantized phase error is set to $\phi_{max} = 5°$ so the quantization of the TDU-A has a minimal effect on the side lobe levels. The maximum *msb* is calculated based on the area in each division level as shown in Fig. 7 (as explained in [9, Sec. III]) by following the method outlined in [8] to find $\tau_{msb_1}^{max} = 376.8$ psec, $\tau_{msb_2}^{max} = 188.4$ psec, $\tau_{msb_3}^{max} = 94.2$ psec and $\tau_{msb_4}^{max} = 47.1$ psec. These values are placed into the constraint vector $\boldsymbol{b}$ [9, eq. (25)] as

$$\boldsymbol{b} = \begin{bmatrix} \phi_{max} & \tau_{msb_1}^{max} & \tau_{msb_2}^{max} & \tau_{msb_3}^{max} & \tau_{msb_4}^{max} \end{bmatrix}^T. \tag{17}$$

The objective function $\boldsymbol{Kx}$ [9, eq. (24)] sets the goal of the optimization, which is to minimize the number of TDUs, the number of bits, and the quantization phase error for the TDU architecture. Hence, $\boldsymbol{Kx}$ can be expressed as

$$\boldsymbol{Kx} = \begin{bmatrix} w_{TDU} & w_{bits} & w_{\phi} \end{bmatrix} \begin{bmatrix} \boldsymbol{\eta}_{TDU} & \boldsymbol{\eta}_{bits} & \boldsymbol{a}_{\phi_e} \end{bmatrix}^T \boldsymbol{x} \tag{18}$$

where w_{TDU}, w_{bits}, w_{ϕ} are the weights for the contributions of the TDU count, bit count, and phase error, respectively, $\boldsymbol{\eta}_{TDU}$ is a vector containing the number of TDUs for each architecture variant, $\boldsymbol{\eta}_{bits}$ is a vector containing the number of bits for each architecture variant, and $\boldsymbol{x}$ is a variable vector $\boldsymbol{x} = [x_1, x_2, \ldots, x_V]^T$ with V being the total number of architecture variants. In this manuscript, the priority is set to minimize TDU count, which is followed by the bit count, and then the phase error with the weight selection of $\begin{bmatrix} w_{TDU} & w_{bits} & w_{\phi} \end{bmatrix} = \begin{bmatrix} 1 & 0.1 & 0.001 \end{bmatrix}$, as described in [9], which was motivated by the industry need to minimize component count to benefit size, weight, power, and cost (SWAP-C). The ILP form for expressing the objective function and constraints of the TDU-A problem is

$$\begin{aligned} &\textit{minimize } \boldsymbol{Kx} \\ &\quad \textit{subject to } \boldsymbol{A}^T\boldsymbol{x} \leq \boldsymbol{b} \\ &x_1 + x_2 + x_3 + \ldots + x_V = 1 \\ &\quad x_v = 0 \textit{ or } 1 \;\forall\; v = 1, \ldots, V \end{aligned} \tag{19}$$

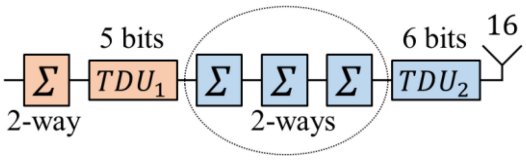

FIGURE 8. Optimized TDU architecture of the 16 element linear PAA where TDU_1 has 5 bits and $\tau_{lsb} = 4.4$ psec and TDU_2 has 6 bits and $\tau_{lsb} = 1.45$ psec.

where v is a particular TDU-A architecture variant and the summing constraint, $x_1 + x_2 + x_3 + \ldots + x_V = 1$, along with the integer constraint, $x_v = 0$ *or* $1 \ \forall \ v = 1, \ldots, V$, ensures that the solution will be $x_o = 1$, where subscript o stands for the optimum variant, and all other variables are zero [9, eq. (23)]. The ILP was run using MATLAB's intlinprog function and produced the optimal TDU-A shown in Fig. 1(b) and expounded in Fig. 8 where TDU_1 has 5 bits with $\tau_{lsb} = 4.4$ psec and TDU_2 has 6 bits with $\tau_{lsb} = 1.45$ psec. The other parameters found from optimization are $\phi_{max} = 4.52°$, $a_{1_{msb}} = 63.8$ psec, $a_{2_{msb}} = 0$ psec, $a_{3_{msb}} = 0$ psec, and $a_{3_{msb}} = 46.4$ psec.

III. DESIGN AND FABRICATION

Three PAAs with static feed networks are pursued for the design, fabrication, and testing of the optimization method. The feed networks are designed for beam steering towards to 0°, 25°, and θ_{max} of 50°. The TDU states for steering the beam towards these scan angles are implemented with fixed length meandered microstrip delay lines. Other design components are the RF connector transition, Wilkinson power dividers, and antennas. The printed circuit board substrate is Rogers 4003 ($\epsilon_r = 3.55$, $\tan\delta = 0.0027$ at 10 GHz) with $h = 0.203$ mm thickness. The microstrip delay lines were individually simulated with Keysight ADS Momentum to verify that the required delay and return loss performances are achieved. The Vivaldi antenna was designed and simulated in Ansys Electronics Desktop HFSS to determine the parameters shown in Fig. 9. The 16 element PAA for the 50° scan angle is shown in Fig. 10 with arrows indicating the layers meandered lines as TDUs. Two additional antenna elements with 50 Ω resistive terminations are added on each side of the PAA to reduce the edge effects for a total of 20 elements. The PAAs are characterized in a far field anechoic chamber as seen in Fig. 11.

IV. EXPERIMENTAL VERIFICATION

Elevation plane radiation pattern measurements are taken from 5 to 30 GHz in 1 GHz steps as θ is varying from $-90°$ to 90° in 0.5° step. These patterns are compared to the simulated radiation patterns obtained from PAA model. The model is multiplication of the array factor (AF) with the radiated electric field of the simulated Vivaldi antenna element. The AF is calculated using equations in [7]

$$AF(f_0) = \sum a_i e^{jk\boldsymbol{r_i}\cdot\hat{\boldsymbol{r}}} \tag{20}$$

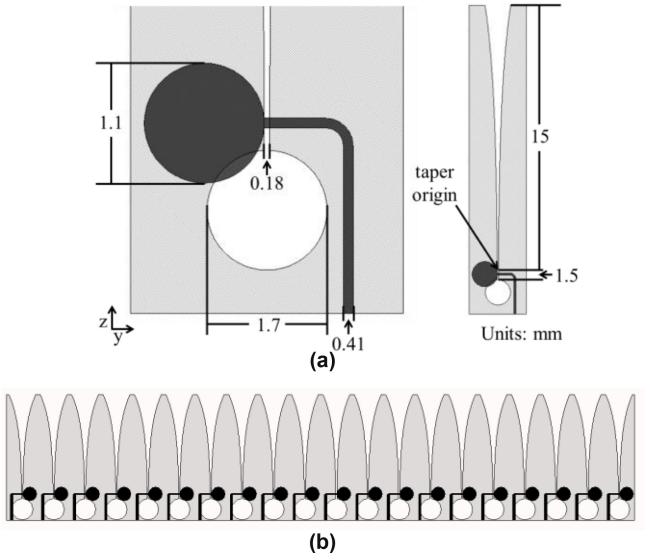

FIGURE 9. (a) Antenna element geometry; (b) 16 element array model with two terminated elements on both sides to reduce edge effects totaling 20 elements.

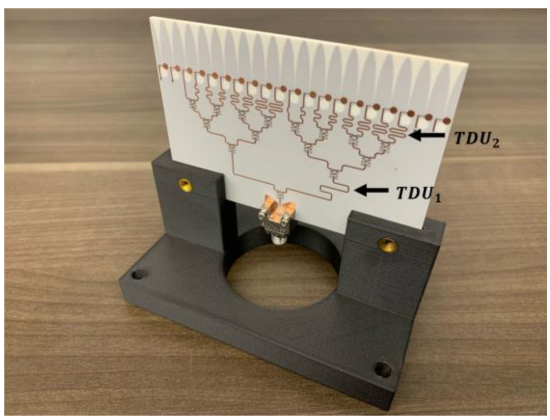

FIGURE 10. Fabricated 16 element linear PAA with feed network implemented for 50° beam steering.

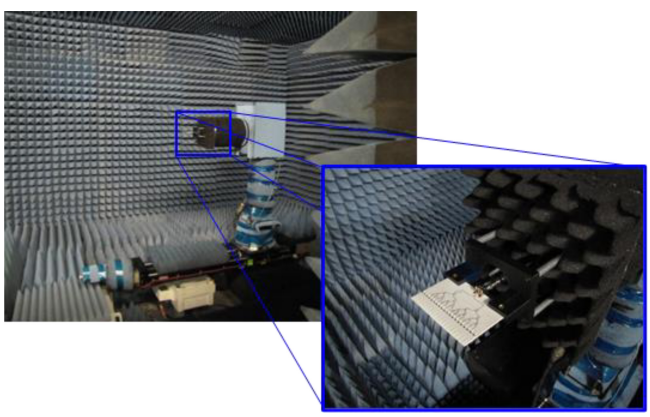

FIGURE 11. 16 element PAA with feed network implemented for 0° beam steering during measurement inside an anechoic chamber.

where $\boldsymbol{r_i}$ is the position vector of the i^{th} antenna element, $\hat{\boldsymbol{r}}$ is the unit vector in the direction of the observation point, $a_i = |a_i|e^{j\phi_{a_i}}$ is the complex weigh of the i^{th} antenna element

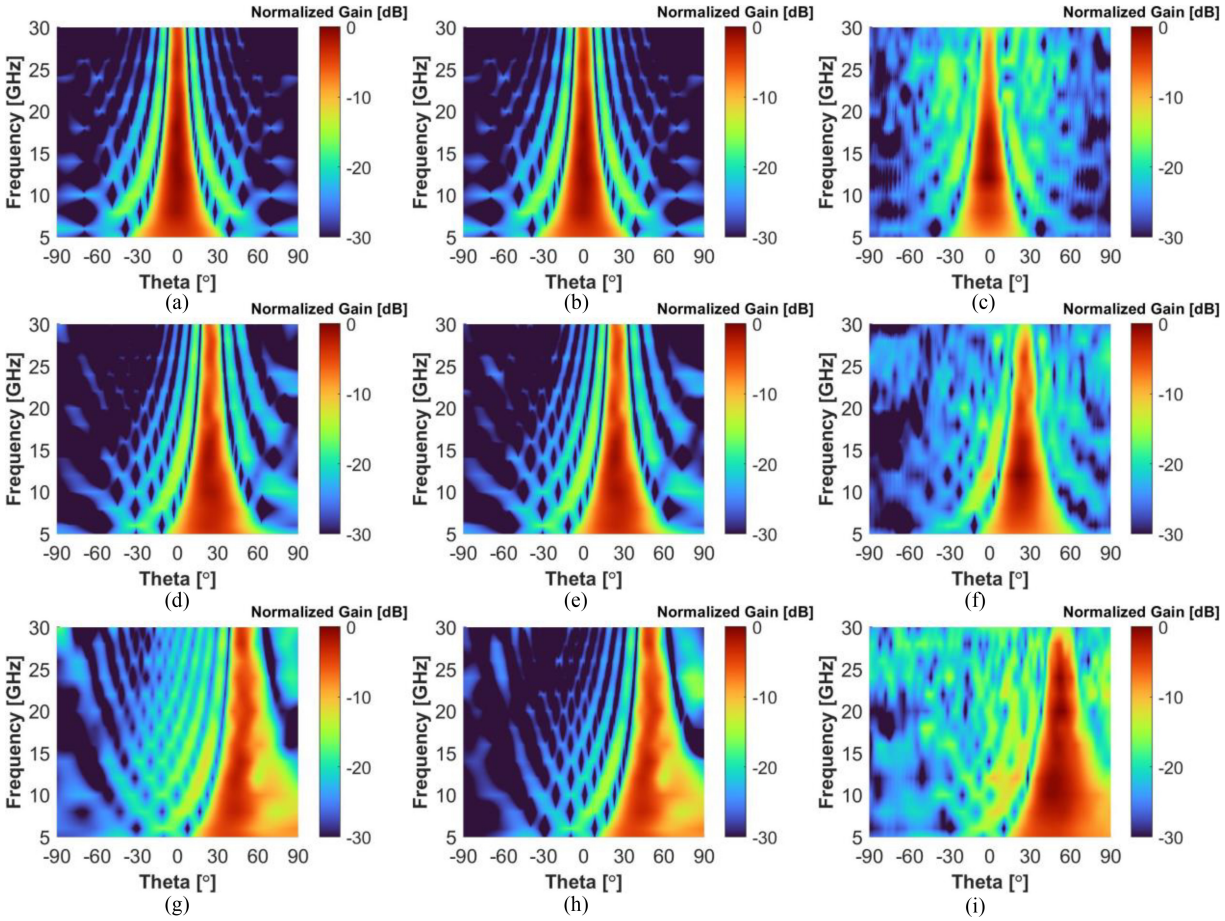

FIGURE 12. Normalized array pattern vs. scan angle and frequency for the TDU-A defined in Fig. 8. Pattern from model without including delay error steered to (a) 0°, (d) 25°, and (g) 50°, pattern from model when including delay error steered to (b) 0°, (e) 25°, and (h) 50°, and the measured patterns from hardware steering to (c) 0°, (f) 25°, and (i) 50°.

and f_0 is the frequency at which the AF is being evaluated. For the following examples, we assume a uniform amplitude distribution with $|a_i| = 1, \forall i$ which is approximately true for our hardware demonstration, and the unwrapped phase excitation of each element weighting (i.e., ϕ_{a_i}) is obtained from a search method. The search method begins by finding the ideal phase excitation required as

$$\boldsymbol{\phi}_{\boldsymbol{a_i}} = -k_0 \boldsymbol{r_i} \sin(\theta_{steer}) \tag{21}$$

where ϕ_{a_i} is the ideal phase excitation at the i^{th} antenna element, $k_0 = 2\pi/\lambda_0$ is the wavenumber and λ_0 is the wavelength, and θ_{steer} is the desired beam steering direction in degrees. Then we find the ideal delay as

$$\boldsymbol{\tau}_{\boldsymbol{a_i}} = \frac{-\boldsymbol{\phi}_{\boldsymbol{a_i}}}{f_0\ 360}. \tag{22}$$

where $\boldsymbol{\tau}_{\boldsymbol{a_i}}$ is the ideal time delay required at the i^{th} antenna element. The TDUs of each path are then configured to provide a total delay at each element which minimizes the error between the ideal state and the quantized bit selection. Note that these the UWB nature of the TDU-A. Once TDU settings are found from a frequency of choice, equations (20) – (22) can be worked backwards to plot AF at any desired frequency.' 'The Vivaldi antenna element is simulated by feeding the 8th element of a 20-element array with all other elements terminated in 50 Ω in order to find the embedded element pattern within the presence of adjacent array elements [7]. The normalized elevation plane radiation patterns obtained from the PAA model without accounting for delay error (i.e., only following the method outlined in [9]) are presented in Figs. 12(a), (d), and (g) as a function of frequency. These patterns clearly show that the true time delay nature of the feed network successfully ensuring that the peak of the radiation pattern is maintained at the desired angle across the UWB frequency. As expected, it is also observed that the beamwidth of the radiation pattern decreases with increasing frequency. However, side-lobe degradation at extreme steer angles can be observed in Fig. 12 (g) when the array is steered to 50°. The normalized elevation plane radiation patterns obtained from the PAA model with delay errors accounted are presented in Figs. 12(b), (e), and (h) as a function of frequency. The same characteristics are observed as before, however now the side lobe degradation at extreme steers is no longer present, as expected. The measured normalized radiation patterns from the fabricated PAAs are shown in Figs. 12(b),

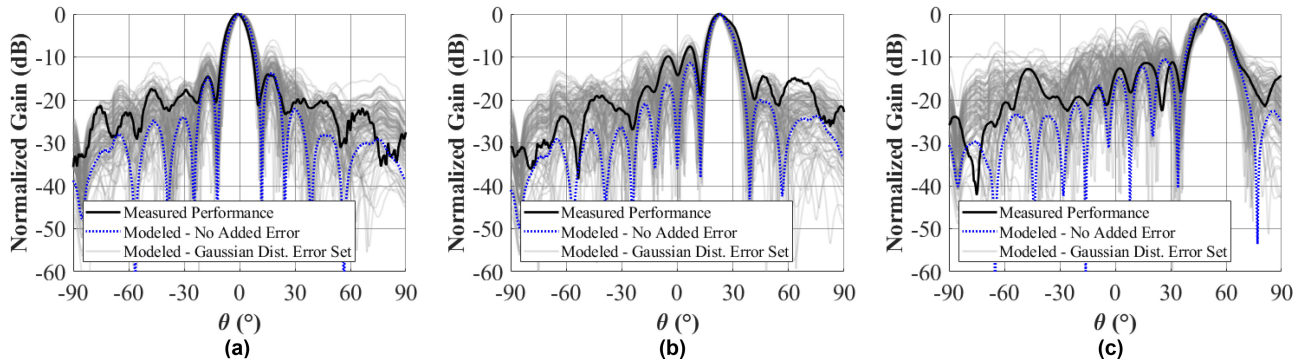

FIGURE 13. Comparison of 18 GHz measurement (bold plots) vs 100 iterations of modeled performance (light gray plots) within the family of expected delay errors in the RF-fanout steered to (a) 0°, (b) 25°, and (c) 50°.

(d), and (f). The frequency dependent steering direction and beamwidth characteristics of the measured radiation pattern agrees well with those obtained from the PAA model and the mainbeam beamwidths are nearly identical. On the other hand, the SLL performance is degraded due to the individual components of the TDU-A (i.e., TDUs and dividers) as well as the antenna array being designed independent of each other, since the TDU-A is designed prior to the individual component design, and then stitched together in a final design as well as the loss in the divider network not included in the modeled simulation. The smearing of the measured pattern (i.e., shifts in the side lobe location and amplitude compared to simulation), occurs due to the time delay errors discussed in Section II of this manuscript which may be calibrated. The cause of the smearing is illustrated in Fig. 13 at 18 GHz, approximately the center of the design bandwidth, by comparing the measured results with two sets of PAA models: (1) a pattern with no random error distributed throughout the array (i.e., "Modeled – No Added Error" in Fig. 13), and (2) a set of 100 array patterns with random errors distributed as a Gaussian PDF across the array elements as defined in Section II-D (i.e., "Modeled – Gaussian Dist. Error Set" in Fig. 13). The worst case SLL performance of Fig. 13 is shown in (b) at $\sim 8°$ which is due to the random stacking of delay errors peaking at 18 GHz and a scan of 25°; however, the performance falls within the set of performance with random errors distributed as predicted. The amplitude variation across the 16-way divider and TDUs was simulated and is approximately ± 0.3 dB at 18 GHz which was determined to be of negligible contribution to the side lobe level performance degradation. An exhaustive set of figures over the entire 5-30 GHz would be impractical in this manuscript, so 18 GHz was chosen as a representation; however, these figures were generated and verified at many other frequencies spaning the entirety of the bandwidth but left out for brevity. Fig. 13 shows that the measured performance lies within the set of 100 modeled patterns with error distribution showing correlation to predicted performance in Section II. Therefore, the TDU-A has the necessary range to be adjusted and achieve approximately the modeled performance through calibration, which is routine for these arrays, as shown in [13], [14], [15], [16], [17], [18].

V. CONCLUSION

An approach for including practical time delay errors in the optimization of a UWB PAA feed network to ensure sufficient time delay range at wide scan angles has been introduced and modeled for the first time. Specifically, the effects of time delay errors due to frequency dependent variations in VSWR, divider isolation and load mismatch, and dispersion were calculated and included in the optimization algorithm to determine a robust TDU-A. The efficacy of the method outlined in this manuscript is implemented and verified experimentally, for the first time, by three 16 element linear PAA test articles with an optimized TDU-A operating from 5 GHz to 30 GHz with beams steered towards 0°, 25°, and 50°. The components were designed independently to emulate a representative architecture design, where the component characteristics across frequency are not necessarily known *a priori*. The simulated and measured performance demonstrated UWB operation with stable radiation patterns.

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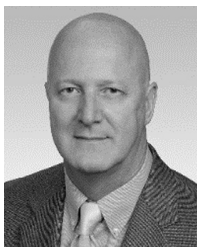
DANIEL A. RAMIREZ (Member, IEEE) received the B.S. degree in electrical engineering from the University of Central Florida in 2013, and the M.S. degree in electrical engineering from the University of South Florida in 2017, where he is currently pursuing the Ph.D. degree focusing on phased antenna arrays (PAAs).

Since 2013, he has been an RF Engineer with L3Harris Technologies, Palm Bay, FL, USA, where he has designed passive and active MMICs in GaAs and GaN technologies, modeled component packaging, and is currently contributing in system architecting for PAAs.



W. JOEL D. JOHNSON (Senior Member, IEEE) received the B.S. degree in electrical engineering from Auburn University, the M.S. degree in electrical engineering (Control Theory Thesis: Robust Control of RF Power Systems for Particle Accelerators) from the University of New Mexico, and the Ph.D. degree in electrical engineering (Approximation Theory dissertation: Rational Fraction Approximations for Passive Network Functions) from the University of South Florida.

Prior to joining Harris, he worked with Raytheon, where he worked on large simulations for 3-Φ power electronics and kilowatt class filters for power electronics, CME, where he worked on credit card size low power radios, and Los Alamos National Laboratory, where he worked on electron and proton particle accelerators as well as free-electron lasers. He is an Advanced Technology Manager within the IRAD office for SAS with 35+ years of experience; and has worked with Harris Corporation for 18+ years. He has been the PI for numerous RF and Communication IRADs and IPT Leader for several Programs of Record within SAS. He has published more than 55 papers in conferences and peer-reviewed journals. He has technical expertise in software defined radio development (both software and hardware), phased-array antenna RF electronics, RF systems engineering (link budgets, RF architectures, and manet planning), RF component design, control systems, and megawatt-class pulse-power systems.

GOKHAN MUMCU (Senior Member, IEEE) was born in Bursa, Turkey, in 1982. He received the B.S. degree in electrical engineering from Bilkent University, Ankara, Turkey, in 2003, and the M.S. and Ph.D. degrees in electrical and computer engineering from The Ohio State University, Columbus, OH, USA, in 2005 and 2008, respectively.

He is currently a Professor with the Electrical Engineering Department, University of South Florida, Tampa, FL, USA. His research interests include reconfigurable antennas and RF circuits with their mm-Wave applications, additive manufacturing of structural antennas and phased array antennas with integrated RF electronics, microfluidics for highly reconfigurable RF devices, and new concepts (e.g., metamaterials, volumetric 3-D reactive loading, polymers) for designing conformal, miniature, and multifunctional antennas. He was the recipient of the 2014 CAREER Award from the U.S. National Science Foundation, the 2014 Faculty Outstanding Research Award from the University of South Florida, and the 2008 Outstanding Dissertation Award of The Ohio State University, ElectroScience Laboratory. He was the recipient of the 1999 International Education Fellowship of the Turkish Ministry of Education. He ranked first on the national university entrance exam taken annually by over 1.5 million Turkish students in 1999. He was the Technical Program Committee Chair of the 2013 IEEE International Symposium on Antennas and Propagation and USNC/URSI National Radio Science Meeting, 2016 International Workshop on Antenna Technology, and 2022 IEEE Wireless and Microwave Technology Conference (WAMICON). In addition, he was the General Chair of IEEE WAMICON 2024.