DESIGN AND MANUFACTURE OF QUANTUM-CONFINED SI LIGHT SOURCES

A.W. Bogalecki[1] and M. du Plessis[2]

[1] and [2] Carl and Emily Fuchs Institute for Microelectronics, Dept. of Electrical, Electronic & Computer Engineering, Corner of University Road and Lynnwood Road, University of Pretoria, Pretoria 0002, South Africa
[1] E-mail: alfons.bogalecki@up.ac.za
[2] E-mail: monuko@up.ac.za

Abstract: To investigate quantum confinement effects on silicon (Si) light source electroluminescence (EL), nanometre-scale Si finger junctions were manufactured in a fully customized silicon-on-insulator (SOI) production technology. The wafers were manufactured in the cleanroom using an electron-beam pattern generator (EPG). The SOI light source with the highest irradiance emitted about 9 times more optical power around λ = 850 nm than a 0.35 µm bulk-CMOS avalanche light-source operating at the same current. It is shown that the buried oxide (BOX) layer in a SOI process could be used to reflect about 25 % of otherwise lost downward-radiated light back up to increase the external power efficiency of SOI light sources.

Key words: Nanometre-scale SOI, Silicon light source, Quantum confinement, Silicon electroluminescence.

1. INTRODUCTION

1.1. Problem statement

While on-chip silicon (Si) optical transmission, detection and manipulation elements are already practically achievable [1], a suitably efficient on-chip Si light source is not yet available. Although light emission from Si was observed as early as 1955 [1] and its high-speed capability [2] and long-term reliability [3] are established, the major reason for the inherently weak light emission of Si is its indirect band-gap [5]. While alternative light-sources have been proposed [1], most require special manufacturing steps that are not easily implemented in the currently prevailing CMOS manufacturing technology.

The authors have been developing Si light sources since 1992 [5]. Si (electroluminescence) EL improvement research within the INSiAVA[1] project has focussed on promising light source configurations that include *inter alia* avalanche, punch-through and carrier-injection [6] Si light sources.

1.2. Quantum confinement

EL enhancement factors of up to 30, due to quantum-mechanical confinement in ultra-thin Si compared to bulk devices, have been reported ([7] - [10]). References [7] and [8] reported a strong efficiency improvement in forward-biased SOI LEDs on a buried oxide (BOX) when the thickness of the regions shown in Figure 1 was reduced. The dramatic increase in integrated EL with reduced device layer thickness (Figure 2) was attributed to the suppression of non-radiative recombination.

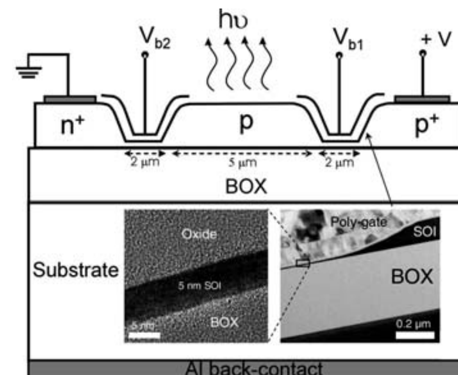

Figure 1: SOI LED manufactured in [7] and [8].

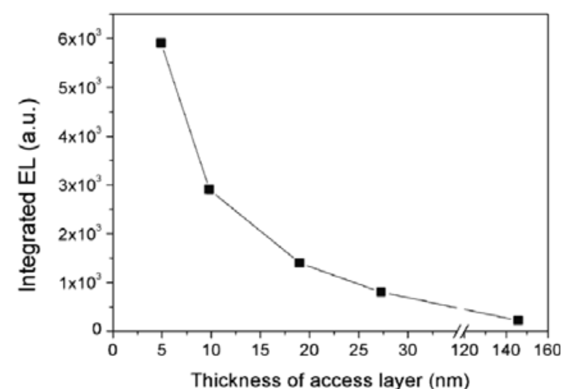

Figure 2: EL intensity against access layer thickness [8].

The abovementioned SOI light sources are only thin in one dimension (1D), their planar thickness, with device

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widths ranging between 20 and 60 µm. It should also be noted that their *pn*-junctions are located outside the thinned area.

1.3. Objective

The main purpose of this work was to design and manufacture SOI light sources that would enable the investigation of quantum confinement effects on EL characteristics like external power efficiency and spectral emission in avalanche, punch-through and carrier-injection Si light sources. Instead of just creating planar thin 1D quantum-confined SOI light sources, the technical objective was to design and manufacture devices that are smaller in two dimensions, i.e. two-dimensional (2D) quantum-confined SOI light sources. With reference to Figure 3, the following finger junction dimensions were targeted:

$$5\ \text{nm} \le t \le 100\ \text{nm}, \tag{1}$$

$$10\ \text{nm} \le w \le 100\ \text{nm and} \tag{2}$$

$$200\ \text{nm} \le l \le 400\ \text{nm}. \tag{3}$$

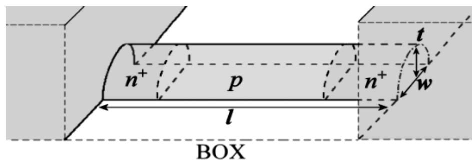

Figure 3: Generalized SOI finger junction dimensions.

Manufacturing larger rectangular Si structures and selectively oxidizing these created the desired thinner Si fingers. Nanometre-scale Si wires had already been manufactured through oxidation [12], but *pn*-junctions had, to our knowledge, never been implemented inside such thin Si wires.

1.4. Punch-through EL enhancement

Figure 4 shows two heavily doped p^+ end regions spaced a distance W_P apart by a lower doped *n*-type drift region.

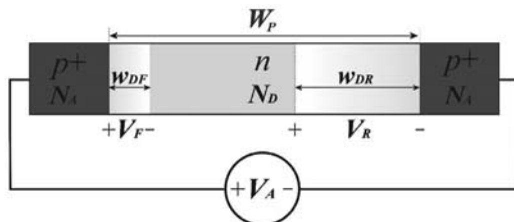

Figure 4: Punch-through variable definitions.

The applied voltage V_A can be increased to the punch-through voltage V_{PT} where the expanding reverse bias depletion region reaches the forward-biased depletion region so that $w_{DF} + w_{DR} = W_P$. At punch-through, the lowered energy barrier of the forward-biased junction injects a larger thermionic hole current that makes more minority carriers in the reverse-bias depletion region available for avalanche multiplication and radiative recombination. Achieving a higher avalanche current at lower terminal voltage also implies that the power efficiency of a punch-through light source is higher than the power efficiency of a single avalanching *pn*-junction.

2. PHYSICAL AND OPTICAL SIMULATION

Simulations were useful during the design stage to predict physical and optical properties achievable at the end of the manufacturing process.

2.1. Impurity redistribution during oxidation

The low diffusivity and solubility of arsenic (As) in SiO_2 results in the "snow-shovel" effect that causes As to pile up against the moving SiO_2 boundary during thermal oxidation [13]. Boron (B) with its higher diffusivity and solubility in SiO_2 is absorbed into the SiO_2 during thermal oxidation, therefore decreasing its concentration in the Si [14]. Since the lower B background doping concentration of n^+p junctions plays a larger role in determining junction characteristics like depletion region width w_d than the higher As concentration, only the spatial B concentration variation with thermal oxidation was further considered. The SOI B concentration $C(y,t)$ as a function of distance y from the BOX-Si interface and oxidation time t during thermal oxidation can be expressed as [14]

$$\frac{C(y,t)}{N_B} = 1 - \frac{\dfrac{k-m}{2}\sqrt{\dfrac{B\pi}{D_B}}\left\{\mathrm{erfc}\left(\dfrac{l-m\sqrt{Bt}-y}{2\sqrt{D_B t}}\right)+\mathrm{erfc}\left(\dfrac{l-m\sqrt{Bt}+y}{2\sqrt{D_B t}}\right)\right\}}{1-\mathrm{e}^{-\left(\frac{l-m\sqrt{Bt}}{\sqrt{D_B t}}\right)^2}+\dfrac{k-m}{2}\sqrt{\dfrac{B\pi}{D_B}}\left\{1+\mathrm{erfc}\left(\dfrac{l-m\sqrt{Bt}}{2\sqrt{D_B t}}\right)\right\}} \tag{4}$$

where:

- m ≈ 0.44 is the ratio of Si removed to SiO_2 thickness grown during oxidation,
- B = parabolic SiO_2 growth-rate constant,
- D_B = B diffusion constant,
- l = initial SOI active layer thickness,
- k = C_{SiO2}/C_{Si} is the segregation coefficient,
- C_{SiO2} = B concentration on the SiO_2 side of the Si/SiO_2 boundary,
- C_{Si} = B concentration on the Si side of the same interface.

Figure 5 shows the simulated B concentration decrease from the initial implanted concentration during successive oxidations. Prior knowledge of oxidation steps therefore allowed specifying the initial B implantation dose so that the desired final average finger background B concentration of about 10^{17} cm^{-3} would be achievable. In reality, some B segregation and re-diffusion into the Si also occurs at the BOX interface, but was ignored in the simulation shown in Figure 5.

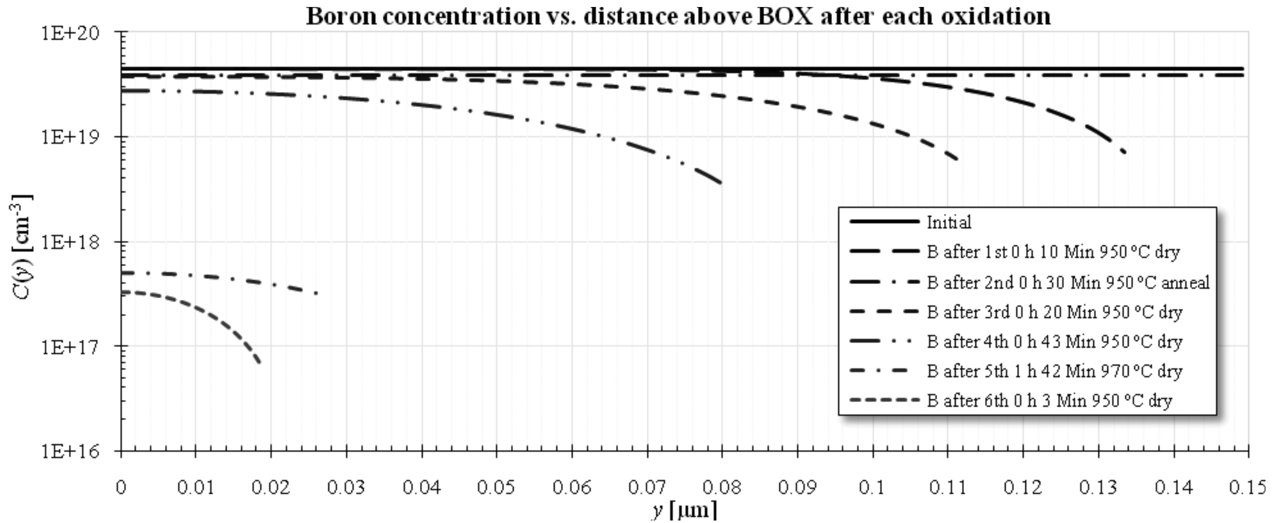

Figure 5: Boron redistribution during thermal oxidation and anneal processing steps.

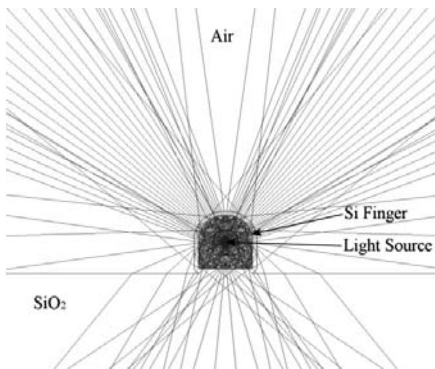

Figure 6: Simulated SOI finger spatial light radiation.

2.2. Optical radiation simulation

Employing the geometric-optical IME RAYTRACE ray-tracing software enabled the simulation of spatial light radiation characteristics of the Si fingers with varying finger geometries and light source locations.

Figure 6, for example, shows how light generated at the centre of a finger with rounded corners focuses into four lobes (recognizable by higher ray density) emanating from the rounded top surface of the Si finger.

It was *inter alia* determined that the maximum useful light emission directed away from the chip surface is achieved with a hemispherical round top finger surface to minimize internal reflection beyond the critical interface incidence angle and a flat bottom surface to maximize reflection back to the top surface.

3. DESIGN

3.1. Lithography

As indicated in Table 1, the small geometries and precise pattern alignment of the current work required electron-beam lithography (EBL), but the single beam EBL scan exposure is too slow to write all features across wafers. Hence a photolithographic mask aligner was used for patterning large-area geometries while a JEOL JBX-9300FS EPG was used for defining fine lines accurately.

Table 1: Photolithography and EBL Comparison.

Aspect	Photolithography	EBL
Wavelength/spot-size	≈ 300 nm	≈ 2 nm
Minimum feature size	≈ 0.5 µm	≈ 6 nm
Alignment accuracy	> 1 µm	> 6 nm
Wafer exposure speed	Whole wafer at once Fast: Minutes	Serial scanning beam Very slow: hours

3.2. 2D-confined SOI finger light sources

Figure 7 defines the dimensions of the pre-oxidized avalanche and punch-through SOI finger light sources.

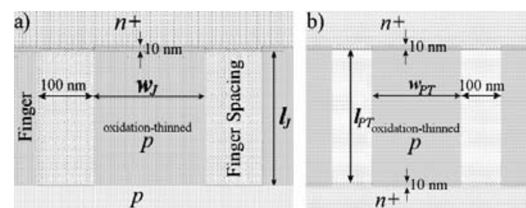

Figure 7: a) Avalanche and b) punch-through finger layout dimensions.

The Si island regions above and below the fingers remained thick while an EBL-written oxidation mask opening across the fingers allowed selective oxidation thinning of the SOI fingers. The dimensions of the devices shown in Figure 7 had to comply with the following specifications to ensure proper functionality:

$$l_J \geq w_d + d_{Ox} + 3\Delta R_{\perp As} \approx 226\text{ nm} \quad (5)$$

$$l_{PT} \approx w_d + 2(d_{Ox} + 3\Delta R_{\perp As}) \approx 352\text{ nm} \quad (6)$$

$$w_J = w_{PT} \approx 2t_{Si} \quad (7)$$

where

w_d = reverse bias depletion region width at breakdown,

d_{Ox} = maximum As oxidation diffusion after implant,
$\Delta R_{\perp As}$= transverse As implantation straggle,
t_{Si} = initial Si thickness (100 nm - 150 nm).
Relations (5) and (6) ensured that the fingers were long enough to accommodate the complete depletion region width after the implanted As (with its horizontal implant straggle) has diffused into the fingers after oxidation while equation (7) aimed to create semi-circular round fingers by assuming isotropic finger shaping oxidation that would thin the Si fingers equally from all sides. Implemented finger dimensions are listed in Table 3. The 30 µm x 34 µm SOI light source layout in Figure 8 depicts how 100 fingers are placed in parallel between thicker and larger Si islands that allow electrical biasing through the interconnect metallization.

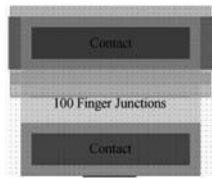

Figure 8: 100-finger junction device layout.

4. MANUFACTURE

Table 2 summarizes the processing steps and equipment involved in the SOI light source manufacture.

Table 2: Process flow overview.

Step	Action	Equipment	Graphical representation
1	Si thinning	Furnace, Reflective spectrometer	p^- Si ≈ 150 nm; BOX; Handle
2	Blanket B implant	Ion implanter	p Si; BOX; Handle
3	Si island definition	PECVD, Mask aligner, RIE	Si Island; BOX; Handle
4	As implant	PECVD, EPG, Mask aligner, RIE, Ion implanter	n+; p; BOX; Handle
5	Finger definition	EPG, RIE	n+; p; BOX
6	Finger oxidation	PECVD, EPG, Furnace	SiO_2; n+; p; BOX
7	Metallization	PECVD, Mask aligner, Sputterer	Al; Al
8	Si isolation spacing	Mask aligner	n+; p; BOX

Since no standard process recipe was employable, the complete manufacturing process had to be designed on self-obtained equipment characterization data, material and chemical properties. Consistent results and acceptable manufacturing performance were ensured through process control and monitoring that employed simultaneous processing of monitor wafer pieces and measurement of on-chip test-structures that could be analyzed with a SEM, a reflective spectrometer (to measure thin film thicknesses) and a profilometer.

Figure 9 shows examples of three final SOI finger junction dimension achieved after finger thinning oxidation.

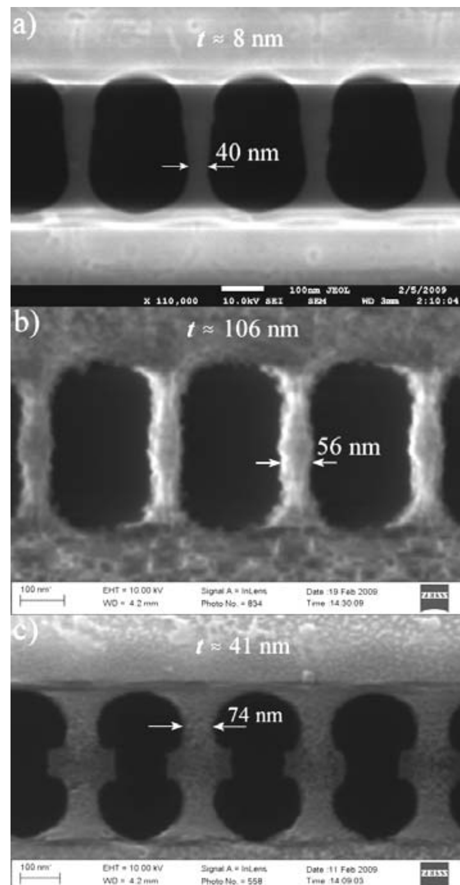

Figure 9: a) and b) avalanche and c) punch-through SOI finger final dimension examples after thinning oxidation with interpolated finger thickness estimates.

The finger thickness shown in Figure 9 are interpolated estimates from oxidation monitor island measurements. In contrast to the broad, but thin fingers in Figure 9 a), the fingers in Figure 9 b) are more thick than narrow. The punch-through SOI fingers in Figure 9 c) clearly shows how the heavily As doped Si oxidized faster than the lightly doped background. This oxidation effect created a drift and recombination region that is slightly larger than the heavily doped contact region, which should result in higher useful light emission from the light source since less light is lost due to internal reflection along the finger axis. Table 3 lists the on-mask and measured final SOI finger dimensions.

Table 3. Achieved SOI Finger Device Dimensions.

Dimension	Layout	Measured
l_J	230 nm	296 – 359 nm
w_J	200 nm – 300 nm	38 nm – 101 nm
l_{PT}	320 nm – 11 µm	348 nm – 11 µm
w_{PT}	220 nm – 12 µm	30 nm – 11.9 µm

5. MEASUREMENT

Table 4 and Figure 10 depict the finger dimensions and measured electrical characteristics of punch-through light sources selected for comparative optical characterization.

Table 4. Selected SOI light source finger dimensions.

Device	w_{PT}	l_{PT}
D1b	11.9 µm	11.8 µm
D2b	11.9 µm	11 µm
D4b	5.9 µm	4 µm
D5b	5.9 µm	4 µm
n1b	485 nm	240 nm
n2b	385 nm	240 nm

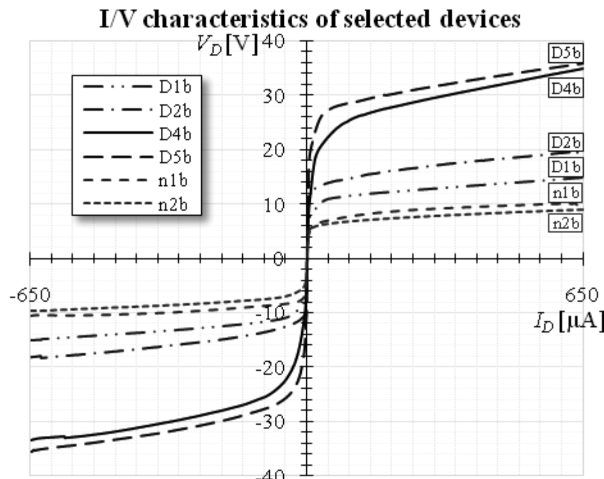

Figure 10: I-V characteristic of selected SOI light sources.

D4b and *D5b* should have high light generation efficiencies, since a higher series resistance corresponds to a thinner Si device layer and an increased breakdown voltage is characteristic of quantum-confinement. Figure 11 shows the light generation of fingered punch-through SOI light source *n1b* at 650 µA.

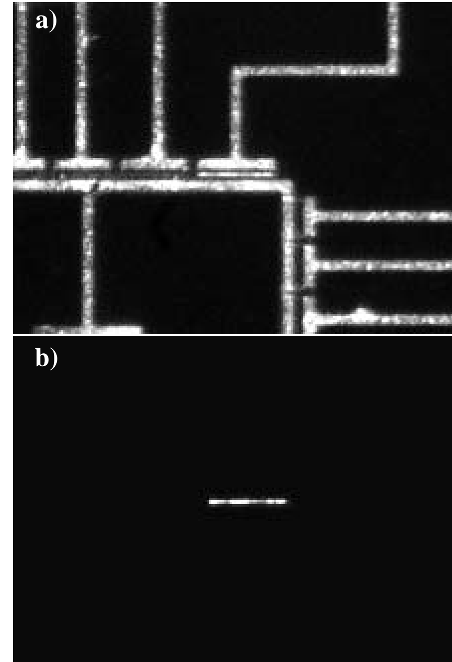

Figure 11: a) Illuminated and b) non-illuminated light generation of punch-through SOI light source *n1b*.

Figure 12 compares the spectrum of the SOI punch-through light source with the highest optical power (*D4b*) to the average optical power of 0.35 µm avalanche CMOS light sources also biased at I_D = 650 µA and measured with the same characterization setup. While the avalanche light sources peak around $\lambda \approx$ 660 nm ($E_{Ph} \approx$ 1.88 eV) the SOI punch-through light source peak around 850 nm ($E_{Ph} \approx$ 1.46 eV) is about 9 times higher. Since significant infrared radiation peaks were observed in Si nano-crystal EL and photoluminescence experiments [15], this could be indicative of quantum confinement. The lower photon energy at longer wavelengths also implies that that the thickness-confined SOI light sources have significantly higher quantum conversion efficiencies than bulk-CMOS avalanche light sources.

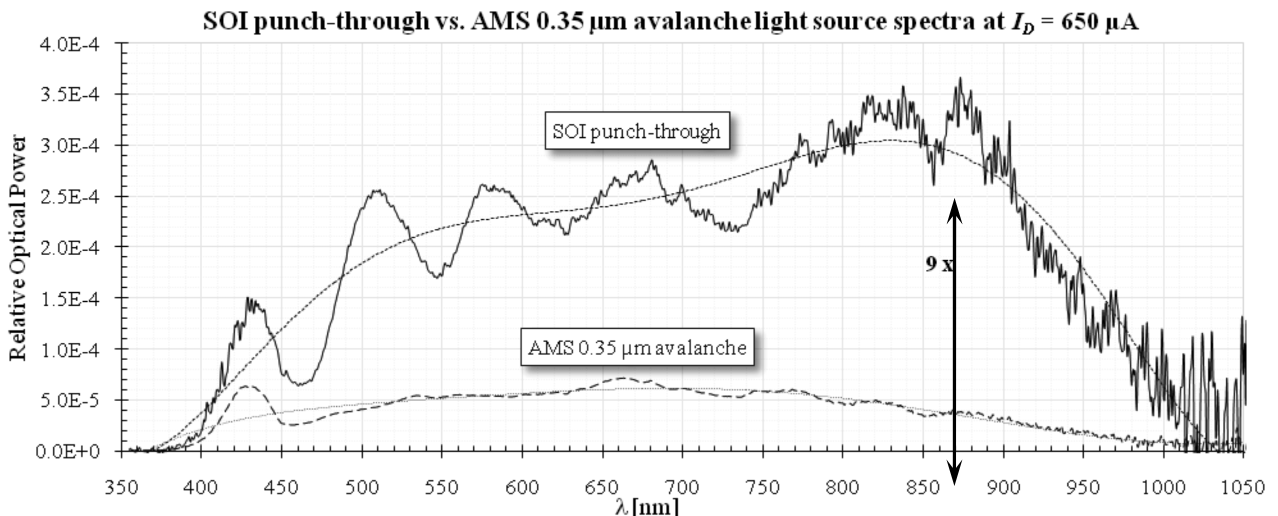

Figure 12: Spectra comparison of SOI punch-through and AMS 0.35 µm CMOS light-sources.

The periodic optical power variation of all measured SOI light sources is due to light reflection off the SiO_2 BOX layer covering the SOI wafer Si handle. Employing the stack transmission model, the best-fitting simulated Si-SiO_2-air stack reflection peaks were achieved for $t_{BOX} \approx$ 860 nm (Figure 13).

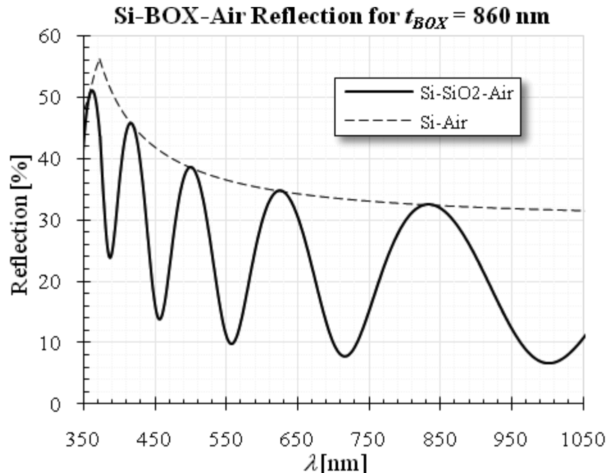

Figure 13: Simulated BOX reflection for t_{BOX} = 860 nm.

Figure 13 shows that an average of 25 % of the light that would have been lost through downward radiation is reflected back up as useful light.

6. CONCLUSION

All measured thickness-confined SOI light sources displayed a pronounced optical power for $0.6 < \lambda < 1$ µm. The SOI light source with the highest optical power output emitted about 9 times more optical power around λ = 850 nm than a 0.35 µm bulk-CMOS avalanche light-source operating at the same current. It has also been shown that the BOX layer in a SOI process could be used to reflect about 25 % of the light that would usually be lost to downward radiation back up, thereby increasing the external power efficiency of SOI light sources.

7. REFERENCES

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