QUANTITATIVE FEEDBACK THEORY DESIGN OF LINE CURRENT COMMUTATED HVDC CONTROL SYSTEMS

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Abstract: Line Current Commutated (LCC) HVDC systems consists of uncertain plants. These uncertainties are result of changes/disturbances in the ac networks or in the LCC HVDC system itself. Further uncertainties can be introduced due to simplified system modelling techniques. Quantitative Feedback Theory is a frequency-domain technique that utilises the Nichols chart to achieve a robust design over a specified region of uncertainty. The Quantitative Feedback Theory design philosophy was applied to design the LCC HVDC control system parameters. The stable start-up and step responses of the LCC HVDC system, for varying ac system conditions, conclusively validate the Quantitative Feedback Theory design method of the LCC HVDC control system parameters.

Keywords: HVDC, control system, uncertainty, Quantitative Feedback Theory

1. INTRODUCTION

Line Current Commutated (LCC) HVDC systems consists of uncertain plants. These uncertainties are result of changes/disturbances in the ac networks or in the LCC HVDC system itself. Further uncertainties can be introduced due to simplified system modelling techniques. Feedback control systems reduce the effects of uncertainty which may appear in different forms as disturbances or as other imperfections in the models used to design the feedback law [1]. Feedback also has the property of increasing linearity of the control system [1]. Therefore, negative feedback control is used to limit the effect of these uncertainties in the LCC HVDC system operation. However, feedback control systems have the inherent risk of instability [1].

Erikson et. al [3]. stated that there is a distinct need for quantitative methods for stability analysis of HVDC control systems. Based on a computer program developed by Persson [2] that calculated the rectifier current control transfer function of the uncompensated control loop, Erikkson [3] et. al. used Nyquist plots to analyse the stability of the LCC HVDC rectifier current control loop. Erikson et. al. [3] also used Bode plots and Nyquist plots to design a PI controller for a certain parametric rectifier current control plant. Freris et. al. [4] used Nyquist plot to analyze the stability of the compensated certain parametric rectifier current control loop of a dc transmission system connected between a rectifier with short circuit ratio 3.75 and inverter with an infinite short circuit ratio. Jovcic et. al. [5] used root locus diagrams to analyse the effect of phase locked loop gains on the stability of a certain parametric rectifier current control plant. Jovcic et. al. [6] also used root locus diagrams to analyse the difference of the direct current feedback control loop and the fast power feedback control loop for a certain parametric HVDC system.

Aten et. al. [7] states that little has been published by the industry on how classical control theory can be used to design HVDC control systems. Aten et. al [7] states that classical control theory can assist in determining stability margins and robustness of HVDC control system. Aten et. al. [7] used Bode plots to determine phase and gain margins for various rectifier and inverter short circuit ratios. Rahim et. al. [8] used modern control theory to design a robust damping controller for an HVDC link within a power system. Bode plots were used as the design tool for shaping of the loop transfer function. From the literature review, it is evident that although classical control theory has been superficially investigated to design LCC HVDC control systems, parametric plant uncertainty has not been investigated. Therefore this paper designs robust LCC HVDC control systems using Quantitative Feedback Theory, so as to accommodate parametric plant uncertainty.

2. QUANTITATIVE FEEDBACK THEORY

Quantitative feedback theory (QFT) was developed by Horowitz [11], to provide an effective approach for the design of control systems for uncertain plants and/or disturbances. QFT is a frequency-domain technique that utilises the Nichols chart to achieve a robust design over a specified region of uncertainty. The QFT design philosophy was applied to design the LCC HVDC control system parameters since LCC HVDC systems are naturally uncertain. The reasons for the uncertain nature of LCC HVDC systems are as follows:

1. AC systems' effective short circuit ratios are variable in nature.

2. The LCC HVDC plant transfer functions were developed from simulations thus introducing, errors even though minor, which can be considered/treated as plant uncertainty [12].
3. Linear LCC HVDC plant transfer functions were derived from nonlinear HVDC dynamics thus introducing errors even though minor, which can be considered/treated as plant uncertainty [12].

The designed controller should meet the performance specifications in spite of the variations of the parameters of the LCC HVDC plant models. QFT works directly with such uncertainties and does not require any particular representation. A key element of QFT is embedding the performance specifications at the onset of the design process. These specifications establish design goals that enhance and expedite the achievement of a successful design. The performance specifications includes percentage overshoot and settling time (t_s) which is defined as the time required by the step response to settle within $\pm\delta\%$ of the final value, where δ is defined.

One of the fundamental aspects in control design is the use of an accurate description of the plant dynamics. QFT involves frequency-domain arithmetic, therefore, the plant dynamics must be defined in terms of its frequency response. The term "template" is used to denote the collection of an uncertain plant's frequency responses at given frequencies. Samples of plant templates at different frequencies are illustrated in Figure 1. The use of templates alleviates the need to develop any particular plant model representation. Once the plant templates are developed, QFT converts closed-loop magnitude specifications into magnitude and phase constraints on a nominal open-loop function.

These constraints are called *QFT bounds* (illustrated in Figure 2). A detailed discussion on the method used to plot templates on the stability margin based on plant parameter uncertainty can be found in [11]. The size of the templates indicates whether or not a robust design is achievable. If a robust design is not possible, then the templates can be used as a metric in the reformation of the control design problem. Another aspect of the QFT design process is the ability to concurrently analyze frequency responses of the plant transfer functions that represent the non-linear dynamical system through its operating environment. This gives the designer insight into the behaviour of the system. The designer can use this insight for such things as picking out the key frequencies to use during the design process, as an indicator of potential problems such as non-minimum phase behaviour, and as a tool to compare the nonlinear system with the desired performance boundaries. Non-minimum phase behaviour occurs when the loop transfer function has real poles and zeros in the right half plane or even consists of dead-time.

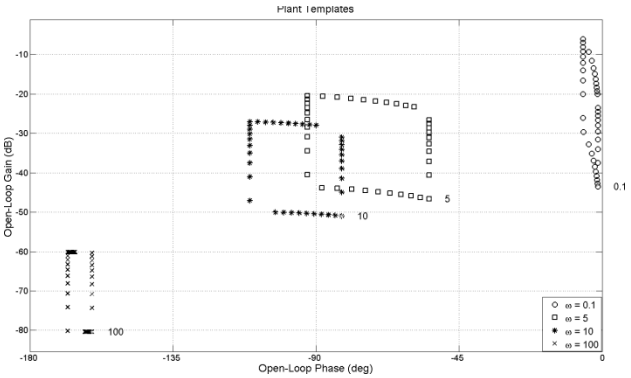

Figure 1: Plant Templates for various frequencies

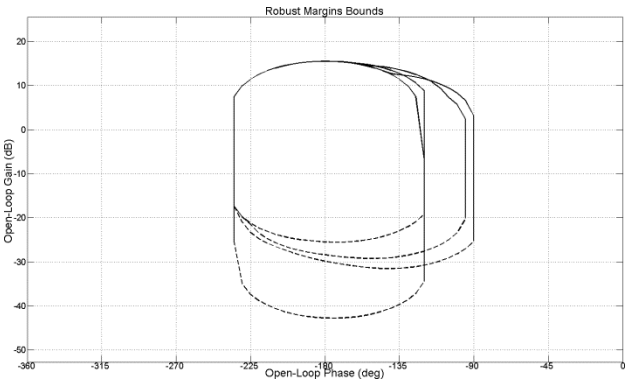

Figure 2: QFT Bounds at various frequencies

The non-minimum phase behaviour will restrict the maximum gain cross-over frequency and will therefore affect the achievement of the specifications. The plotting of the loop transfer functions on Nichols Chart gives the designer a first look at any areas of the design that may present problems during simulation and implementation. To obtain a successful control design, the controlled system must meet all of the specifications during simulation. If the controlled system fails any of the simulation tests, using the design elements of QFT, the designer can trace that failure back through the design process and make necessary adjustments to the design.

3. LCC HVDC CONTROL SYSTEM

The LCC HVDC scheme shown in Figure 3 represents a monopolar link or one pole of a bipolar link. The direct current flowing from the rectifier to the inverter is given by [10]:

$$I_d = \frac{V_{dor}.\cos\alpha_r - V_{doi}.\cos\gamma_i}{R_{cr} + R_L - R_{ci}} \quad (1)$$

By controlling the internal voltages ($V_{dor}.\cos\alpha_r$) and ($V_{doi}.\cos\gamma_i$), the direct voltage and the current (or power) can be controlled. This is accomplished continuously via the control system and the gate control of the valve firing angle.

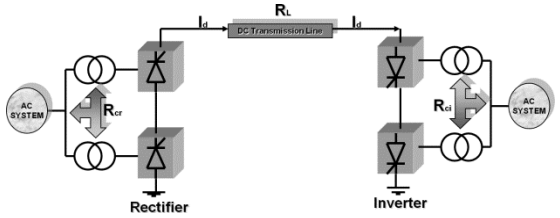

Figure 3: LCC HVDC Scheme

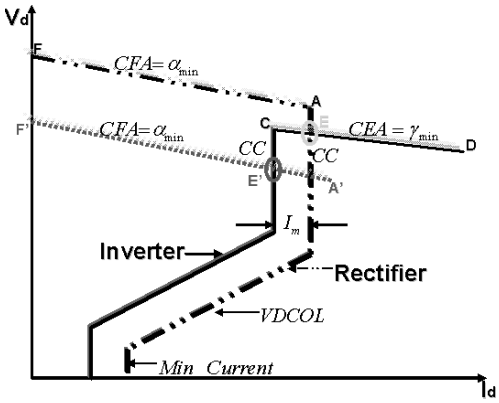

Figure 4: Steady-state V-I Control Characteristics

An important requirement for the satisfactory operation of the LCC HVDC link is the prevention of large direct current fluctuations by rapidly controlling the converters' internal voltages by manipulating the rectifier and inverter firing angles. In effect, the adjustment of the rectifier and inverter firing angles are utilized to improve the small signal stability of the HVDC control system.

To satisfy the fundamental requirements, the responsibilities for dc voltage control and dc current control are kept distinct and are assigned to separate converter stations. Under normal operation, the rectifier maintains constant dc current control (CC), and the inverter maintains constant direct voltage control (VC) by operating with constant extinction angle (CEA) [10]. The basis for the control philosophy is illustrated in Figure 4. Under normal operating conditions (represented by the intersection point E) the rectifier controls the direct current and the inverter controls the direct voltage. With a reduced rectifier voltage, the operating condition is represented by the intersection point E'. The inverter takes over the direct current control and the rectifier establishes the direct voltage. Under low voltage conditions, it is not be desirable or possible to maintain rated direct current or power [10]. The problems associated with operation under low voltage conditions may be prevented by using a "voltage dependent current order limit" (VDCOL) [10]. This limit reduces the maximum allowable direct current when the voltage drops below a predetermined value [10]. The VDCOL characteristic is a function of the dc voltage.

Figure 5 illustrates the scheme for practically implementing the LCC HVDC control system. It should be noted that the rectifier and inverter have the same control system structure. The VDCOL function strives to reduce the dc current order for reduced measured dc voltage. The static characteristics of the VDCOL function are displayed in Figure 6. The phase locked oscillator (PLO) is based on the Phase Vector technique [9]. This technique exploits trigonometric multiplication identities to form an error signal, which speeds up or slow down the PLO in order to match the phase. The output signal θ is a ramp synchronized to the Phase A commutating bus L-G voltage. The block diagram of the PLO is shown in Figure 7. Both the rectifier and the inverter have current control amplifier (CCA) function as illustrated in Figure 5. The main function of the current control amplifier is to improve the dynamic operation of current control loop. The main requirements of the current control loop are:

1. Fast enough step response
2. Insignificant current error at steady-state
3. Stable current control

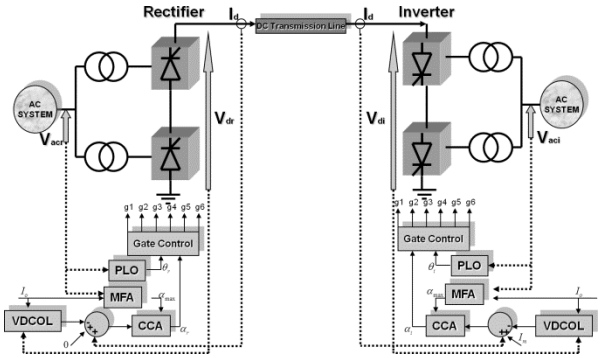

Figure 5: LCC HVDC Control System

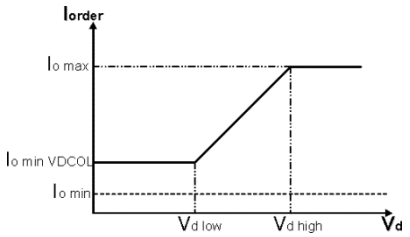

Figure 6: Static characteristics of VDCOL [10]

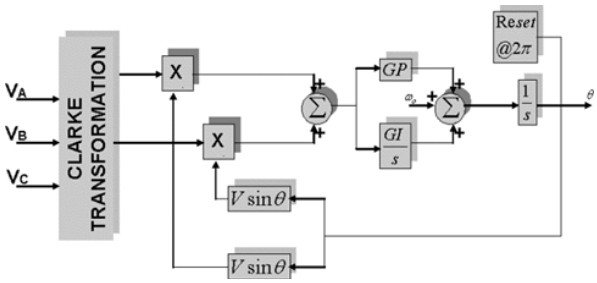

Figure 7: Phase Locked Oscillator (PLO) Implementation

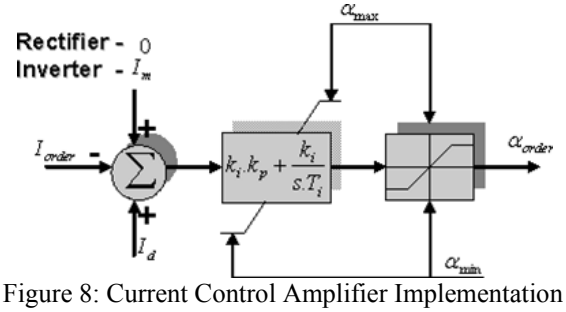

Figure 8: Current Control Amplifier Implementation

The CCA has a proportional part ($k_i.k_p$) and an integrating part ($\frac{k_i}{s.T_i}$), as illustrated in Figure 8. The CCA also has a summing junction, in which the difference between the current order, the current response and current margin is formed. The subsequent firing angle order is determined by the following equation:

$$\alpha_{order} = -\left[k_i.k_p + \frac{k_i}{s.T_i}\right](I_{order} - I_m - I_d) \quad (2)$$

The current controller's proportional gain and integral time constant parameters should be designed to achieve the best stability performance.

The gate control compares the firing order α_{order} to the phase locked ramp signal θ and produces the gate firing pulses.

4. PERFORMANCE SPECIFICATIONS AND CONTROL PROBLEM DEFINITION

Erikson et. al [3] specifies that a minimum phase margin of 40^o from the Nyquist point should be maintained for all frequencies. On the Nichols chart, the 40^o phase margin specification corresponds to the 6dB M-circle. Therefore the control problem is defined as:
"For LCC HVDC plant transfer functions (P_{cr} and P_{ci}) defined in [12], whose parameters vary according to the Tables defined in [12], design the fastest possible control system. The control system should be designed for the following operating conditions: the rectifier's ESCR varies from 6 to 8 and the inverter's ESCR varies from 6 to 8 with the nominal operating condition being rectifier's ESCR equal to 8 and inverter's ESCR equal to 8. The HVDC control system should be designed so as to maintain the 6dB stability margin for all frequencies."

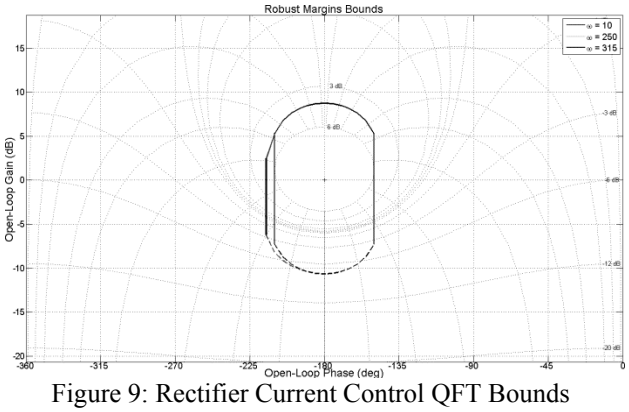

Figure 9: Rectifier Current Control QFT Bounds

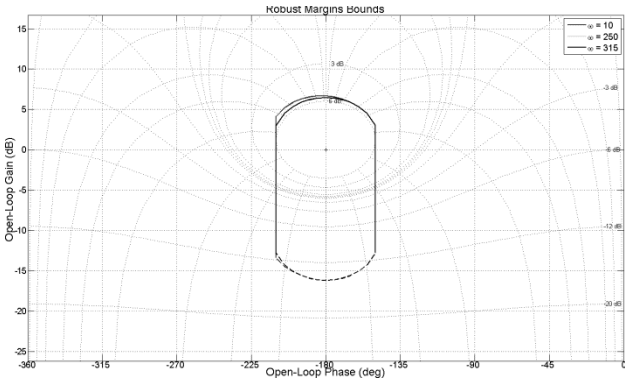

Figure 10: Inverter Current Control QFT Bounds

A fundamental element of the QFT design method is the generation of parametric uncertainty templates and the integration of these templates into the stability margin design bounds. Figure 9 illustrates how the stability margin is modified for nominal rectifier current control plant transfer function, according to parameter variations illustrated in Table 1 of reference [12]. Figure 10 illustrates how the stability margin is modified for nominal inverter current control plant transfer function, according to parameter variations illustrated in Table 2 of reference [12].

5. QFT DESIGN OF LCC HVDC CONTROL PARAMETERS

Since the stability design bounds have been derived, the parameters of the LCC HVDC control system can be designed. The following high-to-low frequency QFT design method was used:

1. The maximum possible gain cross-over frequency ω_{gc} was determined from the non-minimum phase-lag properties of the plant. This gain cross-over frequency will be attempted to be achieved by applying a proportional gain.
2. Then the magnitude of the loop transfer function will be increased, for ω approaching zero, as fast as possible. This will be achieved by applying a first-order integral term.

5.1. Rectifier Current Controller Design

Analysis of Table 1 [12], reveals that the largest time constant is 1.65msec, therefore the performance specifications for the Rectifier Current Controller are defined as:

Overshoot	< 5%
Settling Time (t_s)	< 24.75msec
Steady state error (δ)	< 2%
Gain Margin	< 6dB

The nominal rectifier current control plant is defined as [12]:

$$P_{cr}(s) = e^{-1.65\times10^{-3}s}\left(\frac{-0.026s^3 - 3.424s^2 - 2351s - 9.732\times10^4}{s^3 + 132.7s^2 + 9.049\times10^4 s + 3.829\times10^6}\right)$$

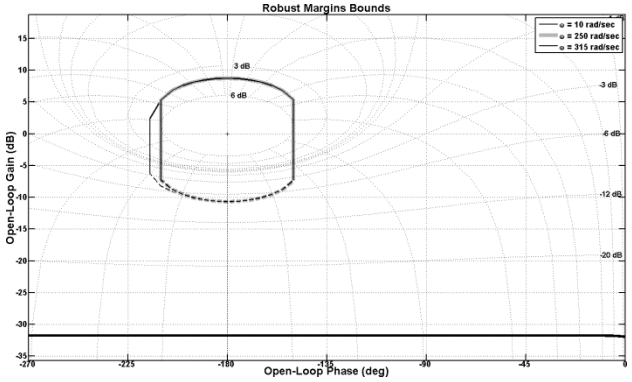

Figure 11: Nichols Plot of $-P_{cr}(s)$

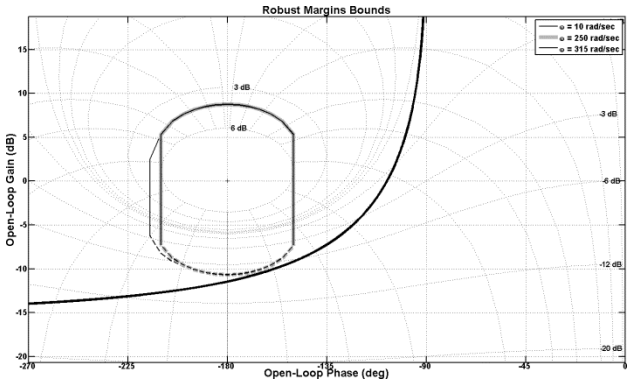

Figure 12: Influence of the designed PI controller on $P_{cr}(s)$

The negative of this plant transfer function is plotted on Nichols Chart with the modified stability margin as shown in Figure 11. To achieve the maximum possible gain cross-over frequency, the gain of the controller was increased, ie k=6.3. To further improve the low frequency performance, a low frequency modifying controller term $(1+\omega_c/s)$ was be used, with ω_c=1750 rad/s. The gain and the low-order controller term define the parameters of the PI controller:

$$G(s) = -6.3\left(1 + 1750/s\right) \quad (3)$$

Equation (2) describes the actual controller parameters as:

$$G(s) = -\left(k_i.k_p + \frac{k_i}{s.T_i}\right) \quad (4)$$

Equating (3) and (4) and choosing T_i=1msec gives:

$k_i = 11.025$

$k_p = 0.57$

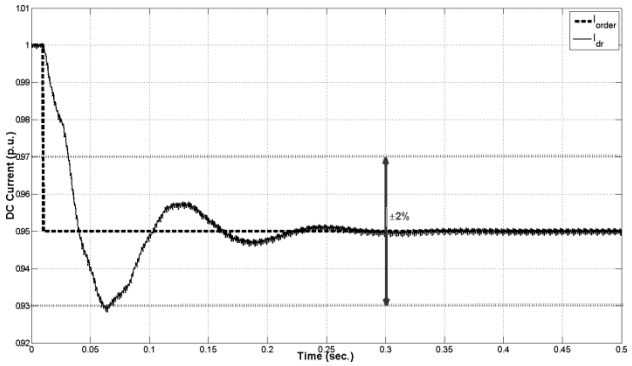

Figure 13: Rectifier DC Current Response

Performance Criterion	Expected	Actual
Overshoot	5%	2.1%
Settling Time (t_s)	24.75msec	23msec
Steady state error (δ)	<2%	<0.1%
Gain Margin	<6dB	<6Db

Table 1: Rectifier Current Controller Performance Assessment

The effect of the controller is displayed in Figure 12. To verify the performance of the control system, the following scenario was simulated in PSCAD/EMTDC: The rectifier's ESCR was set to 8 and the inverter's ESCR was set to 8. The HVDC system was configured so that the rectifier was in current control mode and the inverter was in voltage control mode. The inverter's firing angle was held constant at 138 degrees and the rectifier's current controller's parameters were set according to equation (3). After the HVDC system is run to steady state, the dc current order was decreased by 5%.The plant output response to the small signal transient is illustrated in Figure 13. The control system performance is evaluated in Table 1, which clearly illustrates that the rectifier controller design did meet the specified performance requirements.

5.2. Inverter Current Controller Design

Analysis of Table 2 of reference [12], reveals that the largest time constant is 0.89msec. It should be noted that there exists a 1msec communication time delay with regard to the current order being processed at the rectifier station and then transmitted to the inverter station. Therefore the specifications for the Inverter Current Controller are defined as:

Overshoot	< 5%
Settling Time (t_s)	< 28.35msec
Steady state error (δ)	< 2%
Gain Margin	< 6dB

The nominal rectifier current control plant is defined as [12]:

$$P_{ci}(s) = e^{-0.89\times10^{-3}s}\left(\frac{-0.02s^3 - 2.478s^2 - 1676s - 6.535\times10^4}{s^3 + 124.9s^2 + 8.388\times10^4 s + 3.348\times10^6}\right)$$

The negative of this plant transfer function is plotted on Nichols Chart with the modified stability margin as shown in Figure 14. To achieve the maximum possible gain cross-over frequency, the gain of the controller was increased, ie k=5.62. To further improve the low frequency performance, a low frequency modifying controller term $(1+\omega_c/s)$ was be used, with ω_c=2400 rad/s.

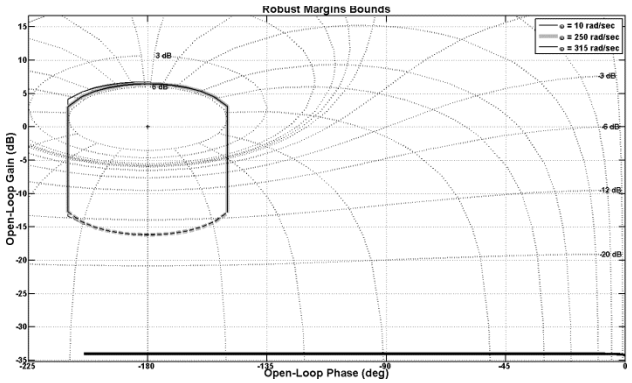

Figure 14: Nichols Plot of $-P_{ci}(s)$

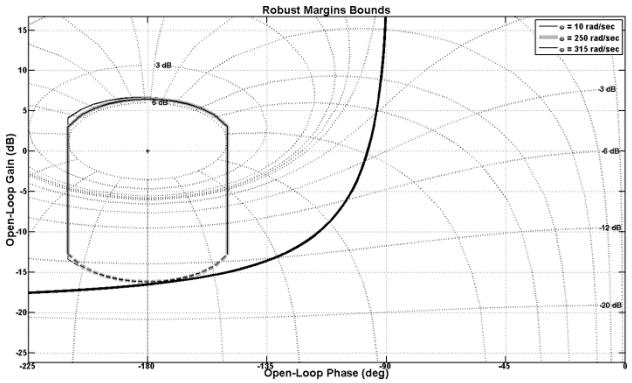

Figure 15: Influence of the designed PI controller on $P_{ci}(s)$

The gain and the low-order controller term define the parameters of the PI controller:

$$G(s) = -5.62\left(1 + 2400/s\right) \quad (5)$$

Equation (2) describes the actual controller parameters as:

$$G(s) = -\left(k_i.k_p + \frac{k_i}{s.T_i}\right) \quad (6)$$

Equating (5) and (6) and choosing T_i=1msec gives:

$k_i = 13.5$

$k_p = 0.417$

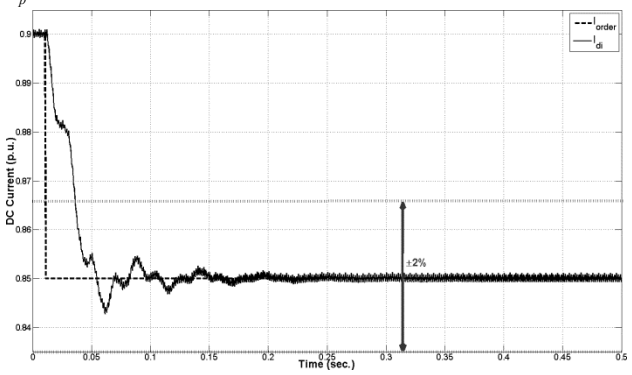

Figure 16: Inverter DC Current Response

Performance Criterion	Expected	Actual
Overshoot	5%	1.3%
Settling Time (t_s)	28.35msec	23msec
Steady state error (δ)	<2%	<0.13%
Gain Margin	<6dB	<6dB

Table 2: Inverter Current Controller Performance Assessment

The effect of the controller is displayed in Figure 15. To verify the performance of the control system, the following scenario was simulated in PSCAD/EMTDC:
The rectifier's ESCR was set to 8 and the inverter's ESCR was equal to 8. The HVDC system was configured so that the inverter was in current control mode and the rectifier was in voltage control mode. The rectifier's firing angle was held constant at 27 degrees and the inverter's current controller's parameters were set according to equation (5). After the HVDC system is run to steady state, the dc current order was decreased by 5%. The plant output response to the small signal transient is illustrated in Figure 16. The control system performance is evaluated in Table 2, which clearly illustrates that the inverter controller design does meet the specified performance requirements.

5.3. *Start-up Performance*

The design of the LCC HVDC control system has been sectionalized into separate design and analysis of THE control systems that constitute the LCC HVDC control system. The design and analysis of the complete LCC HVDC control system was validated by integrating the control systems as illustrated in Figure 5. The stability of the integrated LCC HVDC system was verified by simulating the following scenario in PSCAD/EMTDC:
The rectifier's ESCR was set to 8 and the inverter's ESCR was equal to 8. The firing angle of the inverter station is deblock first at $t_o = 10ms$. The rectifier's firing angle was deblocked at $t_1 = 50ms$ and then ramped up. The rectifier's current controller's parameters were set according to equation (3) and the inverter's current controller's parameters were set according to equation (5). Analysis of start-up response (Figure 17) reveals that the dc current increases after t_1. Between time t_3 and t_2, the dc voltage has not increased above the minimum required dc voltage (0.2 p.u.) as specified by the VDCOL, therefore the current order is constrained to the minimum current order (Rectifier – 0.3 p.u. and Inverter – 0.2 p.u.) as defined by the VDCOL. During this period of time, the designed LCC HVDC control system ensures that LCC HVDC system operates stably and according to the requirements of the VDCOL.

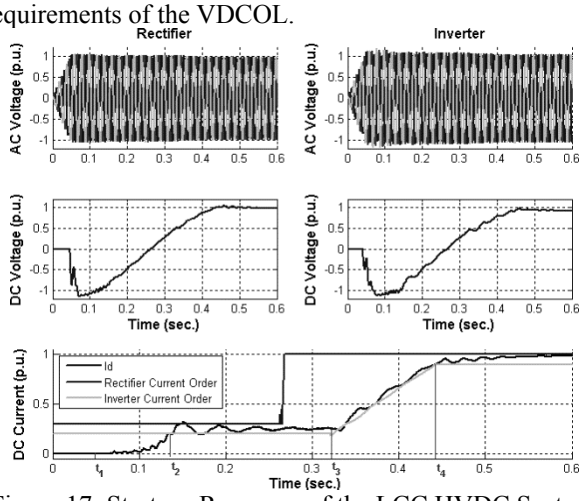

Figure 17: Start-up Response of the LCC HVDC System

Between time t_4 and t_3, the dc voltage increases above the minimum required dc voltage and the current order is determined by the inverter VDCOL. During this period of time, the designed LCC HVDC control system ensures that LCC HVDC system operates stably and according to the requirements of the inverter VDCOL. After time t_4, the inverter receives more current than is ordered therefore the current control moves to the rectifier station. During this current control transitional period, the designed LCC HVDC control system ensures that the LCC HVDC system operates stably and according to the requirements of the rectifier current control amplifier.

6. TRANSIENT ANALYSIS OF LCC HVDC CONTROL SYSTEMS

Transient analysis of an HVDC system provides insight into the interactions between the ac and dc systems. During the transient stability analysis, the rectifier and inverter ac systems' effective short circuit ratios were varied and the LCC HVDC system responses to small disturbances were analysed.

6.1. *Step decrease in rectifier ac system voltage*

The LCC HVDC system responses to a 5% stepped decrease in the rectifier ac system voltage, for varying ac system operating conditions were evaluated. The LCC HVDC system was simulated the following scenarios in PSCAD/EMTDC:

- The rectifier's ESCR was varied from 8 to 6
- The inverter's ESCR was varied from 8 to 6
- The rectifier's current controller's parameters were set according to equation (3)
- The inverter's current controller's parameters were set according to equation (5)
- After the LCC HVDC system is run to steady state, at $t_1 = 10ms$, the rectifier's ac system voltage is decreased by 5%.
- At $t_2 = 0.3\text{sec}$, the current order is decreased by 5%.

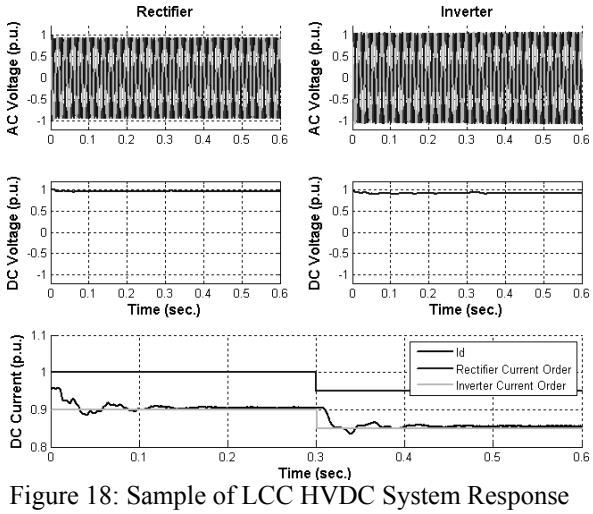

Figure 18: Sample of LCC HVDC System Response to a stepped decrease in the rectifier ac system's voltage

Constant Current Order					
Rectifier ESCR	Inverter ESCR	Characteristics			
		O.S (%)	t_s (msec)	Error (%)	Stable
8	8	1.2	43	0.6	Yes
6	8	1.3	22	0.5	Yes
8	6	2.1	49	0.4	Yes
6	6	2.0	28	0.5	Yes
5% Step Decrease in Current Order					
Rectifier ESCR	Inverter ESCR	Characteristics			
		O.S (%)	t_s (msec)	Error (%)	Stable
8	8	1.6	21	0.5	Yes
6	8	1.6	19	0.6	Yes
8	6	1.9	16	0.6	Yes
6	6	1.9	15	0.6	Yes

Table 3: Analytical Summary of LCC HVDC System Responses to stepped a decrease in the rectifier ac system's voltage

A sample of the LCC HVDC system response to a stepped decrease in the rectifier ac system's voltage is illustrated in Figure 18, for the rectifier ac system ESCR=8 and the inverter ac system ESCR=6. The detailed summary of the LCC HVDC system responses to a stepped decrease in the rectifier ac system's voltage for varying ac system conditions is illustrated in Table 3. Analysis of LCC HVDC system responses reveals that the designed LCC HVDC control system ensures that LCC HVDC system operates stably for varying ac system conditions.

6.2. *Step decrease in inverter ac system voltage*

The LCC HVDC system responses to a 5% stepped decrease in the inverter ac system voltage, for varying ac system operating conditions were evaluated. The LCC HVDC system was simulated the following scenarios in PSCAD/EMTDC:

- The rectifier's ESCR was varied from 8 to 6
- The inverter's ESCR was varied from 8 to 6
- The rectifier's current controller's parameters were set according to equation (3)
- The inverter's current controller's parameters were set according to equation (5)
- After the LCC HVDC system is run to steady state, at $t_1 = 10ms$, the inverter's ac system voltage is decreased by 5%.
- At $t_2 = 0.3\text{sec}$, the current order is decreased by 5%.

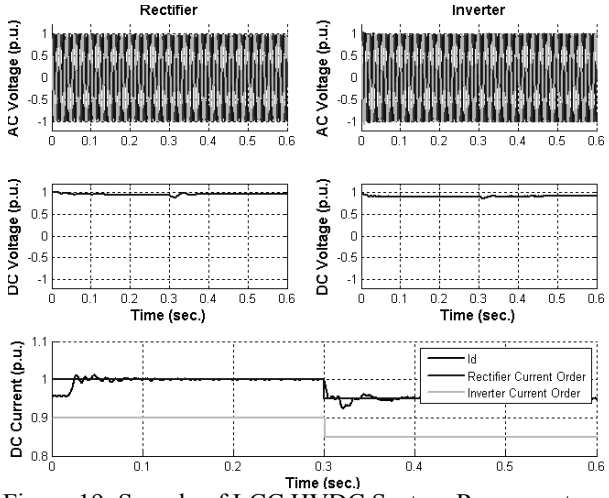

Figure 19: Sample of LCC HVDC System Response to a stepped decrease in the inverter ac system's voltage

Constant Current Order					
Rectifier ESCR	Inverter ESCR	Characteristics			
		O.S (%)	t_s (msec)	Error (%)	Stable
8	8	2.7	27	0.1	Yes
6	8	1.8	26	0.8	Yes
8	6	1.3	37	0.1	Yes
6	6	1.8	38	0.5	Yes
5% Step Decrease in Current Order					
Rectifier ESCR	Inverter ESCR	Characteristics			
		O.S (%)	t_s (msec)	Error (%)	Stable
8	8	2.7	24	0.1	Yes
6	8	3.6	25	1.7	Yes
8	6	2.7	23	0.1	Yes
6	6	4.0	31	1.5	Yes

Table 4: Analytical Summary of LCC HVDC System Responses to stepped a decrease in the inverter ac system's voltage

A sample of the LCC HVDC system response to a stepped decrease in the inverter ac system's voltage is illustrated in Figure 19, for the rectifier ac system ESCR=8 and the inverter ac system ESCR=6. The detailed summary of the LCC HVDC system responses to a stepped decrease in the inverter ac system's voltage for varying ac system conditions is illustrated in Table 4. Analysis of LCC HVDC system responses reveals that the designed LCC HVDC control system ensures that LCC HVDC system operates stably for varying ac system conditions.

7. SMALL SIGNAL STABILITY ANALYSIS OF LCC HVDC CONTROL SYSTEMS

Small signal stability is defined as the ability of the LCC HVDC system to maintain stability following a small disturbance. The small signal stability behaviour of the designed closed loop LCC HVDC control system was obtained by applying a small step output disturbance using MATLAB Control Systems Toolbox. To valid these results, the designed closed loop LCC HVDC system was simulated in PSCAD/EMTDC. The small signal stability behaviour of the designed closed loop LCC HVDC control system was analysed for the Rectifier in Current Control and the Inverter in Voltage Control. The control system illustrated in Figure 20, determines the small signal behaviour of the dc current. The parameters for the rectifier current control plant transfer function were obtained from Table 1 of reference [12]. The solution for the roots of the closed loop system is illustrated in Table 5, which indicates that all the closed loop poles reside in the left hand s-plane, thereby illustrating the unconditional stability of the LCC HVDC system. The lightly damped complex conjugate pole pair at -21.4±273i indicates the response will contain approximately a 43Hz oscillation.

The small signal stability behaviour of the designed rectifier current control loop (Figure 20) was obtained by applying a small (1%) step output disturbance at t = 2.0 seconds using MATLAB Control Systems Toolbox. The same scenario was simulated in PSCAD/EMTDC. The small signal stability behaviour results are illustrated in Figure 21. The results clearly that the MATLAB model results and PSCAD/EMTDC simulation results both concur that the LCC HVDC system is stable which is in agreement with the results and analysis of Table 5.

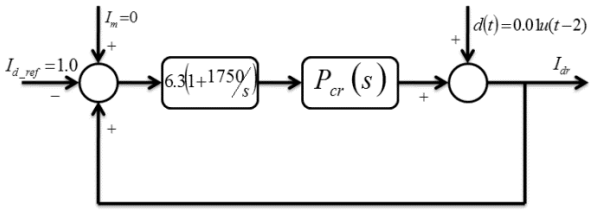

Figure 20: Rectifier Current Control Loop

Eigenvalue	Frequency (Hz)
-20.3	-
-21.40 + 273i	43.45
-21.40 - 273i	43.45
-205	-

Table 5: Eigenvalue Analysis for Rectifier Current Control Closed Loop System

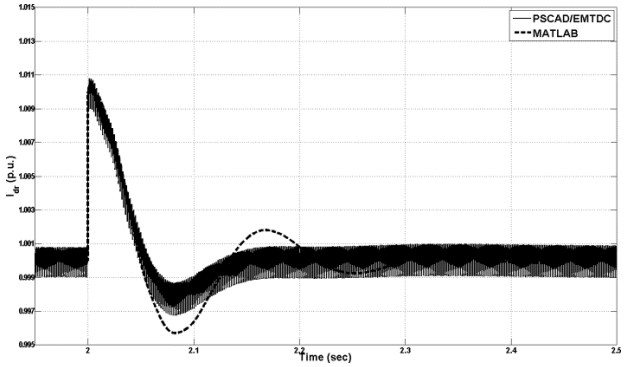

Figure 21: Rectifier DC Current Small Signal Behaviour

The small signal results compare favourably to each other with the approximate 43Hz frequency effect apparent in

both the MATLAB model and the PSCAD/EMTDC simulation.

8. CONCLUSION

A LCC HVDC control system design method based on Quantitative Feedback Theory (QFT) was presented. The QFT design method was used to design the rectifier and inverter current controllers for the LCC HVDC system whose parameters are defined by Table 1 and Table 2 of reference [12]. The designed current controllers individually achieved the specified performance specifications. The stability of the integrated LCC HVDC control system was verified by simulating the start-up of a LCC HVDC system with the rectifier ac system's ESCR=8 and the inverter ac system's ESCR=8. The results revealed that the designed LCC HVDC control system does ensure a stable start-up process, thus preliminarily validating the design method. Due to the uncertain nature of the state of power systems, the conditions defining the operating point of the LCC HVDC system vary. The ability of the designed LCC HVDC control system to remain stable during these operating condition variations is categorized as the "Transient Stability of the LCC HVDC System". The stability of the integrated LCC HVDC control system was verified by simulating the start-up and step responses of the LCC HVDC system with the rectifier ac system's ESCR varying from 8 to 6 and the inverter ac system's ESCR varying from 8 to 6. The stable start-up and step responses of the LCC HVDC system, for varying ac system conditions, conclusively validate the QFT design method of the LCC HVDC control system parameters.

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