GaN HEMT Power Amplifier Design for 2.45 GHz Wireless Applications

Paula Akossiwa Atchike, Jamal Zbitou, Ahmed El Oualkadi, and Pascal Dherbécourt

***Abstract*—Electronic devices with high performances like Power Amplifiers (PA) are very important for Wireless communications. This paper proposes a design of a class AB power amplifier operating at 2.45 GHz, in the S-band frequency. The Cree's CG2H40045F GaN HEMT (High Electron Mobility Transistor) is used for this design. The Gallium Nitride (GaN) technology has been chosen in light of its advantageous properties such as high breakdown voltage, high band gap, as well as high thermal conditions. The paper investigates the different design trade-offs for finding a good balance between various key parameters of the PA (linearity, efficiency, and gain). A design approach has been proposed and the microstrip lines based on the Smith Chart tool available in ADS software have been used for the matching process. The class AB was selected to reach a good agreement between linearity and efficiency, provided by this class. After various process applications from DC characterization to simulations, the proposed design achieves a power added efficiency more than 50% at power saturation with a gain of 15 dB in schematic simulation. The layout dimensions are 55.5 x 64.45 mm^2 on PCB technology.**

***Index Terms*— Class AB, efficiency, gain, GaN, High Frequency, matching, PA.**

I. Introduction

Wireless communications evolution involves high-performing Radiofrequency (RF) devices design. Among them, we have Power Amplifiers (PA) that are essential to the transmission chain. PAs boost up signal in the RF transmitter, which is radiated by the antenna and caught by the receiver[1]. Various past works have studied this device's design using different transistor technologies and approach for miscellaneous applications. Several transistor technologies can be used for RF amplifiers, but GaN HEMT technology is a good choice due to its important characteristics which makes it very interesting for RF applications [2-3-4]. Indeed, this technology is characterized as: wide bandgap (3.4 eV) while Silicon bandgap is 1.12 eV; thus GaN tends to be used instead of Silicon[4] to improve power conversion and energy efficiency. A wide energy bandgap allows the device to support high electric fields. Then GaN has a high breakdown voltage (3.3 MV/cm), which involves large drain voltage operation. A high thermal conductivity (1.7 W/cm.K), also characterizes the GaN technology. A high thermal conductivity results in appropriate temperature working. Furthermore, this technology has the ability to make heterojunctions traduced by high electrons mobility (1000 cm^2/V.s). The GaN technology was chosen for these characteristics in spite of several others like CMOS technology used in [3]. It was proposed in [3] a software routine in order to design a PA on class E or F. However, the proposed design uses only lumped elements and shows a decrease in performances like output power. The design of PA with GaN technology can be completed with different approaches. For instance, envelope tracking (which is the power supply adjustment with the aim to overlap it with signal envelope), was used in [4]. This technique enhance the Power Added Efficiency (PAE), and the simulated value is 55% at 2.45 GHz, while the used GaN transistor could give a value of PAE over 65%. Another works on PA design were made with GaN transistor: such as PA design for radar in [5], using harmonic load network at 2.4 GHz; but also PA design using harmonic tuning at 2.45 GHz ISM frequency in [6]. In these works, good performances were reached but reflection coefficients values don't exceed -15 dB in schematic simulations. Besides, the harmonic tuning used by the previous works, there are other methods in PA design like the internal matching impedance method [7] and, the load pull method [8]. In these quoted works, different approaches were used to design a PA but either the efficiency, or the gain, or the power saturation, or the reflection coefficients were not great as intended. In fact, the challenges in designing a PA are finding the appropriate way to define impedances in the circuit, the design of functional matching networks and in the same time, finding the trade-off between PA parameters. This paper investigates on simple process for PA design with a GaN HEMT transistor operating at 2.45 GHz frequency using ADS software. The bilateral approach was applied in this design with microstrip lines for matching issues based on smith chart. The designed PA achieves a good trade-off between the gain, the efficiency, and the linearity even in electromagnetic simulation (EM). A non-linear model of the chosen transistor was used. In this design, the class AB was preferred owing to good balance between class A with a good linearity and class B with a good efficiency from 50 to 78% [9]. The working frequency f = 2.45 GHz was chosen for Wi-Fi technology and 802.11n standards [10-11]. This paper is organized as follows. Section II presents the proposed PA design, including the bias, the matching networks, and the layout. The results are presented in section III, and the conclusion is given in section IV.

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II. Proposed Power Amplifier Design

A. PA structure

The core of the PA is the transistor and in this paper, the CG2H40045F GaN HEMT transistor has been chosen for its frequency band working from 2 to 4 GHz; a band frequency suitable for wireless communications, especially for 2.45 GHz applications [12]. This transistor can produce 14 dB small signal gain at 4 GHz and 18 dB at 2 GHz and is also class AB operational, therefore the expected efficiency will be high (60% according to the datasheet). A power amplifier is a circuit resulting from joined blocks which are the bias and matching networks. As shown in Fig. 1, these blocks are available at both the PA circuit input and output.

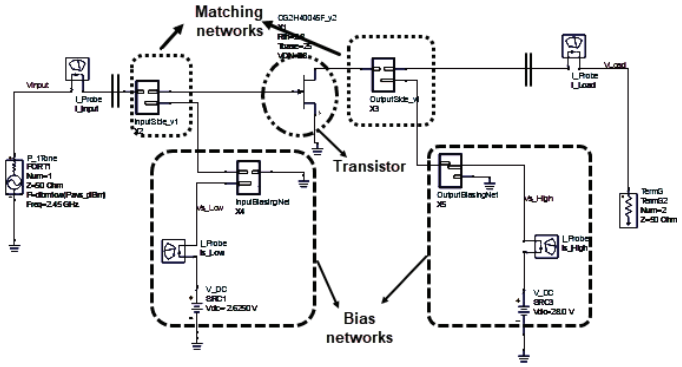

Fig. 1. PA structure

Bias networks are useful to fix an operating point and to decouple RF and DC signals. The matching circuits minimize power reflection to ensure a maximum power transmission. The design of PA is resumed on designing these blocks, for this reason, a design flow is needed.

B. Design flow

To achieve the design of PA, a design flow has been proposed to make different steps clear. The Fig. 2 shows the proposed PA design flow. The first step is a DC characterization of the chosen transistor (CG2H40045F). This initial step is essential for fixing the transistor operating point. Then the stability and the matching issues are considered. A good matching means that S parameter reflection coefficients are low and the performances like output power, gain and efficiency are closed to predicted performances in the transistor datasheet. Since the circuit was built with the represented components available in the used software, a layout conception and a post layout simulations (also called EM co-simulation), are important finalizing steps in a PA design before moving to a practical realization of the circuit.

To achieve all tasks, a professional designing software ADS (Advanced Design System) has been used. This software offers possibility to simulate numerous microwave circuits or complex systems [13]. Thanks to this software multifunction, the opportunity is also given to designer to optimize his results with available methods [14]. This is the ADS optimization that we include in the design flow.

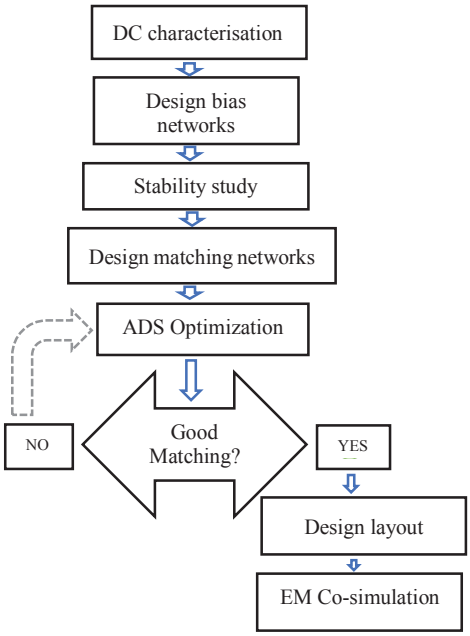

Fig. 2. PA design flow

C. DC characterization

This stage is important in the task of fixing the DC bias quiescent point which depends on the chosen class of the PA. Fig. 3 shows the transistor drain current variations depending on drain voltage for constants gate voltage values. In this case of class AB, we locate this point with load line help [15]. This line results from two points: the first point is located at the limit of the linear zone and the second point at the limit of the saturation zone as shown in Fig. 3.

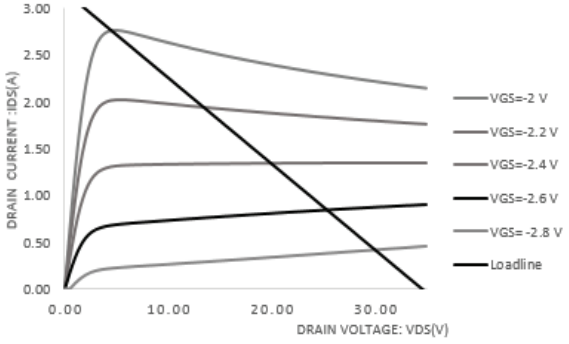

Fig. 3. CG2H40045F DC characteristics

Referring to the transistor datasheet[12], two possibilities for bias point are available for this transistor. The quiescent bias point reserved for our transistor is located in class AB, on load line at VDS0 = 28 V for drain supply; VGS0 = -2.625 V for gate supply and IDS0 = 0.8 A for drain current. To set this point, it is important to build the bias networks.

D. Bias network

As already defined, the bias network is useful to provide DC supply according to the bias point and also to decouple both RF and DC signals. The structure of the proposed bias network is made with a quarter wave line which behaves like an RF choke. By considering a transmission line represented in Fig. 4, the input impedance can be calculated according to the transmission lines theory[16].

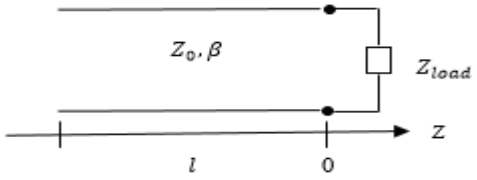

Fig. 4. Transmission line model

The transmission line impedance equation is given by:

$$Z_{in} = Z_0 \frac{Z_{load} + jZ_0 \tan\theta}{Z_0 + jZ_{load} \tan\theta} \quad (1)$$

The electrical length is $\theta = \beta.l$ (2)

For a quarter wave line $l = \frac{\lambda}{4}$: $\theta = \beta.l = \frac{2\pi}{\lambda}\frac{\lambda}{4} = \frac{\pi}{2}$

Where β is the propagation constant, l the line length and λ the wavelength.

Then the equation (1) becomes $Z_{in} = \frac{{Z_0}^2}{Z_{load}}$ (3)

Equation (3) is the expression of the input impedance of a quarter wave transmission line. For a high value of Z_0 this line can similarly behave like an open circuit. Thus to get the RF choke behavior, the chosen bias structure is made with a high impedance quarter wave line (Z_0 = 100 Ω). The RF choke role is to block the RF part around the operating frequency and therefore protect the bias voltage from RF signal [17]. If ever a RF part has managed to pass, it will find a capacitor with a value of 100 pF, which has the role of routing the leaked RF signal to the ground; this is to ensure a perfect decoupling. The final network is shown in Fig. 5.

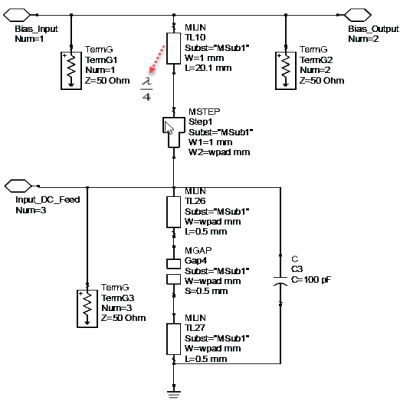

Fig. 5. Bias network structure

As shown in Fig. 6, the values of the S-parameters at f = 2.45 GHz frequency are: S_{21} = -0.004 dB for transmission coefficient (value close to zero) and S_{11} = -50.77 dB, for the reflexion (low value) coefficient, then the isolation is good.

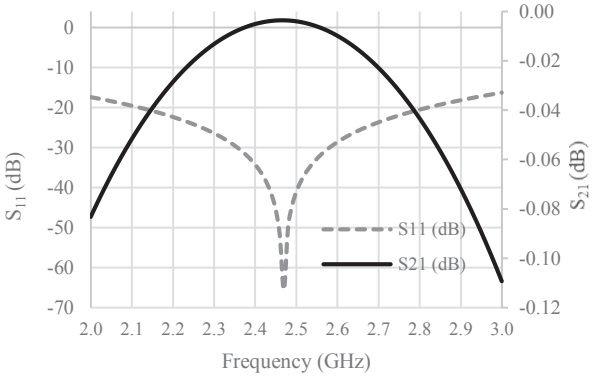

Fig. 6. Simulated bias network S-parameters

E. Small signal stability

The stability notion is very important to remove any oscillation risk and should be carefully checked during the design process. PA is unconditionally stable if Rollet factor K >1 and $|\Delta| < 1$ [1]. These factors are calculated with the S-parameters of the polarized transistor, before the matching process.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}.S_{21}|} \quad (4)$$

Where $\Delta = S_{11}.S_{22} - S_{12}.S_{21}$

The results of the simulated value of these two factors are shown in Fig.7.

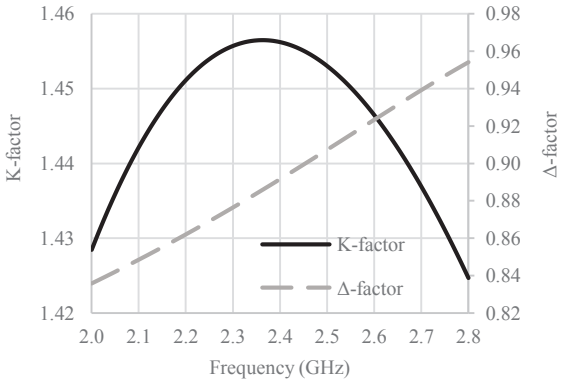

Fig. 7. Stability factors of the biased transistor

At the operating frequency f = 2.45 GHz, K = 1.455 and $|\Delta|$ = 0.899. Since we have K > 1 and $|\Delta| < 1$, then the transistor is unconditionally stable at the operating frequency.

F. Matching networks

In the literature, there are various gain equations defined in the power amplifier design like G_T (transducer power gain),

which is the ratio of power delivered to the load to the power available from the source. There is also G_p (operating power gain) which is the ratio of power dissipated in the load to the power at the network input, and G_a (available power gain) which is the ratio of the power available from the network to the power available from the source. [18]

The transistor's unconditional stability allows for a bilateral approach to be used in PA design, by considering that the transmission coefficient from device input to output called S_{12} parameter, was not neglected $S_{12} \neq 0$ [18]. This approach means that when the input and output of circuit are both matched, the gain is maximized. Then the three defined gains are equal to:

$G_{T,max} = G_{p,max} = G_{a,max} = G_{max}$[18].

Where G_{max} can be calculated by:

$$G_{max} = \frac{|S_{21}|}{|S_{12}|}\left(K - \sqrt{K^2 - 1}\right) \quad (5)$$

By considering the transistor S-parameters and stability simulations results at f = 2.45 GHz frequency:

$S_{21} = 2.496\angle 12.767°$; $S_{12} = 0.021\angle -3.551°$ and K = 1.455

The calculated value of G_{max} is 16.75 dB. This is an indicator to check the gain performance of the PA.

When bilateral approach is used in the matching process, this involves simultaneous matching networks at both the input and output of the circuit. Then, impedances definition in the circuit are necessary. In order to maximize the gain of the PA, the G_a gain can be used in the impedance searching in the circuit. Actually, for a given value of G_a, a constant available power gain circle is plotted with integrated G_a circle tracer in ADS. G_a expression is given by:

$$G_a = \frac{1 - |\Gamma_S|^2}{|1 - S_{11}\Gamma_S|^2} |S_{21}|^2 \frac{1}{1 - |\Gamma_{out}|^2} \quad (6)$$

Where Γ_S is the reflection coefficient at the source of the circuit and Γ_{out}, is the reflection coefficient at output of transistor. In this study, we want to reach a gain value of 16 dB, according to G_{max} value. Then the circle of G_a = 16 dB is plotted and it is known that all Γ_S on this circle produce the given G_a [1]; then, the source impedance can be defined.

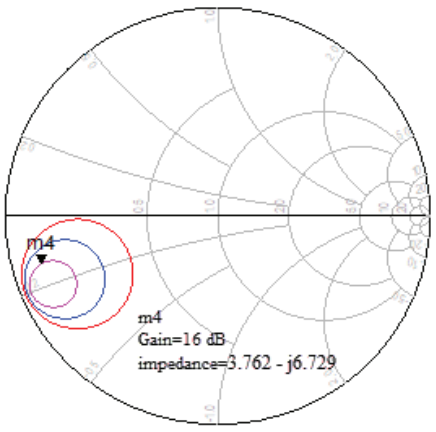

Fig. 8. G_a constant gain circles.

So according to Fig. 8, we get our input impedance Z_S =3.762 - j6.729.

For the output impedance we simply use the value derived by the load reflection coefficient. By plotting S parameters, the corresponding value at output is Z_L = 9.325 + j5.557.

There are several matching methods [14] and in this case we use bilateral approach with transmission lines impedance transforming abilities [14].

Then, with these found impedance values, we design both the Input Matching Network (IMN) and Output Matching Network (OMN) by using Smith chart. We incorporate capacitances which act like DC blocks as we already mentioned. The DC blocks were directly integrated during the matching design to avoid disturbing the process. In the previous section, it has been already mentioned that, the best place for the block capacitance is just after the RF signal generator at the input and just before the load at the output. This is to protect the RF signal generator at the input and the output against the DC signal from the transistor bias source [18]. Matching networks are also made with open shunt stubs and series stubs. The designed IMN and OMN by using Smith Chart are shown in Fig. 9 and Fig. 10 respectively.

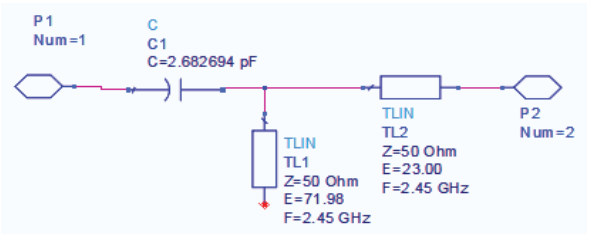

Fig. 9. Designed IMN with Smith Chart tool.

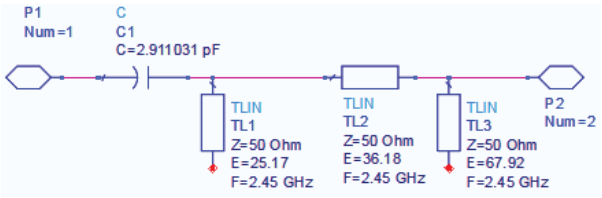

Fig. 10. Designed OMN with Smith Chart tool.

After using Smith Chart tool for matching networks design, the result is ideal transmission lines characterized by electrical length θ and characteristic impedance Z_0. Then, linecalc tool is used to convert the ideal lines into microstrip lines. This tool use the electrical characteristics of the ideal transmission line known as the electrical length θ and characteristic impedance Z_0 to make the conversion to physical characteristics of the microstrip line which are the width *w* and the length *l*.

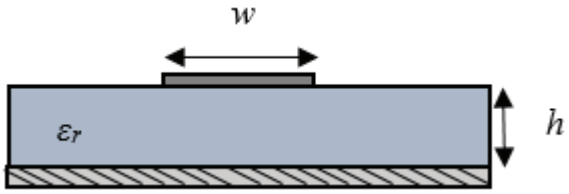

Fig. 11. Microstrip line front view.

For a given Z_0 and a dielectric constant ε_r, the ratio $\frac{w}{h}$ is:

For $\frac{w}{h} < 2$

$$\frac{w}{h} = \frac{8e^{A}}{e^{2A} - 2} \quad (7)$$ Where

$$A = \frac{Z_0}{60}\sqrt{\frac{\varepsilon_r + 1}{2}} + \frac{\varepsilon_r - 1}{\varepsilon_r + 1}\left(0.23 + \frac{0.11}{\varepsilon_r}\right) \quad (8)$$

For $\frac{w}{h} > 2$

$$\frac{w}{h} = \frac{2}{\pi}\left[B - 1 - \ln\left(2B - 1\right) + \frac{\varepsilon_r - 1}{2\varepsilon_r}\left(\ln\left(B - 1\right) + 0.39 - \frac{0.61}{\varepsilon_r}\right)\right] \quad (9)$$

Where $B = \frac{377\pi}{2Z_0\sqrt{\varepsilon_r}}$ (10)

As long as the height of substrate h is given, the value of the microstrip line width *w* can be calculated with the previous expressions[19].

The second physical characteristic of the microstrip line is the length *l*, which can be calculated by:

$$l = \frac{\theta}{\beta} = \frac{\theta \cdot c}{2\pi f\sqrt{\varepsilon_e}} \quad (11)$$

$$\varepsilon_e = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\frac{1}{\sqrt{1 + 12h/w}} \quad (12)$$

Where, θ is the electrical length, c is the velocity of light in a vacuum, f the frequency and ε_e is the effective dielectric constant which can be considered as the dielectric constant of a homogeneous medium that equivalently takes the place of air and dielectric regions of the microstrip line.

The ''linecalc'' tool available on ADS gives the correspondent microstrip line characteristics like width and length. The used substrate is RT/duroid6002, characterized by the height h = 0.508 mm and $\varepsilon_r = 2.94$ [20].

G. Layout and cosimulation circuit

The proposed PA layout is shown in Fig. 12. The PA is implemented on Rogers RT/duroid 6002 substrate and based on CG2H40045F active device. The layout shows both the input and output matching networks, the biasing networks and both the gate and drain paths all, are designed using microstrip transmission lines. According to datasheet transistor the dimensions of the GaN HEMT transistor are: 6 on 15 mm. The layout sizes are 55.5 mm on 64.45 mm.

The Fig. 13 shows the model generated from the designed layout which can be used for EM co-simulation. It is called co-simulation because in the same schematic, layout electromagnetic model and the others circuit elements that cannot be represented in the layout, like power generators, are all simulated together.

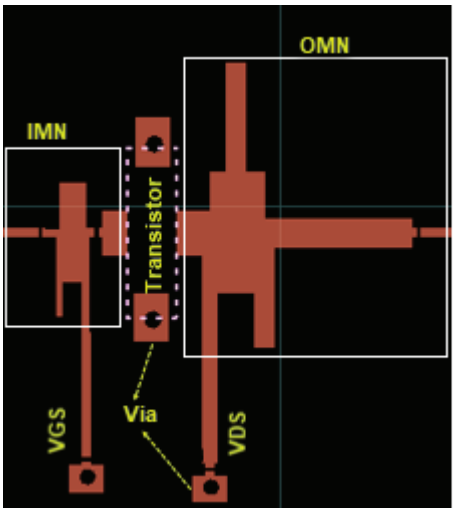

Fig. 12. Designed PA Layout

This kind of simulation is indeed important for considering electromagnetic phenomena occurring in the circuit [21], especially in microstrip lines use.

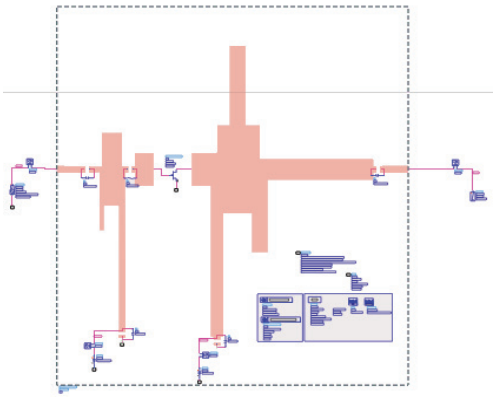

Fig. 13. Post-layout test.

III. Simulation Results

The performances of the simulated PA are presented in this section. First, the stability factors simulations are very important for checking the designed PA stability.

The performances are evaluated in terms of output power, gain, and efficiency. Before moving forward, the checking of S-parameters is also important.

As shown in Fig. 14 the Rollet factor at the operating frequency f = 2.45 GHz is: K = 1.435 and |Δ| = 0.835. K > 1 and |Δ| < 1, then we conclude that the designed PA is stable at the operating frequency; oscillations risks are removed.

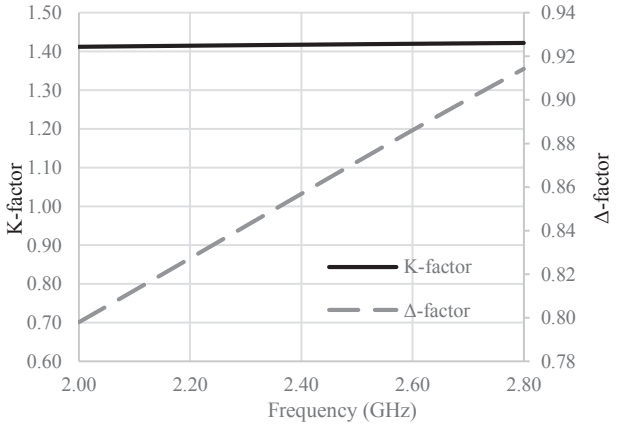

Fig. 14. Designed PA stability factors

The obtained PA at the end of a design must present the low values of reflection coefficients. In other words S_{11} and S_{22} must be low as possible. This is a sign of good matching. The transmission coefficient S_{21} gives an overview of the gain. The S_{12} factor represents the feedback from the output to the input. This factor must necessary be small for the reason that it is the most representative factor of isolation.

Fig. 15 shows the S-parameters values obtained at f = 2.45 GHz operating frequency. It can be observed that the designed PA shows a good matching since the obtained parameters S_{11} and S_{22}, are equal to -47.799 dB and -46.094 dB in schematic simulation, respectively. Transmission coefficients are also a part of S-parameters: S_{12} and S_{21}, are equal to -24.707 dB and 16.871 dB respectively.

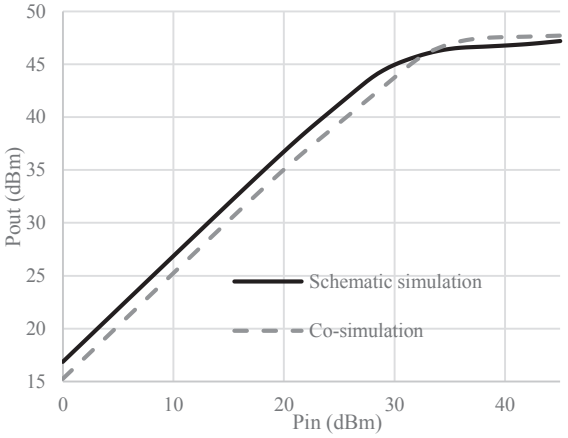

Fig. 16. Output power variation versus input power before and after cosimulation

The variation of the simulated output power versus input power at f = 2.45 GHz frequency, both before and after co-simulation is shown in Fig. 16. These plots show the PA power limitations and the compression point. As observed, the compression point is at P_{1dBm} = 27 dBm and the power saturation is P_{outmax} = 46.9 dBm for schematic simulation. However, for EM simulation, the compression point at the input power is P1dBm = 28 dBm and the power saturation is P_{outmax} = 47.5 dBm for EM simulation. The maximum value of output power extracted from the datasheet is 46.5 dBm.

The compression point P_{1dBm} is the point at which the output power value is 1dB lower than the power value in the ideal linear response.

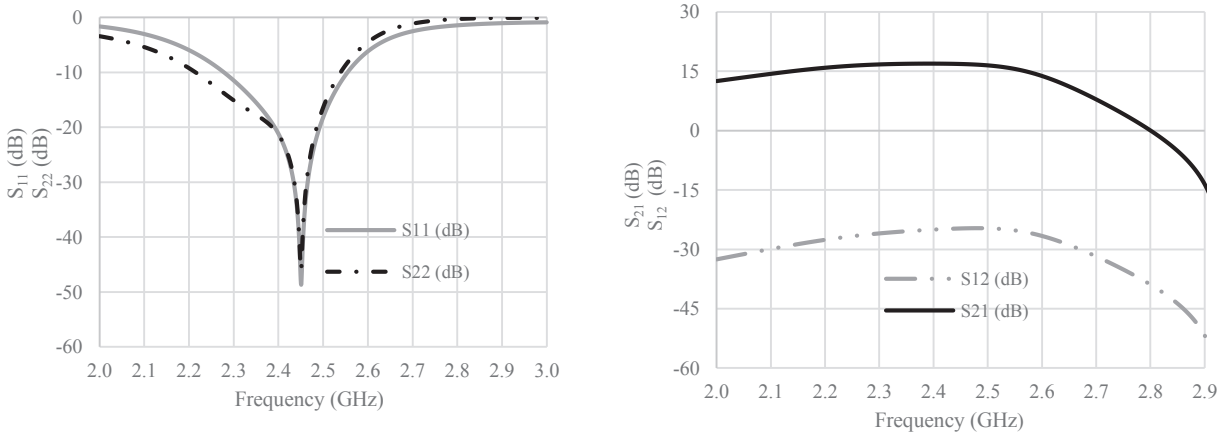

Fig. 15. Simulated S-parameters: (a) S_{11} and S_{22}, (b) S_{12} and S_{21}

The most important PA performance is the power gain which is the ratio between output power and input power [18]. The Fig. 17 shows the variation of the simulated gain versus input power at 2.45 GHz frequency before and after co-simulation. At the compression power, the gain is equal to 15.85 dB for schematic simulation. However, after EM co-simulation, the gain is equal to 14.018 dB. Knowing that this transistor can produce a gain from 14 dB to 18 dB[12], and the expected value is G_{max} = 16.75 dB; the obtained result is still acceptable.

$$Gain(dB) = P_{out}(dBm) - P_{in}(dBm) \quad (13)$$

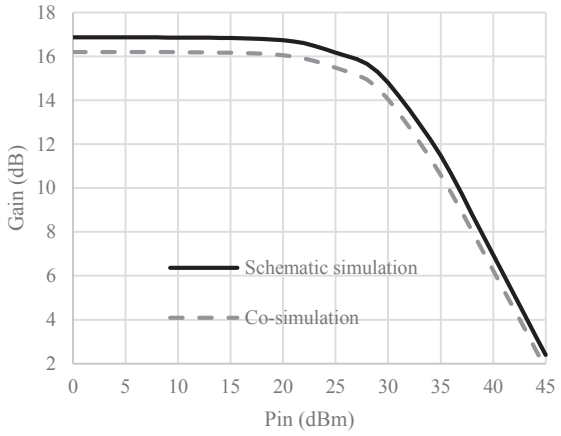

Fig. 17. Gain before and after cosimulation

The Power-Added Efficiency (PAE) is a metric for rating the efficiency of a power amplifier. This efficiency takes account the effects of the input power. The input power, output power and the DC power are used to as given in equation (14):

$$PAE = 100 * \frac{P_{out} - P_{in}}{P_{DC}} \quad (14)$$

The obtained PAE value is 65.9% at power saturation before co-simulation and equals 59.2% after, according to Fig. 18. In the transistor datasheet [12], 60% of efficiency value is expected.

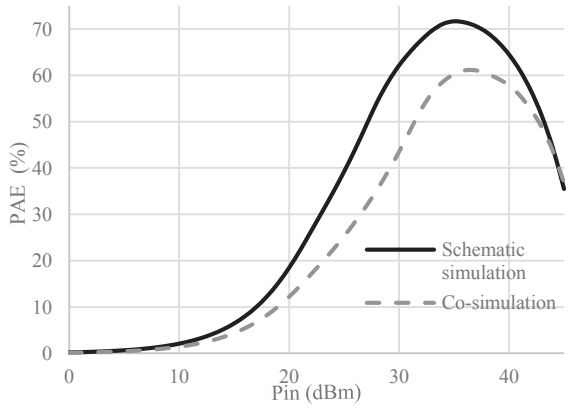

Fig. 18. PAE efficiency

Table I summarized the obtained results of the proposed design compared to similar works in the state-of-the-art. By comparing the obtained results of this work to others in the literature, the proposed GaN HEMT PA exhibits a good output power with a good PAE, a high gain and an excellent impedance matching with a simple approach. These reasons make the designed PA suitable for wireless communication applications operating at 2.45 GHz frequency.

TABLE I

COMPARISON OF THE DESIGNED POWER AMPLIFIER AND OTHERS OF THE STATE-OF-ART

	[5]GaN _2017	[22]GaN_ 2017	[23]GaAs _2020	[24]GaN_ 2022	This work
F(GHz)	2.4	2.45	2 to 3	2.4 to 3	2.45
Gain (dB)	20.727	~9	13.9	13.4<	15.85
$P_{out\ max}$ (dBm)	41.818	~ 39	16.4	>40	46.9
PAE	78.8 %	~46%	25.3%	51%>	65.9%
S_{11} (dB)	-14.017	~ -20	<-10.6	<-10	-47.79
VDS (V)	28	28	2.8	28	28

IV. CONCLUSION

A power amplifier designed at 2.45 GHz with CG2H40045F GaN HEMT transistor in class AB is proposed in this paper. This technology is suitable for high frequency applications and power amplifier performance. To achieve the goal, this conception starts with DC characterization, followed by stability considerations and then matching issues. For matching, the bilateral approach is used, Smith Chart implemented in ADS has been used and we end up with microstrip matching networks. After post layout tests of the achieved PA, we noticed P_{outmax} equals to 46.9 dBm; a gain equals to 15.85 dB and more than 50% PAE efficiency. These results make this design suitable for wifi application. The next step will be to carry out a real prototype of this amplifier.

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