Wafer-Level Vacuum Sealing by Transfer Bonding of Silicon Caps for Small Footprint and Ultra-Thin MEMS Packages

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***Abstract*— Vacuum and hermetic packaging is a critical requirement for optimal performance of many micro-electro-mechanical systems (MEMS), vacuum electronics, and quantum devices. However, existing packaging solutions are either elaborate to implement or rely on bulky caps and footprint-consuming seals. Here, we address this problem by demonstrating a wafer-level vacuum packaging method featuring transfer bonding of 25-μm-thin silicon (Si) caps that are transferred from a 100-mm-diameter silicon-on-insulator (SOI) wafer to a cavity wafer to seal the cavities by gold–aluminum (Au–Al) thermo-compression bonding at a low temperature of 250 °C. The resulting wafer-scale sealing yields after wafer dicing are 98% and 100% with sealing rings as narrow as 6 and 9 μm, respectively. Despite the small sealing footprint, the Si caps with 9-μm-wide sealing rings demonstrate a high mean shear strength of 127 MPa. The vacuum levels in the getter-free sealed cavities are measured by residual gas analysis to be as low as 1.3 mbar, based on which a leak rate smaller than 2.8×10^{-14} mbarL/s is derived. We also show that the thickness of the Si caps can be reduced to 6 μm by post-transfer etching while still maintaining excellent hermeticity. The demonstrated ultra-thin packages can potentially be placed in between the solder bumps in flip–chip interfaces, thereby avoiding the need of through-cap-vias in conventional MEMS packages. [2018-0257]**

***Index Terms*— Vacuum, hermetic, packaging, sealing, MEMS, ultra-thin package, small footprint, transfer bonding, 3D integration, flip chip, aluminum, gold, thermo-compression bonding.**

I. Introduction

VACUUM packaging is a process for encapsulating a device (e.g. a MEMS or nano-electro-mechanical system (NEMS) device) in a vacuum environment and maintaining the internal vacuum level using hermetic seals. It enables functionality and long-term reliability of various MEMS devices, such as inertial sensors, pressure sensors and infrared detectors, but typically also constitutes a significant part of their cost in high-volume production [1], [2]. As a general trend, wafer-scale manufacturability, very high sealing yields, and reduced sealing footprints are required in vacuum packaging for cost reduction and further system miniaturization [3]. At the same time, lower packaging temperatures, sufficient thermal stability and long-term hermeticity of the seals, as well as reduced device thicknesses after capping are pursued for important application areas such as portable devices, and for improving compatibility with other 3D system integration processes such as flip chip bonding [4]–[6]. The use of thin caps for hermetic packaging has drawn particular attention, since it offers many advantages over thick caps [7]–[9]. Thin caps result in low package and device thicknesses, and by combining thin caps with small sealing footprints [8], [9], significant device miniaturization and cost reduction can be achieved. Furthermore, a thin cap (< 50 μm) made of optically transparent materials, such as silicon dioxide, silicon nitride, or silicon (for infrared light), is very useful for low-loss transmission of light signals and optical interfacing, e.g. in micro-opto-electro-mechanical systems (MOEMS) [8]–[11]. Another very important merit of a thin cap is that if the cap height is smaller than the solder or stud bumps in a flip chip bonding process, it allows direct vertical stacking of the encapsulated substrates without relying on through silicon vias (TSVs) or through glass vias (TGVs) in the cap, thus facilitating high-density 3D system-on-chip (SoC) integration of multiple modules [6], as illustrated in Fig. 1.

To realize wafer-level encapsulation with thin caps, two main types of packaging approaches have been developed: vacuum packaging by thin film deposition and wafer bonding of caps. Thin film deposition typically uses a sacrificial layer to cover the structures to be sealed, followed by a cap film deposition. The sacrificial layer is subsequently removed by etching through access holes or by thermal decomposition. Finally, a sealing film is conformally deposited over the cap film to seal the access holes [7], [12]–[20]. The total thickness of the capping film stack is usually only a few micrometers, which offers very low profile as well as small footprint seal in the lateral dimension. However, there are several drawbacks associated with this approach [21]. First, the packaging process is complex, especially if MEMS or NEMS movable structures must also be released, since in this case multiple sacrificial layers have to be incorporated. Second, because all the processes must be compatible with the specific device structures

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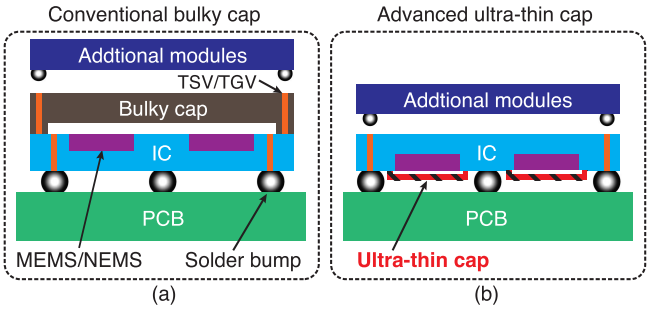

Fig. 1. Illustration of two different 3D heterogeneous integration schemes. (a) System-on-chip (SoC) integration with a conventional bulky cap sealing the integrated circuit (IC) and MEMS/NEMS chip. Through silicon vias (TSVs) or through glass vias (TGVs) in the cap are used to connect to additional modules. (b) SoC integration featuring higher component density using ultra-thin caps locally encapsulating the MEMS/NEMS parts. No TSVs and TGVs are needed in the thin caps.

and materials, this approach suffers from lack of flexibility and universality. Third, in the case of sacrificial and sealing films made of silicon oxide, silicon nitride, or poly-silicon, the deposition processes typically involve high temperatures, which may hinder its use for many applications, e.g. sealing of MEMS on ICs. In contrast, hermetic sealing of devices by bonding caps on top of the devices is a more versatile approach. Since the preparation of the caps is separated from the preparation of the devices to be sealed, and because various material systems for the bonding and sealing process can be employed, this approach overcomes the abovementioned drawbacks of sealing by thin film deposition.

A variety of methods are available for sealing of devices with thin caps by bonding. One such method is transfer bonding, where pre-defined thin caps on a carrier wafer are transferred to the device wafer by wafer bonding and subsequently the carrier wafer is removed [21]–[29]. Transfer bonding of pre-defined caps has the advantage of precise control of the cap thickness, which is promising to realize uniform and ultra-thin caps on wafer-scale. Different cap materials have been investigated for sealing by transfer bonding, including polymers [23]–[27], silicon [22], [28], silicon nitride [29], glass [28], and metals [21], [30], [31]. Polymers are permeable to gases and moisture, and are not suitable for vacuum or hermetic packaging [32], [33], neither as cap materials [23]–[27], nor as bonding and sealing materials [21], [28], [29], [34]. Metals are superior candidates for sealing because they provide excellent hermeticity and mechanical strength, meaning that metal sealing rings as narrow as tens of micrometers could be sufficient for hermetic and vacuum packaging [35]. Efforts have been made to realize hermetic sealing using transferred thin caps in combination with metal-based seals. Au-Si eutectic bonding was investigated for vacuum packaging using deposited poly-Si microcaps. However, the packages exhibited significant internal pressure increase after 50 days of storage [22]. 5 μm-thick electroplated Ni caps were transferred from a carrier wafer to a device wafer using Ni-Sn transient liquid phase (TLP) bonding, however the resulting packages were not hermetically sealed [9], [31]. A transfer bonding approach for selective transfer of specific dies from the carrier wafer to the target wafer by laser debonding has been reported [36]. This approach is based on Au-Au bonded seals and temporary polymer bonding of dies on the carrier wafer. In [36], the dies on the carrier wafer functioned as caps to be transferred to the target substrate. However, no thin caps were realized, and the sealing rings were as wide as 90 μm.

Another wafer bonding-based approach for sealing of devices with thin caps is realized by Au-Au thermo-compression bonding or Au-Sn eutectic bonding of a silicon cap wafer to a device wafer and subsequent thinning of the Si cap wafer by grinding [37]–[40]. Although being an extremely successful packaging approach that is widely used in industry, e.g. for packaging of film bulk acoustic resonator (FBAR) filters [37], [38], this approach poses potential challenges in realizing uniform ultra-thin cap thickness (e.g. $\sim$5μm) on wafer-scale without impairing the structural integrity and hermeticity of the seals during the grinding process. The reported Si caps realized with this approach were relatively thick, ranging from 60 μm to 80 μm [37]–[40]. Besides, either wide metal sealing rings of 75–100 μm were used [39], [40], or no details of the package design, sealing process, and resulting long-term hermeticity are described in the literature reports [37], [38].

In summary, to the best of our knowledge, there have been no reports where transferred thin caps ($<$ 30 μm) in combination with small sealing footprints ($<$ 10 μm) provided reliable vacuum sealing of cavities. Here, we present a novel wafer-level packaging process that realizes vacuum sealing of cavities using 25 μm-thick Si caps transferred from an SOI wafer. We used the Si device layer of an SOI wafer in our work because of the precise control of the thin Si device layer for the pre-defined caps, the excellent mechanical strength and low residual stress of single-crystalline Si, and the minimal thermal mismatch between the Si caps and typical MEMS device wafers. Compared to the abovementioned post-thinning technique by grinding of the bonded Si caps, our approach avoids potential mechanically-induced damage of the caps and sealing rings, if ultra-thin caps are to be achieved. The vacuum sealing is provided by Au-Al thermo-compression bonding at a low temperature of 250 °C, thus being compatible with standard IC processes. The use of thin single crystalline Si caps in combination with narrow metal sealing rings ($<$ 10 μm) aims to provide a reliable and space-efficient solution for fully hermetic packaging of MEMS and NEMS, and potentially for high-density 3D integration with ICs. Furthermore, the hermeticity of the sealed cavities and the strength of the bonds are evaluated. Finally, the influence of sealing ring width on the resulting sealing yield and the possibility of encapsulating cavities of various dimensions using the thin Si caps are investigated.

II. Design and Fabrication

A. Concept of Transfer Bonding of Thin Caps

The concept of our sealing approach by transfer bonding of thin caps is illustrated in Fig. 2. The thin Si caps are prepared on the device layer of an SOI cap wafer. Protruding Si sealing rings are formed along the perimeters of the caps and covered by a layer of Au. The cap wafer is then

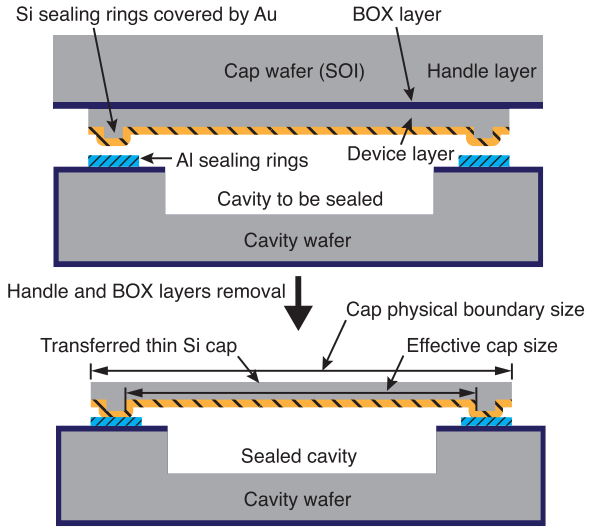

Fig. 2. Schematic cross-sectional drawing of the hermetic packaging concept by transfer bonding of thin Si caps.

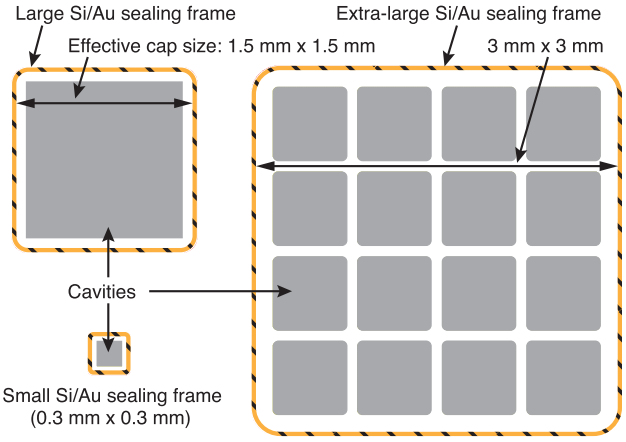

Fig. 3. Three different sealing ring frames with cavities of different dimensions (Si caps are hidden for better illustration).

TABLE I
DIMENSIONS OF KEY DESIGN PARAMETERS AND VARIATIONS

Thickness of thin Si caps	25 μm
Widths of Si/Au sealing rings	3 – 27 μm (3 μm interval, 9 variations)
Thickness of Si/Au sealing rings	5 μm (Si) + 1.8 μm (Au)
Side lengths of the effective square Si caps	0.3 mm / 1.5 mm / 3 mm
Side lengths of the physical boundaries of the Si caps	0.39 mm / 1.6 mm / 3.1 mm
Radii of rounded Si/Au sealing frame corners	20 μm / 100 μm / 200 μm
Thickness of Al sealing rings	650 nm
Widths of Al sealing rings	30 μm wider than Si/Au sealing rings
Number of large / extra-large / small Si caps	432 / 32 / 144

aligned and bonded to the cavity wafer with corresponding Al sealing rings, thus sealing the enclosed cavities. The handle layer and buried oxide (BOX) layer of the cap wafer are removed after the bonding, thus achieving transfer of the thin Si caps. The narrow protruding Si/Au rings are designed to introduce high local pressure at the Au-Al bonding interfaces, which not only results in a small sealing footprint, but also induces plastic deformation of Au and Al. Thus, the Au and Al are partially extruded sideways, which potentially helps breaking the surface oxide formed on the Al sealing rings. Consequently, close and uniform contact between Al and Au layers is formed, which facilitates the subsequent solid-state inter-atomic diffusion processes and bond formation [41]. In addition, the induced plastic deformation makes the bonding and sealing process insensitive to the surface roughness of the Au and Al sealing rings.

The benefit of using Al on the cavity wafer is that Al is a standard bond pad material on MEMS dies and on complementary metal-oxide-semiconductor (CMOS) wafers. Thus, the Al sealing rings can be patterned together with the bond pads in the same process, which introduces minimal changes to the standard processing flow for producing the device wafer. To assist the bonding between the Si caps and the Al sealing rings, soft metals such as Al, Au, and Ag are potential candidates for covering the Si sealing rings on the cap wafer. The bonding temperature for Al-Al thermo-compression bonding is typically as high as 400–450 °C [42], [43], which potentially makes the device structures prone to thermally induced damages. Ag-Al bonding suffers from contact corrosion, especially under humid conditions [44]. Thus, Au is chosen in this work to realize the low-temperature Au-Al thermo-compression bonding, which has been demonstrated for hermetic packaging at a higher temperature of 300 °C [45]. For the cap material, Si is used to minimize the thermal mismatch between the thin caps and the cavity wafer, thus reducing the risk of crack formation in the seals. The use of an SOI cap wafer is to precisely and reliably define the thickness of the Si caps. The relatively high stiffness of single crystalline Si also provides mechanical stability for the thin caps, especially when the thin caps deflect due to pressure difference between the sealed vacuum cavities and the ambient atmosphere.

To investigate the influence of the Si/Au sealing ring width on the resulting sealing yield, nine different sealing ring widths from 3 μm to 27 μm were incorporated on the same cap wafer. Cavities of three different dimensions were also included in the same cavity wafer to study the possibility of applying the proposed packaging method to different cavity sizes, as shown in Fig. 3. The dimension of the large sealing frame of 1.5 mm $\times$ 1.5 mm was designed in the way that the deflections of the thin Si caps due to pressure difference would be smaller than the thickness of the Si/Au sealing rings, thus avoiding any protrusion into the cavities. Extra-large cap designs were included for covering multiple cavities. This is useful for reducing the overall sealing footprint when capping several devices in a single package. In this case, the separation walls between the cavities serve as additional supports that can reduce the deflections of large caps into the cavities. The key design parameters and design variations of the sealing structures are summarized in Table I.

B. Fabrication

The process flow of the proposed wafer-level vacuum packaging method by transfer bonding of thin Si caps is shown

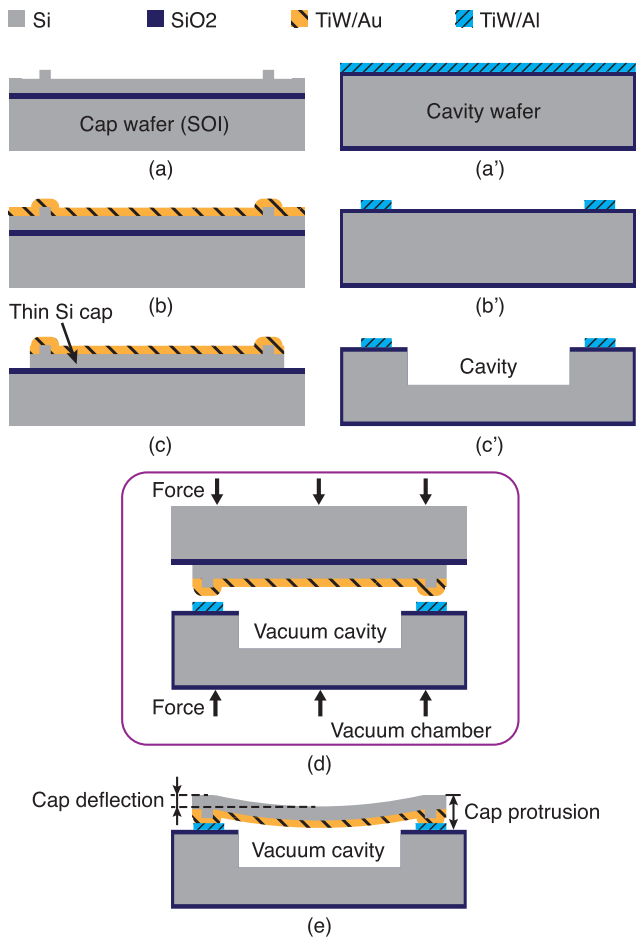

Fig. 4. Process flow of the vacuum packaging method by transfer bonding of thin Si caps. (a) Patterning of Si sealing rings by DRIE on the cap wafer. (b) TiW/Au deposition on cap wafer. (c) Selective Au etching and Si DRIE to define the thin Si caps. (a') Thermal oxidation and TiW/Al coating of the cavity wafer. (b') Patterning of Al sealing rings by selective Al etching. (c') Selective DRIE of SiO_2 and Si to form cavities. (d) Wafer alignment and bonding of the wafers inside a vacuum chamber at 250 °C, thereby achieving sealing of the cavities. (e) Removal of the handle and BOX layers of the cap wafer by RIE, leaving the thin Si caps on the cavity wafer. The thin caps defect if there is a pressure difference between the inside of the cavity and outside atmosphere.

in Fig. 4. A 100 mm-diameter SOI wafer with a 30 μm-thick Si device layer, a 500 nm-thick BOX layer, and a 400 μm-thick handle layer was used as the cap wafer. The 5 μm-high Si sealing rings were firstly formed by photolithography and Si deep reactive ion etching (DRIE) on the device layer of the SOI cap wafer (Fig. 4a). Then, a 100 nm-thick TiW adhesion layer and a 1.8 μm-thick Au bonding layer were sputtered on the Si sealing rings after oxygen plasma cleaning of the cap wafer (Fig. 4b). Thereafter, the Au and TiW layers were selectively etched (using a photoresist mask) in solutions using I_2/KI and $NH_3{\cdot}H_2O/H_2O_2$ as main etchants, respectively. Finally, the thin Si caps were formed by Si DRIE (Fig. 4c). The Au coating covering the caps potentially helps to enhance the overall hermeticity of the resulting packages. However, if optical transparency of the thin Si caps in the infrared wavelength region is needed, the Au coating inside the Si/Au sealing frames can be selectively removed using an additional mask.

For the cavity wafer, a single-side polished 500 μm-thick and 100 mm-diameter Si wafer with a 1 μm-thick thermal SiO2 was prepared. First, a 100 nm-thick TiW adhesion layer and a 650 nm-thick Al bonding layer were sputtered on the cavity wafer (Fig. 4a'). Then, the Al sealing rings and TiW layer were patterned sequentially by selective etching (using a photoresist mask) in solutions using $H_3PO_4/HNO_3/CH_3COOH$ and $NH_3{\cdot}H_2O/H_2O_2$ as main etchants, respectively (Fig. 4b'). The Al sealing rings were designed to be 30 μm wider than the corresponding Si/Au sealing rings on the cap wafer in order to have a large tolerance (30 μm) for wafer-to-wafer misalignment during wafer bonding. Thereafter, the cavities were formed by DRIE of SiO_2 and Si to a depth of 100 μm, using another photoresist mask (Fig. 4c'). Finally, the photoresist mask was removed by oxygen plasma etching.

Prior to wafer bonding, the cap wafer was cleaned by deionized water and dried in a spin dryer. No additional cleaning was used for the cavity wafer. The two wafers were then aligned in a pre-bond wafer aligner (*Suss BA8, Suss MicroTec AG, Germany*), clamped together, and transferred to a wafer bonder (*Suss CB8, Suss MicroTec AG, Germany*) (Fig. 4d). The bonder chamber was firstly evacuated to a pressure of 7×10^{-5} mbar, after which the pump was kept running for one additional hour. Then, a bonding force of 25 kN was applied to the wafer stack by the top and bottom wafer chucks in the chamber, with a force ramping rate of 8 kN/min. Thereafter, the wafer stack was heated to a temperature of 250 °C, with a temperature ramping rate of ~20 °C/min. The set temperature and bonding force were then kept constant for 45 min. The applied force of 25 kN corresponds to a local pressure of approximately 400 MPa at the as-patterned Au-Al bonding interfaces, which is four times the yield strength of Au. This pressure level was used to ensure plastic deformation of the Au-Al sealing rings. Finally, the wafer chucks were cooled down to room temperature with a cooling rate of ~5 °C/min, followed by removal of the bonding force and venting of the bonder chamber.

After bonding, the handle layer of the SOI cap wafer was removed by Si RIE, which stopped at the BOX layer. After the Si etching, the BOX layer wrinkled in the areas where there were no Si caps, due to relaxation of internal compressive strain. The wrinkled BOX layer was easily removed by an N_2 gas jet. Next, the remaining BOX layer was removed by SiO_2 RIE, which was controlled by time so that the thermal SiO_2 on the cavity wafer was not etched significantly. Thus, the Si caps were successfully transferred from the cap wafer to the cavity wafer to hermetically seal the vacuum cavities. Alternatively, the BOX layer in between the Si caps could be removed by SiO_2 RIE before the wafer bonding and after the formation of individual caps by Si DRIE (between steps of Fig. 4c and Fig. 4d), which would avoid the formation of a wrinkled BOX layer in the first place. At atmospheric pressure, the thin Si caps deflected due to the pressure difference between outside atmosphere and the sealed vacuum cavities, as depicted in Fig. 4e. This offers a convenient way for monitoring the sealing yield over the wafer and evaluating leak rates of the seals during long-term storage [41], [46].

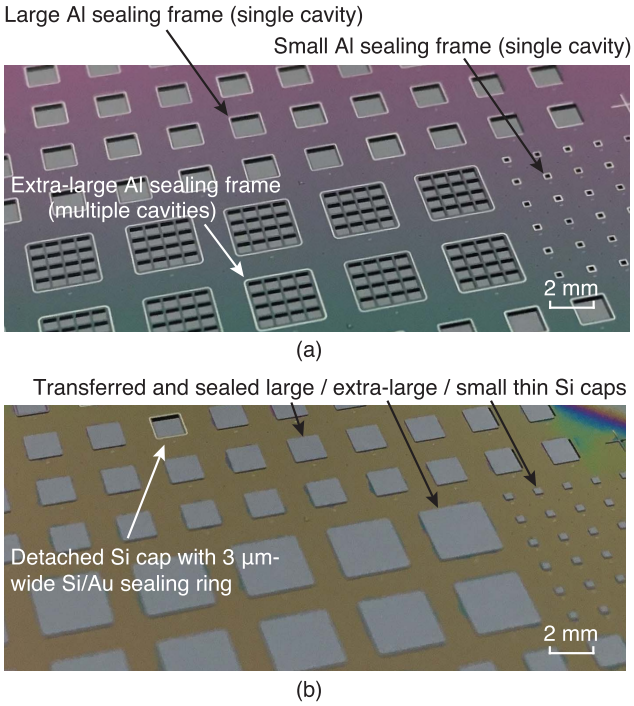

Fig. 5. Optical images of the cavity wafer before and after the transfer of the thin Si caps. (a) Image of a part of the cavity wafer before the thin cap transfer. (b) Image of the same site after the thin cap transfer.

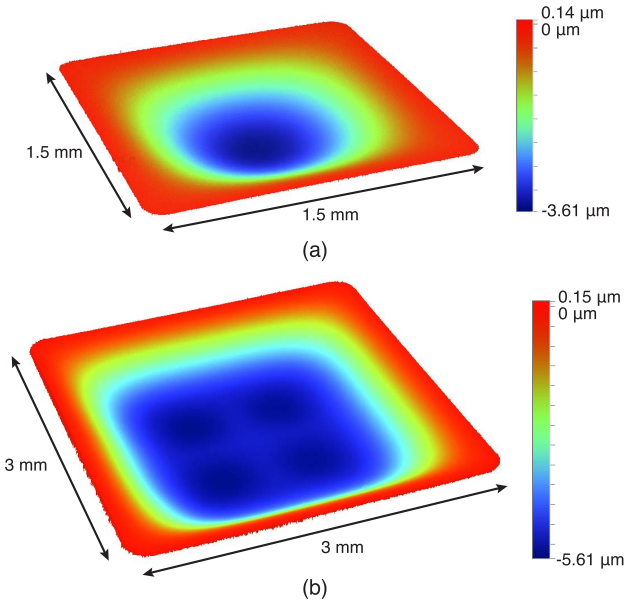

Fig. 6. Measured thin cap deflections by white-light interferometry. (a) A large Si cap (~25 μm thick) with a 15 μm-wide Si/Au sealing ring. (b) An extra-large Si cap (~25 μm thick) with an 18 μm-wide Si/Au sealing ring. The extra-large Si cap landed on the separation walls between the multiple cavities. The zero level refers to the initial top surface of the thin Si caps.

We also tested the above described Au-Al bonding process at room temperature in combination with a higher bonding force of 32 kN, instead of the utilized 250 °C. However, in this case the cap wafer detached from the cavity wafer during the wafer thinning process, indicating that the resulting Au-Al bond was not sufficiently strong. Another Au-Al bonding test was conducted at 250 °C but with a lower bonding force of 16 kN, instead of 25 kN. The bonded wafers survived the wafer thinning process and exhibited a similar high sealing yield, indicating that the above described Au-Al bonding process can be used for sealing with lower bonding forces.

III. Results and Discussion

A. Yield of Thin Cap Transfer and Sealing

After bonding and removal of handle and BOX layers of the SOI cap wafer, all the thin Si caps with different dimensions were successfully transferred to the cavity wafer, except for 5 out of the 432 large Si caps with 3 μm-wide Si/Au sealing rings (Fig. 5). Cavities with intentionally designed leakage also exhibited small deflections of the caps (0.1–0.3 μm), which however were significantly lower than that for the sealed cavities. While this indicates the presence of residual stresses in the caps, the observed stress levels did not cause damage of the seals or the caps. The sealing yields of the large and extra-large Si caps were evaluated by measuring the cap deflections by white-light interferometry (*Wyko NT9300, Veeco Inc., US*), as shown in Fig. 6. The deflections of the large Si caps with sealing ring widths above 3 μm were below 6 μm, which avoids any protrusion into the cavities. The extra-large Si caps deflected and landed on the separation walls between the sealed multiple cavities, with protrusion into the cavities of ~100 nm. For the small Si caps, the theoretical cap deflection is on the order of a few nanometers (calculated according to equation (1) in section III.C), which is below the detection limit of our measurement setup, thus the sealing yield of small cavities cannot be confirmed by this method. The protrusion of the transferred Si caps out of the cavity wafer plane were within 31 ± 1 μm, which is below typical solder and stud bump heights of ~50 μm after flip chip bonding [47]. Thus, our approach is dimensionally compatible with flip chip bonding as illustrated in Fig. 1b.

To evaluate the wafer-scale sealing yield as a function of the Si/Au sealing ring width, all the 432 large Si caps distributed over the whole wafer were evaluated over a period of two months, using 48 samples for each of the nine different sealing ring widths, as shown in Fig. 7. Except for the cavities with 3 μm-wide Si/Au sealing rings, all the cavities showed excellent sealing yields of either 98% (47 out of 48 cavities sealed) or 100%, even when the Si/Au sealing rings as narrow as 6 μm. The lower sealing yield of the 3 μm-wide Si/Au sealing rings is most likely due to insufficient bond strength as a result of the small bonding area. After two months of storage, the cavity wafer with the transferred thin Si caps was diced using a standard dicing saw (*DAD 320, Disco Corp., Japan*). The resulting yield after dicing, also plotted in Fig. 7, exhibited no drop except for one leaked cavity with a 24 μm-wide Si/Au sealing ring. For the multi-cavity designs with four types of Si/Au sealing ring widths of 6–24 μm, the overall sealing yield is 97% (31 out of 32 cavities sealed). These cavities also survived dicing and exhibited no gross leakage, which would be indicated if the cap deflections decreased to

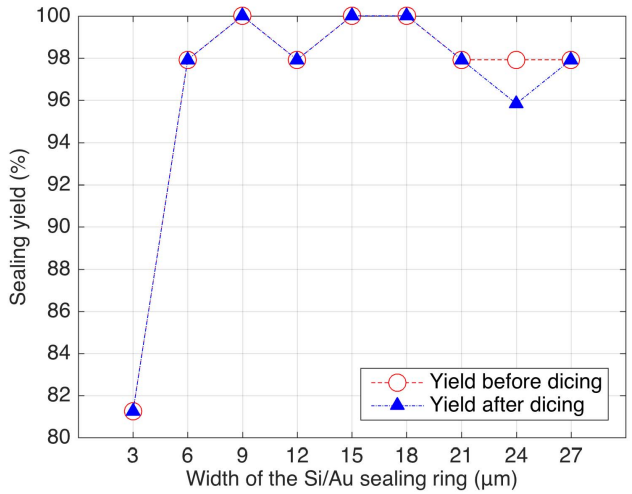

Fig. 7. Wafer-scale sealing yield as a function of the Si/Au sealing ring width before and after wafer dicing, after two months of storage in ambient pressure and at room temperature. All the 432 cavities (48 cavities for each of the nine different sealing ring widths) with large Si caps (1.5 mm × 1.5 mm, 25 μm thick) distributed over the whole wafer were used for the evaluation.

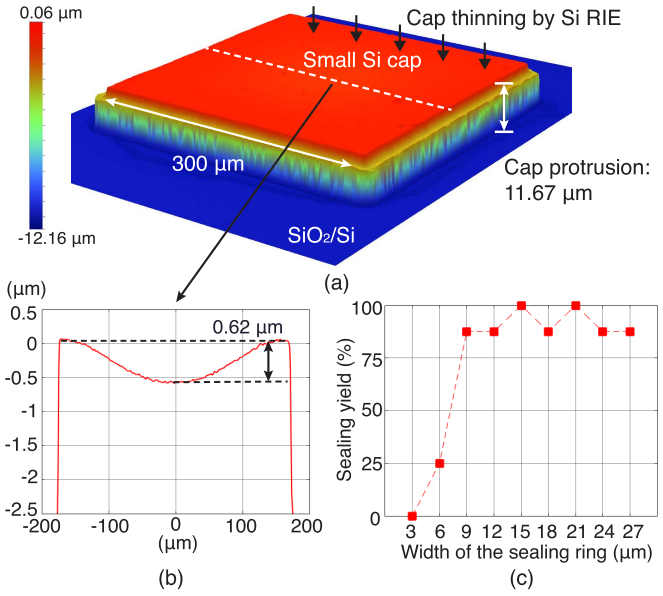

Fig. 8. Sealing yield evaluation of the small Si caps (0.3 mm × 0.3 mm) by white-light interferometry after cap thinning (~6 μm thick). (a) Measured protrusion from the cavity wafer plane of a small Si cap with a 15 μm-wide Si/Au sealing ring. (b) Measured deflection of the same small Si cap. (c) Sealing yield of the 72 evaluated small Si caps as a function of the Si/Au sealing ring width. 8 samples were used for each of the nine different sealing ring widths.

below 1 μm, i.e. a loss of the vacuum inside the package. The achieved excellent sealing yields of the large and extra-large cavities after dicing demonstrated excellent mechanical stability of the seals.

To investigate the sealing yields of the small cavities after dicing, 72 caps out of 144 (8 samples for each Si/Au sealing ring width) were thinned down to a thickness of approximately 6 μm by Si RIE so that the cap deflections due to pressure difference were significant enough to measure by white-light interferometry (Fig. 8). The deflections of the thin

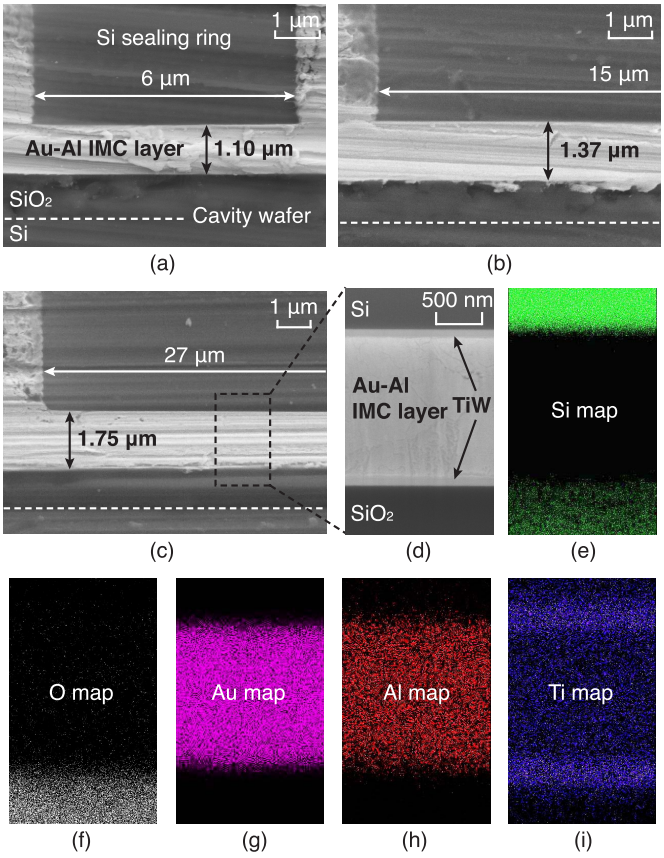

Fig. 9. Cross-sectional SEM images of the Au-Al bond interfaces. (a)-(c) Bond interfaces of 6 μm, 15 μm, and 27 μm-wide Si/Au sealing rings, respectively. (d) Focused ion beam (FIB) milled bond interface of the 27 μm-wide Si/Au sealing ring in (c). (e)-(i) Silicon, oxygen, gold, aluminum, titanium element maps of (d) by electron-dispersive X-ray spectroscopy (EDS).

small caps were all below 1 μm (Fig. 8b), which avoided any protrusion into the cavities. Although the sealing yields for the 3 μm-wide and 6 μm-wide Si/Au sealing rings were low, all the other Si/Au sealing ring widths resulted in high sealing yields (Fig. 8c). After cap thinning, the cap protrusions were measured to be within 12 ± 1 μm from the cavity wafer plane, which is dimensionally compatible with the heights of various fine-pitch solder or stud bumps for flip chip bonding [48].

B. Inspection of Bond Interfaces

To inspect the bond interfaces between the Si/Au sealing rings and the corresponding Al sealing rings, randomly selected large cavities were diced along the central axes of the sealed cavities. The scanning electron microscopy (SEM) images of three diced Au-Al bond interfaces are shown in Fig. 9. Three representative types of Si/Au sealing ring widths, i.e. 6 μm, 15 μm, and 27 μm, were compared and showed different degrees of plastic deformation of the Au-Al metal stacks (Fig. 9a–9c). The original 2.65 μm-thick Au-Al metal stacks were compressed to 1.10 μm, 1.37 μm, and 1.75 μm-thick Au-Al intermediate metal compound (IMC) layers, respectively. This difference in thickness was attributed to resulting nonuniform bonding pressures at different sealing ring structures on the cap wafer.

To investigate the resulting solid-state diffusion conditions in the Au-Al intermediate metal compound layers, the bond interface of the 27 μm-wide Si/Au sealing ring was milled using a focused ion beam (FIB, gallium ion) and analyzed by energy-dispersive X-ray spectroscopy (EDS), as shown in Fig. 9d–9i. The resulting element maps confirmed the expected compositions and locations of the different layers in the inspected bond interface. Especially, the uniform distribution of the Au and Al elements in the intermediate metal compound layers demonstrated uniform inter-atomic diffusion at the bond interface, although individual micro-voids were sometimes found at the bond interfaces. The EDS analysis revealed an Au to Al atomic ratio of more than 4.8, indicating that the formed IMCs were likely to be Au_4Al or a combination with Au_8Al_3, which is in agreement with the resulting IMCs of previous work where Au-Al wire bonds underwent a similar thermal process at 250 °C [49]. In addition, the exposed Au-Al IMCs have a tan color after shear testing (Fig. 13), indicating the presence of Au_4Al or Au_8Al_3 rather than brittle 'purple plague' $AuAl_2$. These two types of Au-rich IMCs are considered to be ductile [50], [51], and thus potentially beneficial for the reliability of the bond.

C. Leak Rate Evaluation

The leak rates of the sealed cavities were evaluated by monitoring the thin cap deflections over a period of two months. For a square cap with four clamped edges, the deflection W at the center of the plate due to the pressure difference of the sealed cavity pressure and the ambient atmosphere can be calculated using the following equation [52]:

$$W = \frac{3a^4\left(1-\mu^2\right)P}{188Ed^3} \tag{1}$$

where a and d represent the width and thickness of the cap, respectively. P is the differential pressure, and E and μ stand for the Young's modulus and Poisson's ratio of the plate material, respectively. Since the deflection at the center of the cap is proportional to the differential pressure, the true leak rate L_a can be calculated using the following equation [46]:

$$L_a = \ln\left(\frac{W_{t_1}}{W_{t_2}}\right)\left(\frac{V\,P_0}{t_2-t_1}\right) \tag{2}$$

where W_{t_1} and W_{t_2} represent the measured deflections at time points of t_1 and t_2, respectively. V is the cavity volume, and P_0 is the reference ambient pressure, i.e. standard 1 atmosphere. 30 large Si caps with three representative types of Si/Au sealing ring widths of 6 μm, 15 μm, and 27 μm (10 samples for each type) were randomly selected from different locations of the cavity wafer and measured during the two-month period. The changes in ambient pressure were compensated for using data from a pressure gauge in the lab. The deflection measurement results are shown in Fig. 10.

As can been seen from Fig. 10, the average deflections are the largest for Si caps with 6-μm wide Si/Au sealing rings, and the smallest for Si caps with 27-μm wide Si/Au sealing rings. This difference is also significant between Si caps that are located adjacently on the wafer and thus have nearly identical cap thicknesses. This cannot be explained by equation (1) and could be due to the difference in the effective bending stiffness of the caps caused by different sealing ring widths. In order to investigate this, simulations (Comsol Multiphysics) were performed for three evaluated Si/Au sealing ring widths using our cap geometries (1.5 mm × 1.5 mm large, 25 μm thick) and the material properties of single-crystalline Si and typical Au (Fig. 11a). For simplification, the Au layer on the Si cap was ignored because it was much thinner than the Si cap and Au has much lower Young's modulus than Si. Deflection data from 15 Si caps (5 caps for each sealing ring width) located close to the center of the wafer (similar cap thickness) were also plotted in Fig. 11a to compare them with the simulation results. As can be seen from Fig. 11a, the simulated cap deflection indeed varies with the Si/Au sealing ring width, and is in good agreement with the measured data. This confirms that the sealing ring width does cause differences (non-linear) in the effective bending stiffness of the caps.

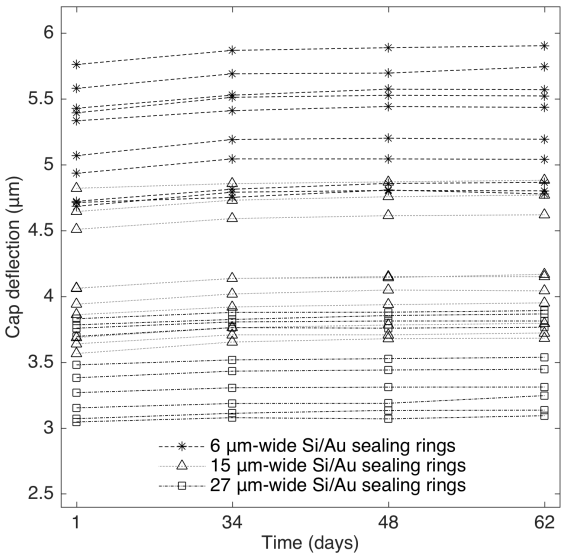

Fig. 10. Si cap deflections (23–25 μm-thick caps) over a period of two months. The data was collected from 30 large caps (1.5 mm × 1.5 mm) with three different Si/Au sealing ring widths and has been adjusted to compensate for ambient pressure variations. For each type of cap, 10 samples located at different positions of the cavity wafer were randomly chosen and measured.

To validate the assumption that the cap deflection is proportional to the differential pressure, we simulated the cap deflection as a function of the differential pressure using our Comsol model (see Fig. 11b). The deflections of the different caps with the three evaluated sealing ring widths all exhibit linear dependency on the differential pressure load, indicating the validity of using equation (2) for evaluating the leak rates. Cap deflection values calculated using equation (1) were also plotted in Fig. 11b. The predicted values are in good agreement with the simulation results for the caps with the wide sealing ring (27 μm), which is reasonable since the edge fixation conditions of the caps with wide sealing rings are closer to the assumed clamped fixation used in equation (1).

The variations in the thickness of the Si caps (23–25 μm) resulting from etch rate difference across the wafer during DRIE of the Si sealing rings, contributed to the difference in the deflections of the caps with the same sealing ring width.

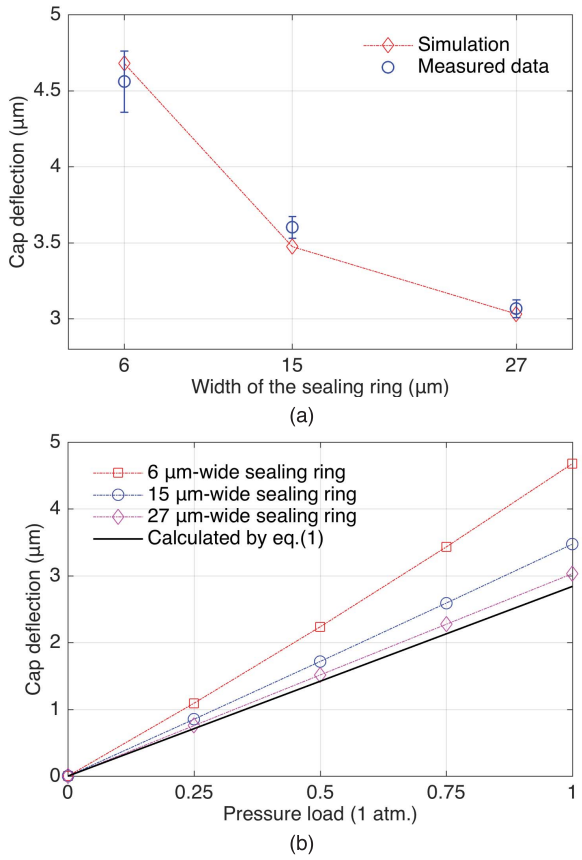

Fig. 11. Simulation of Si cap deflection as a function of the Si/Au sealing ring width and differential pressure load using Comsol. Cap dimensions used in the simulation: 1.5 mm × 1.5 mm large, 25 μm thick, and Si/Au sealing ring dimensions: 6 μm/15 μm/27 μm wide, 5 μm high for Si rings, and 1.10 μm/1.37 μm/1.75 μm high for Au rings (according to Fig. 9). Material properties for single-crystalline Si and typical Au: 170 GPa/ 70 GPa as Young's modulus and 0.28/0.44 as Poisson's ratio, respectively. (a) Simulated Si cap deflection with respect to three different Si sealing ring widths. Data from 15 caps (5 caps for each sealing ring width) located close to the center of the wafer (similar cap thickness) were plotted for comparison. (b) Simulated Si cap deflection (three different sealing ring widths) with respect to differential pressure load.

This was confirmed by calculating the equivalent cap thickness spread by using equation (1) with the measured deflection spread (3.04–3.83 μm) of the caps with 27 μm-wide sealing rings from Fig. 10, which is derived to be 22.6–24.4 μm and thus, is in agreement with the measured cap thickness variations.

There was no significant decay trend of the cap deflections during the evaluation period since both positive and negative changes of the deflections are present in the data in Fig. 10, which reflects the noise level and thus, the detection limit of our measurement. The variations in the measured cap deflections over the entire period were within $\pm$0.16 μm, among which the higher variations were from the caps with 6 μm-wide Si/Au sealing rings. The detection limit of the leak rate can be conservatively calculated, using (2) with the largest deflection change of 0.16 μm, the calculated cavity volume of 0.185 mm^3, the reference ambient pressure of 1013.25 mbar, and the smallest deflection of 4.68 μm from the data group with 6 μm-wide Si/Au sealing rings.

TABLE II
RESIDUAL GAS ANALYSIS RESULTS OF THREE CAVITIES WITH DIFFERENT SI/AU SEALING RING WIDTHS

Gas	6 μm-wide seal		15 μm-wide seal		27 μm-wide seal	
	Pressure [mbar]	Percent [%]	Pressure [mbar]	Percent [%]	Pressure [mbar]	Percent [%]
Ar	4.3×10^{-1}	31.88	7.3×10^{-1}	30.91	2.0	59.28
CO_2	4.1×10^{-1}	30.40	6.0×10^{-1}	25.40	3.4×10^{-1}	10.08
H_2	2.0×10^{-1}	14.83	5.7×10^{-1}	24.13	5.5×10^{-1}	16.30
CH_4	2.0×10^{-1}	14.83	2.5×10^{-1}	10.58	2.6×10^{-1}	7.71
CO	9.4×10^{-2}	6.97	1.9×10^{-1}	8.04	1.9×10^{-1}	5.63
CHs[a]	1.3×10^{-2}	0.96	2.1×10^{-2}	0.89	3.3×10^{-2}	0.98
He	1.6×10^{-3}	0.12	1.0×10^{-3}	0.04	8.7×10^{-4}	0.03
N_2	0	0	0	0	0	0
O_2	0	0	0	0	0	0
H_2O	0	0	0	0	0	0
Total	1.3	100	2.4	100	3.4	100

[a] CHs represents the contribution due to ethane and propane.

The derived detection limit of the leak rate is 1.2×10^{-12} mbarL/s, which is better than reported results that have been measured using helium fine leak tests (10^{-10}–10^{-8} mbarL/s) [41], [46]. The true leak rates of the sealed cavities should be lower than this value of 1.2×10^{-12} mbarL/s.

D. Residual Gas Analysis

To get an accurate estimate of the pressure and gas composition inside the sealed cavities, three cavities with large caps (1.6 mm × 1.6mm) using different Si/Au sealing ring widths were evaluated (*SAES Getters S.p.A, Italy*) by residual gas analysis (RGA) 101 days after bonding. During the RGA, the sealed packages were mechanically opened inside an ultra-high vacuum chamber ($< 10^{-8}$ mbar) that was connected to a mass spectrometer. The gases emitted from the cavities were then guided to, and analyzed by the mass spectrometer, yielding information on the species of the gas molecules and corresponding partial pressures. The results are summarized in Table II. The overall sealed pressures were on the order of 1–3 mbar, which is comparable with reported values of 0.8–7 mbar using thin film deposition methods [13], [14], [19]. No traces of N_2 and O_2 were found in any of the tested samples, indicating that the seals were leak-tight. Ar appeared as the dominant gas for all the tested samples, which is most likely due to outgassing from sputtered Au and Al, since the Ar sputtering gas is known to be implanted into the metals during sputter deposition [53]. The other major gas species were CO_2, H_2, CO, and CH_4, which could result from reactions between residual water vapor and sputtered metals and carbon impurities present on the cavity walls in the heating step during bonding [54]. The heating was applied after the venting channels were closed by the applied bonding force, meaning that these gases resulting from outgassing and reactions were trapped in the cavities. The sample with a 6 μm-wide Si/Au sealing ring exhibited the lowest measured gas pressure of 1.3 mbar, demonstrating the excellent hermeticity achievable using such a small cavity and sealing footprint. The sample with a 27 μm-wide Si/Au sealing ring showed the highest measured gas pressure of 3.4 mbar, due to

a more significant contribution from Ar, compared to the other two samples. The difference between the three samples could be ascribed to different pumping efficiencies and nonuniform distribution of Ar and other impurities.

The sealed gas pressures were higher than the gas pressure in the wafer bonder chamber during bonding. This is expected and consistent with literature reports, since outgassing from the cavity surfaces can significantly increase the internal pressure due to the high surface to volume ratios of the small cavities. Assuming that the sealed cavity pressure increased from hypothetical absolute vacuum (0 mbar) to 1.3 mbar after 101 days of storage, a leak rate of 2.8×10^{-14} mbarL/s can be calculated. This is a worst-case estimation and the actual leak rate should be much lower than this value. Our achieved vacuum level is suitable for applications such as pressure sensors, accelerometers [19], as well as NEMS relays and MOEMS devices where O_2-free and H_2O-free atmospheres are desired [55], [56]. An additional outgassing step, use of evaporated or electro-plated metal sealing layers, and a more thorough pumping during bonding should help achieve even higher vacuum levels in the cavities, as indicated by previous work [41]. If very high vacuum levels are required, e.g. for gyroscopes or infrared bolometers, getters that absorb residual gases can be incorporated in the cavities and be activated during or after the vacuum sealing.

E. Shear Strength Testing

Shear strength testing was conducted using a shear tester (*2400PC, Dage Ltd, UK*) to characterize the mechanical stability of the seals. Data was collected from 6 samples (large Si caps) for each of the nine different types of Si/Au sealing ring widths (Fig. 12). As expected, the seals featuring 3 μm-wide Si/Au sealing rings exhibited relatively low average shear force of 4.9 N. All the other seals demonstrated sufficient average shear forces of 10–12 N, even with Si/Au sealing rings as narrow as 6 μm. No significant dependence of shear strength on the Si/Au sealing ring width was observed, except for the 3 μm-wide sealing rings. This was probably due to uneven bonding pressure distribution over the wafer, as confirmed by the different thicknesses of Au-Al intermediate metal compound layers of different sealing ring widths shown in Fig. 9. The widening of the Au-Al sealing rings after bonding was taken into account when calculating the shear strengths. All the calculated average shear strengths were higher than 60 MPa, which is four times higher than the conservative pass criterion of 12.4 MPa for die shear strength in the military standard [57]. Despite the narrow sealing footprints, the seals with 6 μm and 9 μm-wide Si/Au sealing rings demonstrated high mean shear strengths of 156 MPa and 127 MPa, respectively, which are higher than reported values of 28 MPa using Au-Sn eutectic bonding [31], 72.4 MPa using Cu-Sn transient-liquid-phase diffusion bonding [58], and 90 MPa using Cu-Cu thermo-compression bonding [41].

All the tested large Si caps were completely detached from the cavity substrate at the end of the test, as pictured in Fig. 13a. In some regions of the Si/Au sealing rings, the Au and TiW layers remained bonded to the cavity substrate after

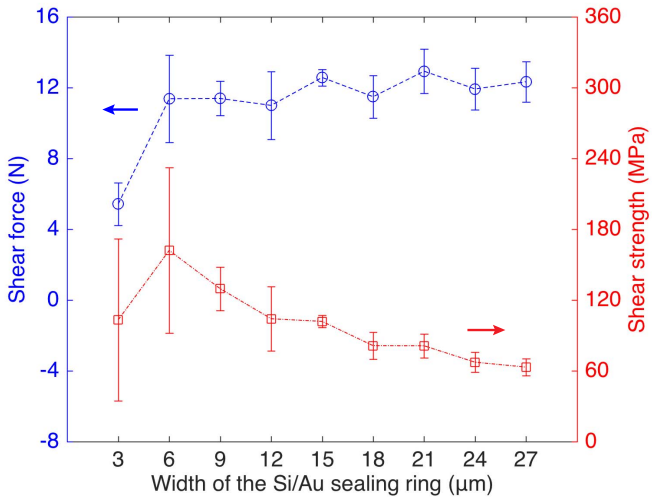

Fig. 12. Shear force and shear strength as a function of the Si/Au sealing ring width. 54 samples with large Si caps (1.5 mm × 1.5 mm) were used (6 samples for each Si/Au sealing ring width). The calculated shear strengths were compensated for widening of the Au sealing rings due to plastic deformation. Measured mean values and standard deviations are shown in the plot.

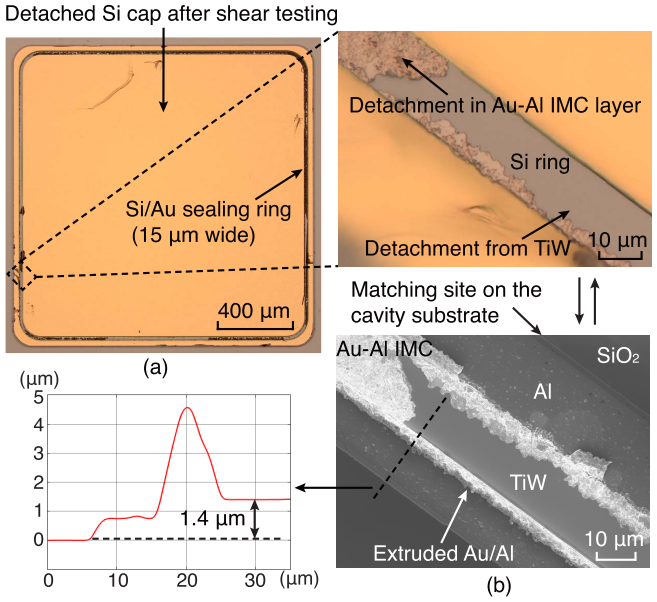

Fig. 13. Analysis of a large Si cap (1.5 mm × 1.5 mm) detached from the cavity substrate after shear testing. (a) Optical microscope image of the detached large Si cap with a close-up view of the 15 μm-wide Si/Au sealing ring. (b) SEM image of the matching site on the cavity substrate, with respect to the close-up image in (a). The cross-sectional profile indicated in (b) was measured using a profilometer (*KLA-Tencor P-15*).

shear testing (Fig. 13b). This was confirmed by the measured thickness of the remaining metal layers of 1.4 μm (from a 15 μm-wide Si/Au sealing ring), which corresponds well to the thickness of the Au-Al intermediate metal compound layer of 1.37 μm in Fig. 9b. This indicated good bond strengths of the seals.

F. Temperature Stress Testing

To evaluate the thermal stability of the Au-Al seals, 45 sealed large cavities (5 cavities for each of the nine different

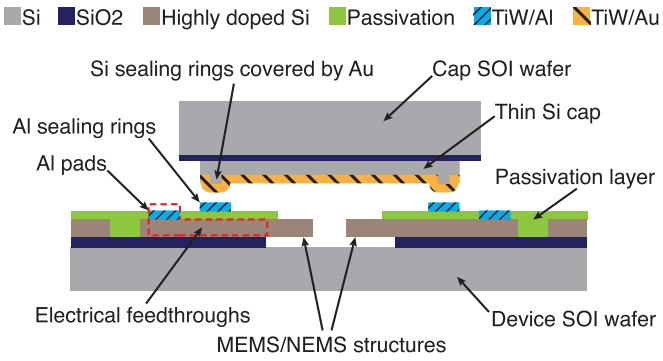

Fig. 14. A possible packaging scheme for encapsulating MEMS or NEMS devices by transfer bonding of thin Si caps and with electrical feedthroughs extending into the packages.

Si/Au sealing ring widths) were placed in an oven. The temperature was ramped up to 300 °C in nitrogen atmosphere and kept constant for 1 hour, followed by cooling down to room temperature. The temperature ramping rates for both heating and cooling were set to ∼5 °C/min. No gross leakage was observed for any of the tested samples. The tested temperature of 300 °C is higher than the typically required temperature for reflow of solders and curing of underfill materials in flip chip bonding [48], indicating that the seals are potentially compatible with flip chip bonding processes.

Furthermore, we performed thermal cycling experiments on 45 different sealed large cavities (5 cavities for each of the nine different Si/Au sealing ring widths). The temperature cycling was set between −5 °C to 100 °C for 700 cycles with a cycle rate of 1.5 cycles/h and a soak time of 5 minutes at the end-point temperatures, all in accordance with JEDEC standards A104E and 47I [59], [60]. The sealed cavities were evaluated by measuring the deflections (as described in section III.C) of the thin caps before and after the thermal cycling. For all the tested samples, the measured deflection changes (± 0.17 μm) before and after thermal cycling were close to the noise level of the measurement. Hence, no significant leakage was detected, and all the samples passed the test.

IV. Outlook

In this work, we use Au-Al thermo-compression bonding to realize vacuum packaging. This is beneficial since Al is a standard metallization, interconnect and bond-pad material in CMOS and MEMS devices, and thus the Al sealing rings could simply be patterned together with one of these layers using the same mask. A possible scheme to realize this is illustrated in Fig. 14, where typically an SOI wafer is used as the MEMS/NEMS device wafer. Firstly, during the fabrication of the MEMS/NEMS structures in the highly doped Si device layer of the SOI wafer, contact pads are opened through a passivation layer, followed by deposition and patterning of an Al layer for both electrically contacting the MEMS/NEMS devices via the Si feedthroughs, and forming the surrounding Al sealing rings in the same step. After the MEMS/NEMS device wafer is prepared, the SOI cap wafer is bonded to the device wafer using the method described in this paper. On the other hand, if lower bonding force and temperature are required, Au sealing rings can also be used instead of the Al sealing rings on the device wafer, to achieve Au-Au bonding and sealing. Au-Au bonding has been reported to achieve vacuum sealing even at room temperature [4], and Au-Au bonds are potentially more reliable than Au-Al bonds, since no brittle Au-Al intermediate metal compounds are formed, although the present work already demonstrates good hermeticity and bond strength. In addition, the presented method of wafer-level transfer bonding of thin Si caps for hermetic sealing could also be achieved using other metal-based bonding methods, e.g. transient liquid phase bonding.

The added cost of the SOI wafer used in this work can be reduced by replacing the SOI wafer with a standard Si wafer containing thermally grown SiO_2 and a layer of deposited low-stress poly-crystalline Si, which would resemble the configuration of a SOI wafer. In addition, the proposed approach could be applied to 200 mm-diameter wafers that are commonly used in industry. This would require a bonding force of approximately 64–100 kN, which is within the specifications of typical industrial wafer bonders.

The good hermeticity of 6 μm-thick small Si caps after cap thinning suggests that such thin caps could be evaluated for sealing cavities of larger dimensions, with the help of supporting walls or pillars underneath the thin caps. Additionally, testing the proposed method on actual MEMS/NEMS devices to assess the quality of the thin packages, and investigations of the influence of bonding temperature, bonding force, and thickness of the Au and Al sealing rings on the resulting hermeticity and bond strength can be the focus of future work.

V. Conclusions

A novel wafer-level vacuum packaging method based on transfer bonding of thin Si caps has been proposed and evaluated. 25 μm-thick Si caps were transferred from an SOI wafer to a cavity wafer. Hermetic sealing of the cavities was achieved by Au-Al thermo-compression bonding at a low temperature of 250 °C. Sealing yields of 98% and 100% after wafer dicing were accomplished using sealing rings as narrow as 6 μm and 9 μm, respectively. The chip-scale packages with 9 μm-wide sealing rings demonstrated a high mean shear strength of 127 MPa. Sealed vacuum levels in these getter-free packages were measured by residual gas analysis to be as low as 1.3 mbar, and the leak rate is calculated to be smaller than 2.8×10^{-14} mbarL/s. The thickness of the Si caps was also reduced to 6 μm after transfer and still maintained excellent hermeticity. Furthermore, the seals can tolerate exposures to high temperature of at least 300 °C, which makes them compatible with flip chip bonding processes. The demonstrated ultra-thin packages in combination with small footprint can be useful for vacuum and hermetic packaging of MEMS and NEMS, and for high-density system-on-chip integration of capped MEMS and NEMS with ICs by flip chip bonding, since the ultra-thin packages can potentially be placed in between the solder bumps in flip chip interfaces, thereby avoiding the need of through-cap-vias in conventional MEMS packages.

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