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A New Microfabrication Method for Ion-Trap Chips That Reduces Exposure of Dielectric Surfaces to Trapped Ions

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***Abstract*— Accumulated electrostatic charges on the dielectric surfaces of ion traps are known to induce stray fields, leading to ion micromotions. In typical microfabricated ion-trap chips, metal electrodes are electrically isolated using thick dielectric pillars, which can accumulate stray charges on their sidewalls. This letter presents a new microfabrication method for ion-trap chips that reduces the exposure of dielectric surfaces to trapped ions. The dielectric pillars are fabricated with large T-shaped overhangs, and the sidewalls and top surfaces are coated with AlCu (1%) films. The bottom sides of the overhang parts provide electrical isolation. To prevent oxidation of the AlCu (1%) films, the electrode surfaces are coated with an additional Au film. The fabricated chips were implemented to trap $^{174}Yb^{+}$ ions, and the laser-induced stray fields were measured. The results indicated that the trap chip fabricated by the newly developed method generates significantly smaller stray fields as compared with previous chips. [2017-0233]**

***Index Terms*— Ion-trap chip, microfabrication, sacrificial process.**

I. Introduction

Microfabrication is an important technology for constructing scalable qubit platforms based on trapped ions [1]–[3]. Advanced microfabrication techniques enable the integration of multiple ion-trap arrays and various functional components on a miniaturized ion-trap chip [4]–[7]. However, the ions are confined closer to the electrode structures in microfabricated ion-trap chips than in macroscopic ion traps; therefore, they are more affected by electric-field noises from various parts of the trap. Suppressing the electric-field noises poses a major challenge in microfabricated ion traps. Among these noises are laser-induced stray charges on the dielectric surfaces near the trapped ions. Stray charges can be generated by photoelectric effects when ultraviolet (UV) lasers are illuminated on the dielectric surfaces [8], [9]. Thus, the exposure of dielectric surfaces to trapped ions or propagating laser beams should be minimized. This letter develops a new microfabrication method for ion-trap chips that reduces the exposure of the dielectric surfaces to trapped ions. The fabrication processes for sputtering AlCu(1%) films on sloped sidewalls of thick dielectric pillars and patterning the AlCu(1%) films were developed. For releasing the large overhangs of the dielectric pillars, a sacrificial process using a polymeric material as a sacrificial layer was developed. The fabricated chip was implemented to trap ytterbium ions (isotope 174; $^{174}Yb^{+}$). The laser-induced stray fields were investigated by illuminating a UV laser to the chip surface and measuring the ion displacement along the axial direction. The experimental results show that the proposed electrode structures suppress the generation of stray fields, thereby reducing the ion micromotions.

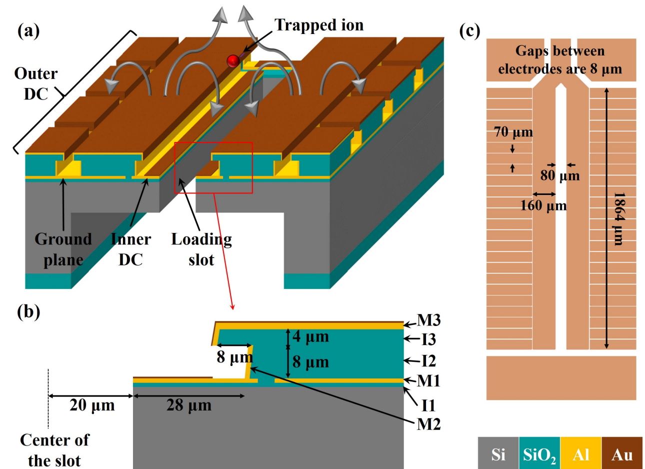

Fig. 1. Schematics of the proposed surface ion-trap chip. (a) Overview of the chip structure (not to scale). The gray arrows on the chip indicate the direction of electric field direction when a positive voltage is applied. Figure not to scale. (b) Magnified view and the dimensions of the electrode structure, showing its dimensions. (c) Layout design of the proposed chip.

II. Design

The proposed electrode structure is schematized in Fig. 1(a) and (b). The first metal (M1) layer is laid above the first insulating (I1) layer, providing inner direct-current (DC) electrodes and a ground plane. To reduce the laser scattering immediately beneath the trapped ions, the inner DC electrodes are laid on the M1 layer instead of the top metal (M3) layer. The dielectric pillars consist of two insulating layers, I2 and I3, whose sidewalls are covered by the second metal (M2) layer and the M3 layer, respectively. The lateral dimensions of the two dielectric layers differ by a sizable amount, realizing large overhangs that electrically isolate the M2 and M3 layers. The M3 layer provides the radio-frequency (RF) and outer DC electrodes. The distances between the adjacent metal layers that prevent electrical breakdown were determined in our previous experiments [10], and the lateral dimensions of the electrodes were designed in [11] (Fig. 1(c)).

III. Fabrication Method

This section describes the fabrication process. First, a 1 μm-thick SiO_2 (I1) layer was deposited by a plasma-enhanced chemical vapor

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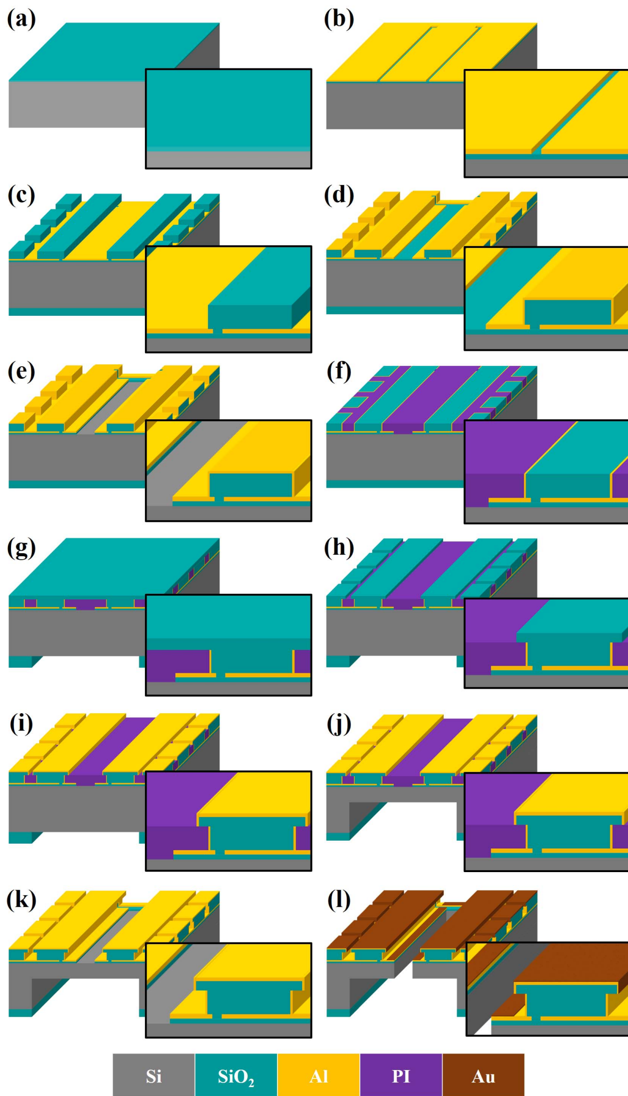

Fig. 2. Schematics of the fabrication process flow (not to scale). (a) Deposition of SiO_2 layer. (b) Deposition and patterning of AlCu(1%) layer. (c) Deposition and patterning of SiO_2 layer. (d) Deposition and patterning of AlCu(1%) layer. (e) Patterning of SiO_2 layer. (f) Deposition of polyimide layer and CMP. (g) Deposition and patterning of SiO_2 layer. (h) Patterning of SiO_2 layer. (i) Deposition and patterning of AlCu(1%) layer. (j) DRIE. (k) Removal of polyimide. (l) DRIE and deposition of Au layer.

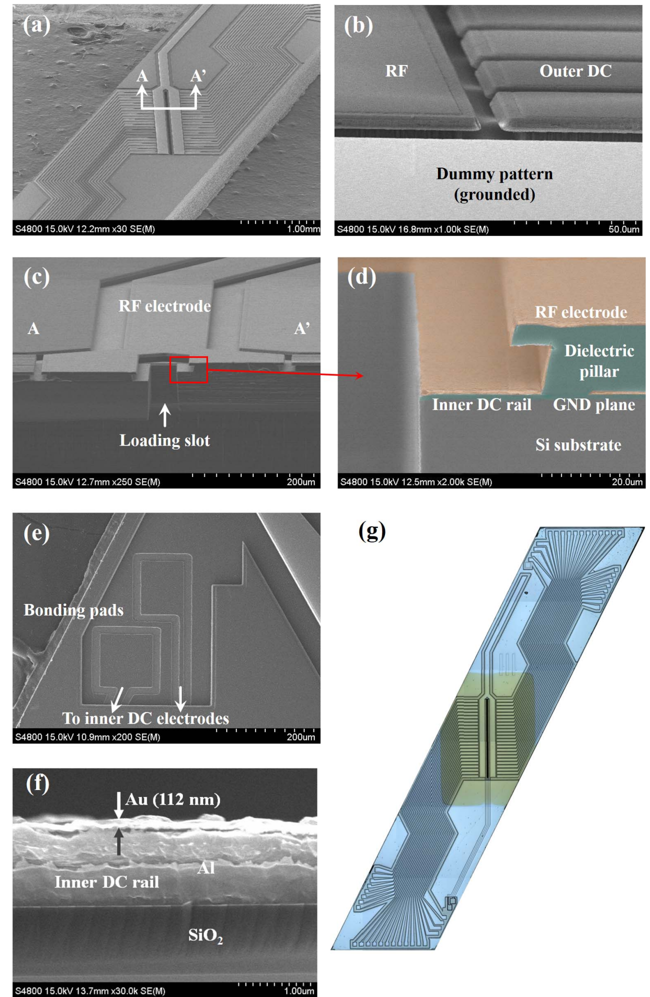

Fig. 3. Results of the developed fabrication method. (a) Top view of the entire chip. (b) Tilted view of the segmented DC electrodes (the dielectric surfaces are concealed). (c) Cross-sectional view of the trapping region. (d) Magnified view of the cross-sectional image. Image is colored for clarity. (e) Top view of the bonding pads for the inner DC electrodes laid on the M1 layer. (f) Cross-sectional view of the Au layer deposited on the AlCu(1%) layer. (g) Mosaic optical image of the entire chip.

deposition (PECVD) process (Fig. 2(a)). A 0.8-μm thick AlCu(1%) (M1) layer is sputtered and dry-etched to define the gaps between the ground plane and the inner DC rails (Fig. 2(b)). Next, a 10 μm-thick SiO_2 (I2) layer was deposited on both sides of the wafer by PECVD, and the film on the front side was dry-etched to provide the lower part of the thick oxide pillars (Fig. 2(c)). The profile of these oxide pillars is approximately 75° to allow the deposition of a metal layer on the sidewalls of the pillars. The M2 layer was also deposited on the top surfaces of the pillars. The inner DC rails and the loading slot were defined by dry- and wet-etching of the M2 layer (Fig. 2(d)). The wet-etching was required for clean etching of the metal residue on the pillar sidewalls. The I1 layer between the inner DC electrodes was dry-etched to reveal the silicon substrate (Fig. 2(e)). A polyimide (PI-540, ACT corp., Republic of Korea) layer was spin-coated and cured at 300° C for 2 hours. The fabricated structures were planarized by a chemical mechanical polishing (CMP) process (Fig. 2(f)). After the CMP process, the oxide pillars were approximately 8 μm thick, and their separation gaps were filled with polyimide material. A 4 μm-thick SiO_2 (I3) layer was then deposited on both sides of the wafer. The SiO_2 layer on the back side was dry-etched, defining a hard mask for a deep reactive ion etching (DRIE) process (Fig. 2(g)). The I3 layer was also dry-etched, providing the upper part of the oxide pillars (Fig. 2(h)). To form the RF and outer DC electrodes, a 1.5 μm-thick AlCu(1%) (M3) layer was sputtered and dry-etched on the I3 layer (Fig. 2(i)). The back of the silicon wafer was etched to a depth of 470 μm by the DRIE process (Fig. 2(j)). After the DRIE process, the wafer was diced into several pieces. At the beginning of the die-level process, the polyimide sacrificial layer was removed by a photoresist remover (PRS-2000, J. T. Baker, United States) and an O_2 plasma ashing process (Fig. 2(k)), releasing the overhung oxide pillars. The loading slot was then penetrated from the front of the wafer by DRIE. Finally, a 10 nm-thick Ti layer and a 100 nm- thick Au layer were sequentially deposited on the chip surface by sputtering processes with a shadow mask (Fig. 2(l)).

IV. Results

The fabrication results are shown in Fig. 3. Large overhangs were fabricated on the dielectric pillars, and the pillar sidewalls

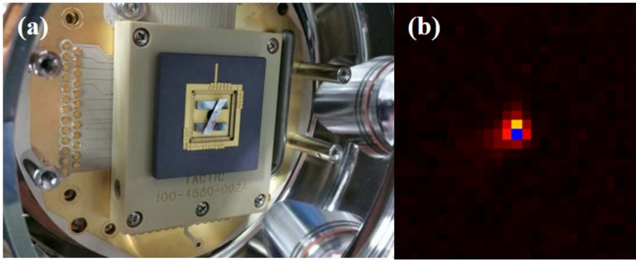

Fig. 4. Ion trapping experiment. (a) Fabricated trap chip mounted on the chip carrier and installed inside the UHV chamber. (b) Electron multiplying charge-coupled devices (EMCCD) image of a $^{174}\mathrm{Yb}^{+}$ ion trapped using in the fabricated trap chip.

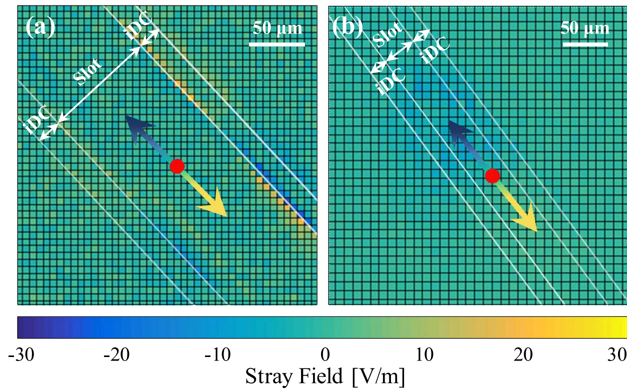

Fig. 5. Laser-induced stray fields measured in the experiments. The color of each pixel represents the intensity of the induced stray field when a UV laser is injected at that point. Blue and yellow arrows indicate the direction of the stray fields. The red dot marks the position of the trapped ion. (a) When the laser beam injects near the electrode edges, the stray fields are noticeably increased in the structure with exposed dielectric sidewalls (b) but are markedly suppressed in the proposed trap chip.

were covered by separate AlCu(1%) films (Fig. 3(a)–(e)). The shadow mask prevented undesirable electrical shorts by the Au layer deposited on the top electrodes and the inner DC rails (Fig. 3(f), (g)). Following the procedures in [10], the fabricated chip was mounted on a ceramic chip carrier (CPG10039, NTK Ceramic, Japan), and installed inside an ultra-high vacuum (UHV) chamber, as shown in Fig. 4(a). A $^{174}\mathrm{Yb}^{+}$ ion was trapped by an RF voltage of 90 V (peak-to-peak) at 23.75 MHz (Fig. 4(b)). The radial secular frequencies were 1.51 and 1.23 MHz, and the corresponding stability q-parameter was 0.18.

To evaluate the effectiveness of the proposed electrode structure, the laser-induced stray fields were measured at the $^{174}\mathrm{Yb}^{+}$ ion position. Electrostatic charges were induced by a 355-nm pulse laser (Paladin, Coherent, United States) guided to the chip surface through the front view port of the UHV chamber. The laser beam was injected perpendicularly to the chip surface. The exposure time, estimated beam power at the chip surface, and laser spot size were 0.5 s, 40 μW, and $\sim$8 μm, respectively. After injecting the laser, the ion displacements along the axial direction were measured from images captured by electron multiplying charge-coupled devices (EMCCDs). The measurement unit was an EMCCD pixel. To calculate the stray fields from these results, we measured the ion displacements induced by a sample DC voltage set, and the stray field induced by the same voltage set is calculated through electric field simulations. Using the ratio of the measured ion displacement and the estimated electric field generated by the sample voltage set, we transformed the measured data in the camera-pixel units into electric-field data (in V/m) at the ion position. The experimental results are presented in Fig. 5. In the trap chip with AlCu(1%) electrodes and exposed dielectric sidewalls [8], laser injection near the electrode edges induced relatively intense stray fields (Fig. 5(a)). On the other hand, when the laser was focused on the surface or edges of the electrode in the proposed chip, minimal stray fields were induced (Fig. 5(b)). These results indicate that shielding the sidewall with AlCu(1%) and coating the top electrodes with Au films suppresses the generation of stray fields induced by accumulated electrostatic charges.

V. Conclusion

This letter described a new microfabrication method for ion-trap chips that reduces the exposure of the dielectric surfaces to trapped ions. Trap chips were fabricated by the developed method and implemented to trap $^{174}\mathrm{Yb}^{+}$ ions. To investigate the effectiveness of the proposed structure, stray fields were induced by illuminating a UV laser light on the surfaces of trap chips with and without the application of the proposed shielding method. The proposed electrode structures significantly reduced the stray fields induced by built-up charges on dielectric surfaces.

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