CMOS-Compatible Hollow Nanoneedles With Fluidic Connection

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Abstract—**Nanoneedles are used for a variety of different biomedical applications such as intracellular injection/extraction and electrical recording. Combining these two capabilities in one device, however, remains challenging. We propose a novel method for fabricating fluidically connected arrays of hollow nanoneedles and characterize the resulting devices regarding their fluidic and electrochemical functionalities. The fabrication process relies solely on complementary metal-oxide-semiconductor (CMOS) compatible and scalable microsystems technology methods. Fluorescence microscopy is used to prove the successful transport of molecules through the passive nanoneedle chips. Electrochemical measurements of ion flows through these devices further confirm both the fluidic contact and the validity of an analytical model used to estimate the electrical resistance of the chips. In total, the presented work paves the way for monolithic integration of fluidic and electrical functionalities for intracellular contacting in a single device. This, in turn, can enable controlled, continuous drug delivery with simultaneous electrical recording on a highly scalable platform.** [2023-0171]

Index Terms—**Hollow nanoneedles, nanopipettes, intracellular access, drug delivery, integrated microfluidics, post-CMOS processing, biomedical transducers.**

I. INTRODUCTION

NANONEEDLES can provide access to the cytosol which makes them valuable in biomedical research [1], [2], [3]. The intracellular access can, for instance, be used to record electrical signals and thus provide insights into cell behavior and communication. Arrays of needles which penetrate several cells simultaneously further enable the study of cell (e.g. neural or cardiac) networks. Another application is the delivery/extraction of substances to/from pierced cells which can be used for transfection and research on treatments for various medical conditions.

In principle, two strategies for nanoneedle assisted intracellular delivery can be distinguished. The first approach uses solid nanoneedles which are coated with the molecules to be administered. When a cell is pierced by the needle, the cargo is delivered. The precise timing of the delivery, however, is difficult to determine and control. Moreover, this method does not allow repeated or continuous delivery without extracting and reloading the needles [4]. Therefore, a second strategy employs hollow nanoneedles with a fluidic connection from the backside, allowing for more flexible, longer and more controlled injections.

Several corresponding nanoneedle devices have been developed using different fabrication methods. A perforated membrane such as a track-etched polycarbonate or an anodized aluminum oxide membrane can, for instance, be used as a template of which the walls are coated with the desired nanoneedle material [5], [6], [7], [8]. The hollow cylinders thus created in the template holes are subsequently released with a timed selective etch of the substrate. A template for the nanoneedles and the fluidic connection can also be created in silicon wafers using deep reactive ion etching (DRIE) and/or KOH wet etching [4], [9], [10]. The walls of this template are then covered with thermally grown SiO_2 and the needles are released from the silicon substrate by selective etching techniques. Yet another option for creating nanoneedles on top of a fluidic channel is to use a focused ion beam (FIB) to mill holes into a photoresist [11], [12], [13]. In the process, the walls of the holes are exposed to secondary electrons and thus form the hollow nanoneedles after development of the photoresist. Moreover, metal organic vapor phase epitaxy (MOVPE) can be used to grow nanowires which are subsequently coated with the needle material [14], [15]. The nanowire core is then selectively removed and the remaining nanoneedles are connected to a backside fluidic channel.

With these methods, hollow nanoneedles of various geometries, heights, diameters, pitches and materials have been fabricated. However, none of the described techniques allows a monolithic complementary metal-oxide-semiconductor (CMOS) integration. They are not performed on silicon wafers and/or rely on KOH wet etching or process temperatures above 500 °C which are not compatible with post-CMOS processing. In contrast, the fabrication method developed here exclusively uses scalable low temperature and dry etching processes on silicon wafers. The fabrication of both hollow nanoneedles using a sacrificial layer process [16] and thin perforated membranes with fluidic connection [17] has been demonstrated by our group before. Here, the two

TABLE I

TOOLS AND MAXIMUM PROCESS TEMPERATURES (T) USED IN THE
FABRICATION PROCESS. FOR THE DRIE, RIE AND IBE,
THE TEMPERATURE TO WHICH THE WAFER BACKSIDE
IS COOLED IS INDICATED. GRINDING AND DICING
ARE PERFORMED AT ROOM TEMPERATURE

Process	T (°C)	Tool
ALD	300	P-300B, Picosun Oy
PECVD	400	DCVD Centura, Applied Materials Inc.
Lithography	205	ACS200 Gen3, SÜSS MicroTech SE and PAS5500/200B, ASML Netherlands B.V.
RIE	45	Centura 5200 Etch System, Applied Materials Inc.
DRIE	10	Tegal 200, Tegal Corp.
IBE	20	scia Mill 200, scia Systems GmbH
CVE	20	XERIC SVR XeF2/HF, Memsstar GmbH
Grinding	25	DAG810, DISCO Corporation
Dicing	25	DFD651, DISCO Corporation

concepts are combined to create fluidically connected hollow nanoneedles with well defined geometries. After fabrication, the basic functionalities of the resulting devices are characterized. Transport of substances across the nanoneedles is performed and evaluated and electrochemical measurements of ion currents through the chips are compared to corresponding analytical estimations.

II. HOLLOW NANONEEDLE FABRICATION

A. Fabrication Concept

Fig. 1 illustrates the process flow developed here for the fabrication of hollow nanoneedles with fluidic connection and Table I lists all the tools used and the corresponding maximum process temperatures. 200 mm silicon wafers with a thickness of 725 μm ± 25 μm are used as substrates which are first coated with Al_2O_3 by means of thermal atomic layer deposition (ALD). In a plasma-enhanced chemical vapor deposition (PECVD) process, a layer of SiO_2 is subsequently deposited which the nanoneedles are later anchored in (a). Therefore, this membrane is structured (b) using reactive ion etching (RIE) and then coated by thermal ALD to form the needle bases. This Al_2O_3 layer serves to protect the membrane material from subsequent etching processes.

A sacrificial layer of amorphous silicon (a-Si) is then added by means of PECVD (c). Following projection lithography, a DRIE process etches holes for the nanoneedles into the sacrificial layer (d). This DRIE process uses an inductively coupled plasma (ICP) power of 1 kW and a radio frequency (RF, 13.56 MHz) power of 5.5 kW. Next, thermal ALD is used to cover the walls of the holes with Al_2O_3 (e). After horizontal layers of the Al_2O_3 are removed using anisotropic ion beam etching (IBE), vertical hollow nanoneedles made of Al_2O_3 embedded in the anchoring membrane and the sacrificial layer remain (f). To further protect the nanoneedles during backside processing, an additional a-Si layer is deposited on top by PECVD (g). This protection layer allows to turn the wafer upside down and process the backside without using an additional carrier wafer.

Analogous to the process described before [17], the substrate is subsequently thinned by grinding (h) and an Al_2O_3 hard mask is deposited on the backside. This masking layer
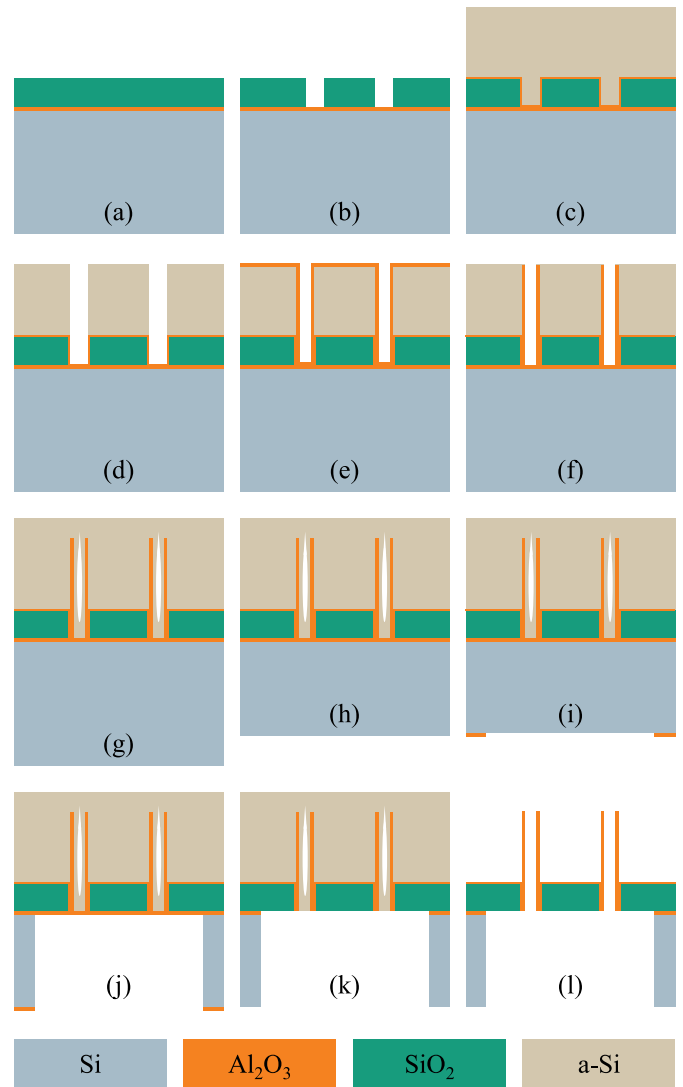

Fig. 1. Concept for fabricating hollow nanoneedles connected to a backside fluidic channel. (a) ALD of an etch stopping layer and PECVD of a membrane layer, (b) lithography and RIE for structuring the membrane, (c) ALD of the needle base and PECVD of a sacrificial layer, (d) lithography and DRIE for structuring the sacrificial layer, (e) ALD of the needle material, (f) IBE for removal of horizontal layers from the previous deposition, (g) PECVD of a protection layer, (h) grinding for thinning the Si wafer substrate, (i) ALD of a backside hard mask and RIE for structuring the same, (j) DRIE of the fluidic channel, (k) IBE for removal of the etch stopping layer, (l) CVE for removal of the protection and sacrificial layer.

is structured by RIE (i) and the cavities are etched through the entire wafer in a DRIE process (ICP power: 3 kW, RF power: 5.5 kW) which is stopped on the Al_2O_3 layer underneath the membrane (j). This etch stopping layer is then removed by anisotropic IBE (k) before the protection and the sacrificial layer are removed (l) by isotropic chemical vapor etching (CVE). XeF_2 is employed in this process which etches the a-Si selectively to both the membrane and the nanoneedles.

Dicing can be performed before or after step (l). If the a-Si layers are removed on chip level, the chips are placed on a carrier wafer for the CVE. On the specially grooved carrier wafer, the chips are only secured by form-fit and not by force or material fit so that releasing the chips from the carrier wafer does not pose a risk of damage.

B. Geometric Parameters

In total, 16 different designs of the device were fabricated with varying number (5, 9, 64, 100, 256 and 400), outer diameter (500 nm, 1 μm and 2 μm) and pitch of the nanoneedles on each cavity. The membrane thickness (800 nm), the needle height (2 μm), the needle wall thickness (50 nm), the thickness of the needle base (25 nm) and the thickness of the etch stopping layer (50 nm), by contrast, were kept constant. In principle, however, these parameters can flexibly be adjusted as well by altering the thickness of the depositions in steps (a), (b), (c) and (e), respectively. Similarly, the diameter of the cavities (50 μm) and the number of fluidic channels per chip (16) were kept constant but can be controlled by adjusting the backside lithography. The total thickness of the devices can in turn be adapted by modulating the grinding step (h). Here, chips with two different thicknesses (750 μm and 450 μm) were fabricated. All these diameters, heights and thicknesses, however, are nominal values which the resulting dimensions vary from slightly.

C. Fabrication Results

Micrographs of the resulting nanoneedles connected to a backside cavity are shown in Fig. 2. The positions and measurements of the nanoneedles and the underlying channel and membrane are well defined. In two of the micrographs, a darker circle around the needle arrays is visible: Under the light microscope, the fluidic channel can be seen through the translucent membrane (b), whereas the scanning electron microscope (SEM) detects differing charging of the thin membrane the needles are anchored in (c). The FIB-SEM analysis (e) further confirms both the connection of the hollow needle cylinder to the backside cavity and the stable anchoring of the needles in the membrane. The etch stopping layer underneath the membrane is not visible, proving its successful removal. Moreover, the inner needle channel has a slightly conical form but is uninterrupted and crosses the entire membrane. Fluidic connection between the front and the backside of the chip is thus established through the needle and cavity.

Measurements of the wafer thickness after thinning provide information about the precision of the process. The mean thickness of the wafers after grinding is 450 μm ± 5 μm. The standard deviation in the thickness across an individual wafer is 1.4 μm or lower which is negligible compared to the diameter and remaining thickness of the substrate. By comparison, backside DRIE results in a standard deviation of 5 μm across an individual wafer with the same wafer-to-wafer deviation in mean thickness. However, these thickness and etching variations across the wafer are compensated for by slight overetching in step (j). As the DRIE for creating the fluidic channels is stopped on the Al_2O_3 stopping layer and the etching selectivity between the Si and the Al_2O_3 is large, no negative effects of this overetching were observed.

Similarly, inhomogeneities in the etching rate of the DRIE for creating the needle cylinders are balanced by short overetching into the Al_2O_3 stopping layer as well. Therefore, the needle height is well defined by the height of the
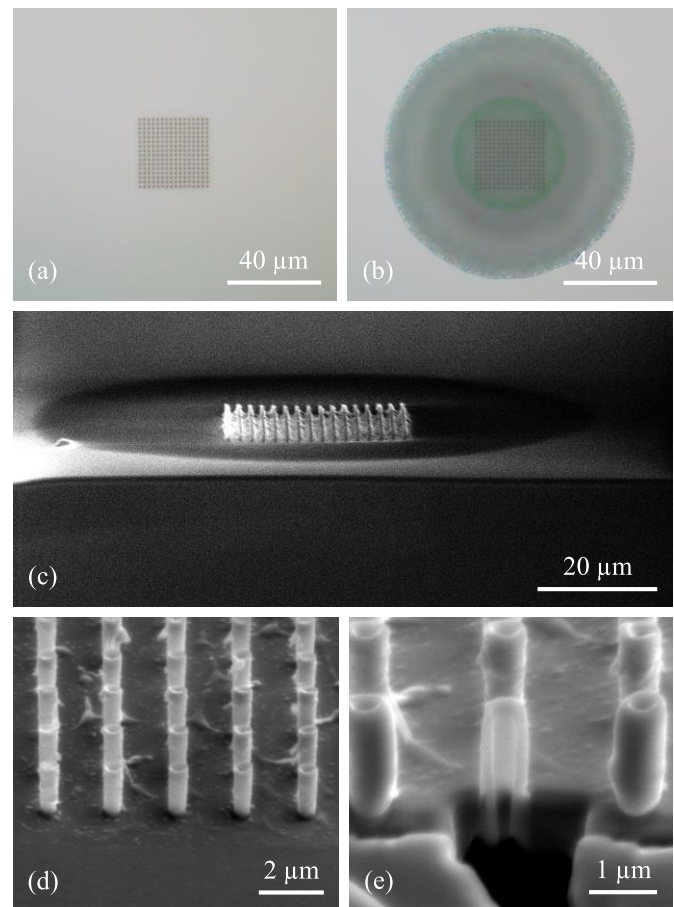

Fig. 2. Microscopic analysis of the resulting nanoneedle chips. Top view of an array of 256 nanoneedles (a) before and (b) after etching the fluidic channel from the backside. The fluidic channel is visible through the membrane as a green/blue circle around the needle array. Scanning electron micrographs of the same nanoneedle array connected to a backside fluidic channel: (c) Overview of the array and close-up on several needles (d) before and (e) after cutting through one of them using a FIB. The needles analyzed in the FIB-SEM (images (d) and (e)) are coated with an additional layer of carbon for enhanced visualization.

sacrificial layer. Measurements after its deposition revealed that the thickness of the sacrificial layer is 1.88 μm ± 0.15 μm instead of the intended 2 μm. The resulting nanoneedle height, determined with SEM recordings at 36 randomly chosen sites across 10 wafers, is 1.72 μm ± 0.14 μm. Thus, the needles are about 160 nm shorter than the sacrificial layer is thick. This height reduction is mostly due to material removal at the top of the needle template during steps (d) and (f). Among individual needle arrays like the one shown in Fig. 2, however, no significant variations in the needle height were observed.

In comparison, the needle diameters are more homogeneous as the standard deviation across a given wafer is smaller than 5 % of the nominal value. Moreover, the needle diameters can well be controlled with the parameters of the exposure during lithography. In respective experiments, the mean diameters could be adjusted by about 130 nm without changing the lithography masks. For the chips analyzed here, the lithography parameters were chosen to create a mean outer diameter at the needle top of 565 nm. This is larger than the intended 500 nm to counterbalance the conical etching profile.

In these experiments on correlating lithography parameters to resulting needle diameters, the lowest inner diameter measured at the bottom of a needle was 160 nm. A smaller diameter could not be fabricated because the resolution limit of the i-line stepper did not allow further reduction of this dimension. Thus, the lithography diameter at which the needles clog due to the conical needle walls could not be determined.

III. EVALUATION OF FLUIDIC FUNCTIONALITY

To evaluate the transport of substances across a given nanoneedle chip, fluorescent particles are used. Microscopy images and corresponding simplified illustrations of the procedure are shown in Fig. 3. First, the chip is treated in an O_2 plasma for 10 min to improve the wettability of its surface. Then, the fluidic channels and the nanoneedles are filled with a solution of acriflavine in deionized water and the chip is observed under a fluorescence microscope. After applying a drop of deionized water on top of the chip, the particles diffuse into the drop. As the membrane is translucent, however, the fluorescent particles in the cavities can generally not be distinguished from particles on top of the membrane. Therefore, the concentration of acriflavine in the fluidic channels is raised to the point that the particles inhibit each other and no fluorescence is detectable. The intensity of the light emitted by the solution in the cavities is thus low in comparison to the light emitted by a solution with lower concentration of acriflavine. When the particles start to diffuse into the drop on top of the chip, the concentration in the drop is initially lower than the concentration in the channel underneath the membrane. The transport of particles across the membrane is therefore proven by the detection of a changing intensity of the emitted light after applying the drop of water to the chip surface. This experiment was successful for plasma treated chips without defects as shown in Fig. 3. Without the plasma treatment before the experiment, however, no transport of particles across the chips could be detected.

IV. ELECTROCHEMICAL CHARACTERIZATION

A. Setup for Electrochemical Measurements

For measuring ion currents flowing through the nanoneedle device, a given plasma treated chip is placed between two chambers, each containing a Ag/AgCl electrode and an opening for the chip (see Fig. 4). This procedure is based on setups described in [17], [18], and [19]. As the interface between the edges of the chip and the two reservoirs is properly sealed, the fluidic channels in the chip are the only fluidic connection between the two chambers. A solution of KCl in water is then added to the reservoirs and a linear voltage sweep is applied between the two electrodes. The ionic currents passing the nanoneedle chip are subsequently recorded, analyzed and compared to analytical estimations. Before and after each measurement, the setup is manually and macroscopically inspected for defects. Obstruction of one or more fluidic channels by the gaskets, leaks or deficient chloridization of the electrodes can thus be spotted and the respective measurements can be eliminated from further analysis.
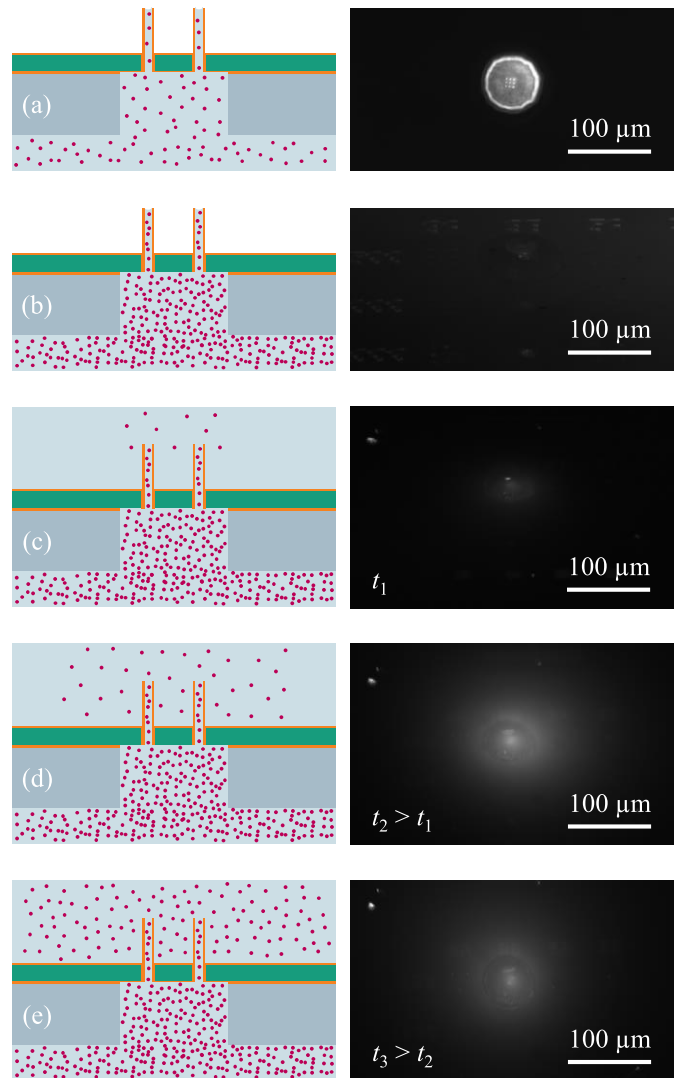

Fig. 3. Microscopic analysis of the transport of fluorescent particles through a plasma treated nanoneedle chip: Top view micrographs and respective cross-sectional sketches of an array of needles anchored in a membrane on top of a fluidic channel filled with a solution of acriflavine in deionized water. (a) The concentration of acriflavine in the cavity is set so that the fluorescence can be seen through the translucent membrane. (b) At a higher concentration of acriflavine in the cavity, the particles inhibit each other so that no fluorescence is detected. (c) A drop of water is applied to the top surface of the chip at t_0 so that the acriflavine particles start to diffuse through the nanoneedles (t_1). (d) As the diffusion process continues and the concentration of acriflavine on top of the membrane increases, the fluorescence grows brighter and its radius larger. (e) The acriflavine concentration on top of the membrane increases further so that the particles begin to inhibit each other and the intensity of the emitted light decreases again.

B. Electrical Resistance Estimation

Similar to the model described previously [17], the electrical resistance of the nanoneedle chips filled with electrolyte solution can be estimated using equation 1:

$$R_{\text{Chip}} = \frac{1}{n_c \kappa_e} \left(\frac{l_c}{\pi r_c^2} + \frac{1}{4r_c} + \frac{l_n}{n_n \pi r_n^2} + \frac{1}{4n_n r_n} \right), \quad (1)$$

where

- R_{Chip} is the total resistance of a given chip,
- n is the number of cavities (index c) per chip or needles (index n) per cavity,
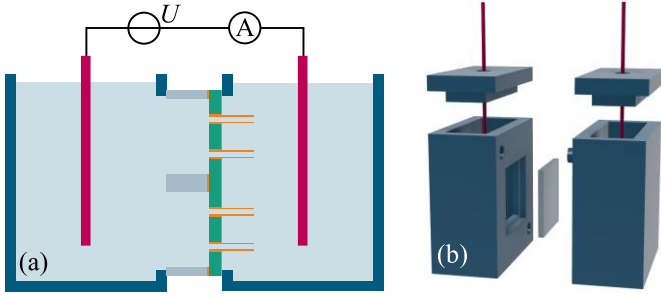
Fig. 4. Illustration of the setup for the electrochemical measurements: (a) Conceptual drawing and (b) exploded-view of a computer-aided design (CAD) model.
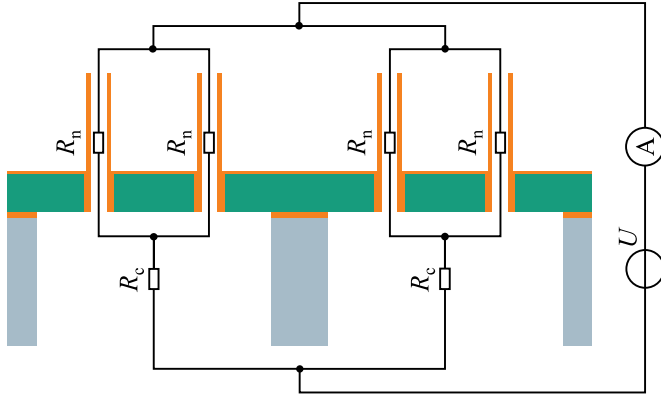

Fig. 5. Illustration of the concatenation of individual resistors in the described model for estimating the total resistance of a chip. In principal, several cavities are connected in parallel with each cavity being serially connected to several parallel nanoneedles. For simplicity, only two cavities ($n_c = 2$) with two needles each ($n_n = 2$) are shown here.

- κ is the electrical conductivity (the index e stands for the electrolyte solution),
- l is the length of the cavities or needles and
- r is the radius of the cavities or needles.

In this model, the total resistance is composed of several resistors connected in parallel and in series, representing the cavities and hollow nanoneedles (see Fig. 5). The electrolyte solution filling a cavity or needle is in turn modeled as cylindrical conductor according to equation 2:

$$R_{\text{Conductor}} = \frac{l}{\kappa \pi r^2} . \quad (2)$$

In addition, the resistance for ions entering the needles and cavities is accounted for by an access resistance term (equation 3) based on [18] and [19]:

$$R_{\text{A}} = \frac{1}{4\kappa_{\text{e}} r} . \quad (3)$$

The model described above, however, is based on the assumption that nonlinearities (e.g. capacitive effects) as well as parasitic currents across the membrane are negligible. To examine the adequacy of this presumption, chips containing only the cavities and membranes but no needles or membrane pores are analyzed. If the SiO_2 membrane and the thin Al_2O_3 layer on top of it are modeled as cylindrical conductors according to equation 2, the resistance of such a dummy chip

TABLE II
COMPARISON OF CALCULATED AND MEASURED RESISTANCES FOR DIFFERENT CHIPS WITH $n_c = 16$, $r_c = 25\,\mu\text{m}$, $l_c = 750\,\mu\text{m}$, $l_n = 2.8\,\mu\text{m}$ AND $\kappa_e = 1.39\,\frac{\text{S}}{\text{m}} \pm 0.28\,\frac{\text{S}}{\text{m}}$. EACH CHIP DESIGN WAS MEASURED FIVE SEPARATE TIMES AND THE EXACT κ_e WAS DETERMINED IN CALIBRATION MEASUREMENTS BEFORE EACH EXPERIMENT

n_n	r_n (nm)	$R_{\text{Chip,calculated}}$ (kΩ)	$R_{\text{Chip,measured}}$ (kΩ)
5	200	271	271 ± 4
9	200	128	130 ± 27
5	450	74	75.9 ± 2.8
9	450	34	35 ± 5

can be calculated using equation 4:

$$R_{\text{Dummy}} = \frac{1}{n_c \pi r_c^2} \left(\frac{l_c}{\kappa_e} + \frac{\pi r_c}{4\kappa_e} + \frac{l_{\text{SiO}_2}}{\kappa_{\text{SiO}_2}} + \frac{l_{\text{Al}_2\text{O}_3}}{\kappa_{\text{Al}_2\text{O}_3}} \right) . \quad (4)$$

In light of the results from the fluidic experiments, it is expected that filling the fluidic channels and needles with the electrolyte solution is only successful after plasma treatment. If wetting is unsuccessful, by contrast, the resistance of the respective chip can be approximated by equation 5, where A_{Chip} is the area of the chip perpendicular to the ion flow. This equation assumes that without the electrolyte solution filling the channels, the current has to pass through the material of the chip. Moreover, the resistance of the air-filled fluidic channels and needles is neglected in this estimation, as the area of the channels ($n_c \pi r_c^2$) is small compared to A_{Chip}.

$$R_{\text{Chip,untreated}} = \frac{1}{A_{\text{Chip}}} \left(\frac{l_{\text{Si}}}{\kappa_{\text{Si}}} + \frac{l_{\text{SiO}_2}}{\kappa_{\text{SiO}_2}} + \frac{l_{\text{Al}_2\text{O}_3}}{\kappa_{\text{Al}_2\text{O}_3}} \right) . \quad (5)$$

C. Comparison Between Measurements and Analytical Estimations

The calculated and measured mean resistances for four of the fabricated nanoneedle chip designs are listed in Table II and the respective current-voltage curves are shown in Fig. 6. Therein, chips with 5 and 9 nanoneedles per cavity and inner nanoneedle diameters of 400 nm and 900 nm are compared. The experimental data matches the estimations well in all four cases as the relative error between calculated and measured mean resistances is below 3 %. The error decreases with higher resistances or lower ion currents, respectively. By contrast, the relative standard deviation is lowest for the chips with 5 nanoneedles per cavity and significantly higher for the chips with 9 nanoneedles. Nonetheless, the measured current-voltage curves of all the nanoneedle chips are approximately linear. In addition, Fig. 6 includes the results for dummy chips without needles which can well be distinguished from the data of the nanoneedle chips. Similarly, the measurements of chips with different numbers and diameters of the nanoneedles can clearly be distinguished from each other as well.

Fig. 7 further shows different measurements on chips with the same geometry ($n_n = 9$ and $r_n = 200\,\text{nm}$). First, the measurements from Fig. 6 are compared to measurements and calculations of a chip without a previous plasma treatment. The effect of the plasma treatment – facilitating filling of the channels and needles with the electrolyte solution – is obvious
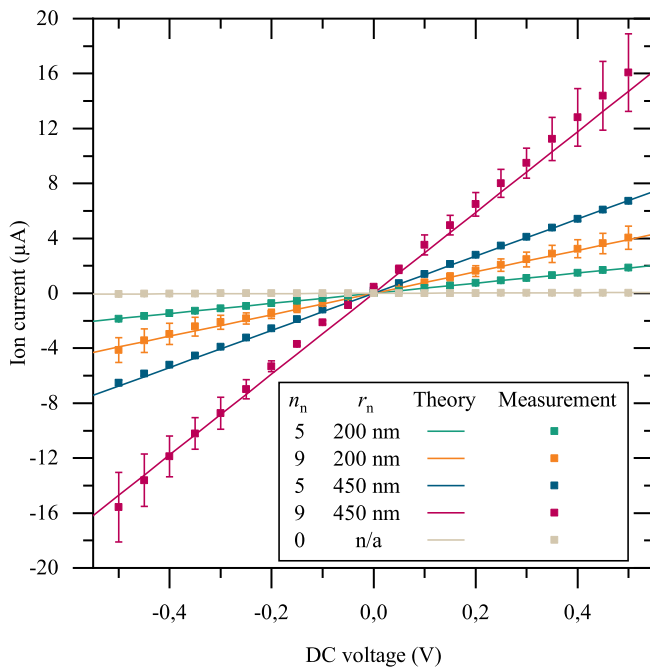
Fig. 6. Results of the electrochemical measurements compared to the respective analytical estimations for five distinct chip designs. Current-voltage curves of nanoneedle chips with different number and inner radius of the nanoneedles are shown and contrasted with corresponding graphs of dummy chips which contain no needles. The measurement data stems from five individual voltage sweeps per chip design.
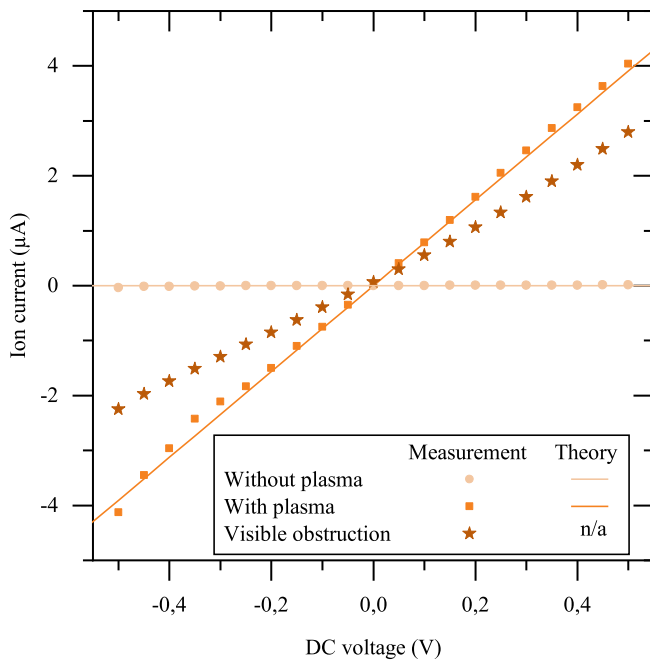

Fig. 7. Different measurements on chips with $n_n = 9$ and $r_n = 200\,nm$ and two corresponding calculated curves. Measurements on a chip that was not treated with an O_2 plasma prior to the experiments are compared to two measurement series on plasma treated chips. From the plasma treated chips, in turn, data matching the calculations well and data from measurements with a defect in the setup are shown. This defect refers to a visible obstruction of several fluidic channels on the edges of the chip.

as the graphs before and after surface hydrophilization are clearly distinguishable.

Moreover, the results from an additional experiment after plasma treatment but with defects in the measurement setup
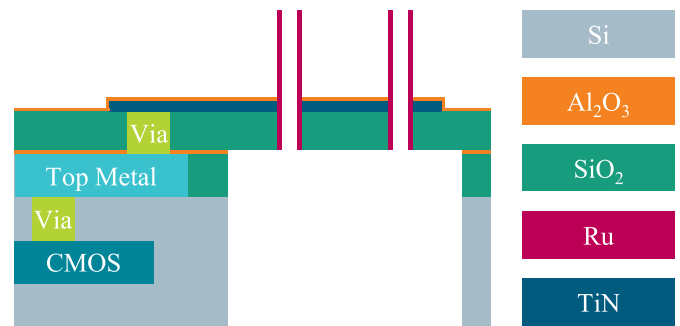

Fig. 8. Concept for combining the Ru nanoelectrodes by Allani et al. [16] with a backside fluidic connection on a CMOS substrate. All the CMOS layers need to include free space for the fluidic channels. The vias connecting the TiN base electrodes with the first metal layer are placed beside the fluidic channels instead of underneath the nanoelectrodes. The base electrodes, in turn, are located above the membrane and can thus connect the nanoelectrodes to the vias. Both the etch stopping layer and the membrane require additional structuring to accommodate the vias. Moreover, the backside DRIE for creating the fluidic channels needs to etch through the additional buried oxide and the SiO_2 passivation under the membrane before stopping on the Al_2O_3.

are shown. During this measurement series, an obstruction of several fluidic channels by the gaskets at the edges of the chip was visible. This defect is discernible in the respective graph as it varies both from the calculations and the other measurements shown. The measured resistance is clearly higher than predicted for this chip design. On the contrary, when a leak was suspected to have occurred between the two containers of the measurement setup, the measured total resistance was significantly smaller than calculated.

V. DISCUSSION AND CONCLUSION

In total, a novel fabrication method for hollow nanoneedles connected to backside fluidic channels was successfully demonstrated. Due to the specific choice of fabrication steps with a maximum process temperature of 400 °C, the process is compatible with post-CMOS processing. This enables monolithic integration of electrical functionalities into the devices and may thus open up possibilities for new applications. For instance, hollow, vertical nanoelectrodes as described by Allani et al. [16] may be integrated to allow recording of intracellular electrical signals with simultaneous delivery of substances. Fig. 8 illustrates a device that combines the two concepts.

Moreover, the exclusive use of i-line projection lithography and microsystems technology on 200 mm wafers enables high scalability of the fabrication. Geometric parameters such as number, diameter, pitch, height and wall thickness of the needles, fluidic channels and/or membranes can easily be adjusted to specific applications. The materials of the needles and membranes can be varied as well – as long as the respective etching selectivities remain. Furthermore, entire chips can be encapsulated using ALD in order to adapt the surface properties of the devices. Among others, biocompatibility, surface wettability and electrical conductivity may thus be adjusted to the respective requirements.

Improvements, however, are needed in both DRIE processes. As described before [17], the sidewalls of the backside channels show substantial bulging. Causes may be bowing,

overheating during the DRIE or a large wafer bow. The exact causes, however, are yet to be determined. The DRIE for the nanoneedle cylinders, by contrast, creates smooth but slightly conical sidewalls (see Fig. 2 (e)). The parameters of both etching processes thus need to be adjusted. Nonetheless, neither the bulging nor the conical needle sidewalls impair the principle functionality of the fabricated chips.

Another improvement may be required regarding the needle height, if the standard deviation of 140 nm between devices is not acceptable for a given application. In this case, either the good dice need to be selected at the end of the process, reducing the yield, or the homogeneity of the a-Si depositions needs to be optimized.

In addition, the resulting nanoneedle devices were evaluated regarding their fluidical functionality and electrical properties. Targeted transport of substances across the chips and through the nanoneedles was shown successfully. Each of the 16 cavities of the present chip design can individually be selected for delivery and thus 16 distinct substances can be transported to different sites at the same time. In addition, this number can flexibly be scaled up or down by either adapting the chip design (i.e. changing the lithography of the backside processing, see Fig. 1 (i)) or by adjusting the fluidic connection to the chip. By placing only one needle on each cavity, the needles can even be addressed individually which may enable single cell resolution in drug delivery applications. However, this concept – including cell penetration – needs to be evaluated on living cells in future research. Moreover, the transport of fluorescent particles was only successful after plasma treatment of the chips. This indicates that surface hydrophilization is necessary to fill the fluidic channels and nanoneedles with an aqueous solution.

Furthermore, the electrochemical measurements show good agreement with the analytical estimations. Therefore, the assumption that capacitive effects and parasitic currents across the membrane are negligible is considered appropriate. This finding is also supported by the results of measurements on the dummy chips which contain no nanoneedles and no membrane pores. The analytical model can thus be used to estimate the resistance of a given chip or, conversely, infer geometric parameters, fabrication success or blockage of the nanoneedles from corresponding measurements. For detecting the clogging of an individual needle, however, the standard deviation of the measurements needs to be reduced. This may be achieved by refining the measurement setup and especially the self-made Ag/AgCl electrodes.

Moreover, the success of wetting the fluidic channels can be examined and defects in the setup can be detected using the electrochemical measurements. The data suggest that an obstruction increases and a leak decreases the electrical resistance. Both outcomes are expected by the model. An obstruction of several fluidic channels, for instance, can be seen as a reduction of n_c. This, in turn, leads to a higher total chip resistance R_{Chip} according to equation 1. Thus, the basic concept of clogging detection using the analytical model appears to work.

However, a microscopic leak can currently only be detected after the fact, either because the size of the leak increases to a macroscopic scale or because the measurements deviate strongly from the predictions. Sorting out measurements with a suspected leak based on these criteria thus introduces bias in favor of the theoretical model. Therefore, more measurements from additional chip variations are needed for statistical validation of the presented analytical model. Furthermore, it is necessary to decrease the number of setup defects or establish a dependable method for early detection of such defects.

Nonetheless, the basic functionality of the fabrication, the fluidic connection, the electrochemical measurements and the corresponding analytical model was successfully demonstrated. These results lay the groundwork for applying the described nanoneedle devices for drug delivery, electrical recording, intracellular sensing and especially combinations of these tasks.

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