Investigation of Vapor HF Sacrificial Etching Characteristics Through Submicron Release Holes for Wafer-Level Vacuum Packaging Based on Silicon Migration Seal

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***Abstract*— Vapor hydrogen fluoride (vHF) sacrificial SiO_2 etching is a crucial process for wafer-level packaging based on silicon migration seal (SMS) technology. In this study, by using test samples with several kinds of test patterns and structures, the characteristics of vHF etching through release holes with a diameter of 0.5 μm were investigated. The results showed that through-hole etch rate had some dependence on the number and distribution of release holes, distance from the release holes, and dimension of sealed cavity, which is much different from normal vHF etching. The stiction problem in such a special case was also tested by releasing cantilever structures of different length. They were more likely to bend during through-hole etching than during normal etching. This work reveals the role of the water as both a by-product and catalyst during through-hole vHF etching. The results of this study provide important design guidelines for SMS-based MEMS packaging as well as other similar vacuum packaging technology and improve the understanding of vHF etching mechanisms. [2023-0065]**

***Index Terms*— Vapor hydrogen fluoride etching, silicon migration sealing, through-hole etching, wafer-level vacuum packaging.**

I. Introduction

HIGH-VACUUM wafer-level packaging is essential especially for resonant-type MEMS to improve the performance by reducing air damping and to reduce the fabrication cost by wafer batch process. For wafer-level packaging, there are typically two sealing methods [1], [2]; one is to use a lid wafer and the other is to deposit a sealing layer. In the former case, a high vacuum in the sealed cavity is usually achieved by using a non-evaporative getter to absorb residual gas at an elevated temperature after packaging [3], [4]. In the latter case, the residual gas is evacuated by annealing under specific conditions after [5] or before the deposition of sealing layer [6].

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Silicon migration seal (SMS) is a wafer-level vacuum encapsulation technique based on silicon migration [7]. Silicon migration refers to the phenomenon that silicon tends to deform on the surface to achieve the minimum surface energy under a high-temperature and low-pressure hydrogen environment [8]. It is possible to obtain various kinds of complex structure by utilizing silicon migration [9], [10], [11], [12]. For example, an array of holes can be transformed into a diaphragm on a cavity, which is applied to a pressure sensor [13].

SMS technique takes the advantage of this phenomenon to achieve hermitical sealing by occluding through holes. When SMS technique is applied to the wafer-level packaging of silicon-on-insulator (SOI) MEMS, a cap wafer with release hole is directly bonded with a device SOI wafer, and then the MEMS structures in the cavities are released by sacrificial layer etching through the release holes [14]. After the MEMS structure is released, the release holes are closed by silicon migration in hydrogen atmosphere at high temperature, and as a result the cavities are hermetically sealed. The release holes must be sub-microns in diameter to be occluded in a shorter time, which is preferable considering the deformation of inside MEMS structures and the fabrication cost. The remaining hydrogen inside the sealed cavity will be thermally diffused out, and consequently a high-vacuum (less than 10 Pa) environment can be achieved [15]. SMS technique requires neither the getter nor the deposition of sealing layers, simplifying the fabrication process and reducing the costs.

For this technology, vapor hydrogen fluoride (vHF) release etching via submicron-sized, deep release holes is a key process [16]. vHF etching is a commonly used method for MEMS to fabricate a free-standing structure by sacrificial SiO_2 layer etching [17]. The etching mechanism is based on the reaction of SiO_2 and anhydrous hydrogen fluoride with catalyst like water or alcohol [18]. Compared with the conventional wet chemical etching [19], gas phase etching has an advantage of being less likely to have a stiction problem [20], which refers to the adhesion of free-standing structures to an underlying substrate or each other [21].

During the release process of MEMS structures inside a cavity by vHF etching, the reactant gas and catalyst as well as etch products can only go through the release holes.

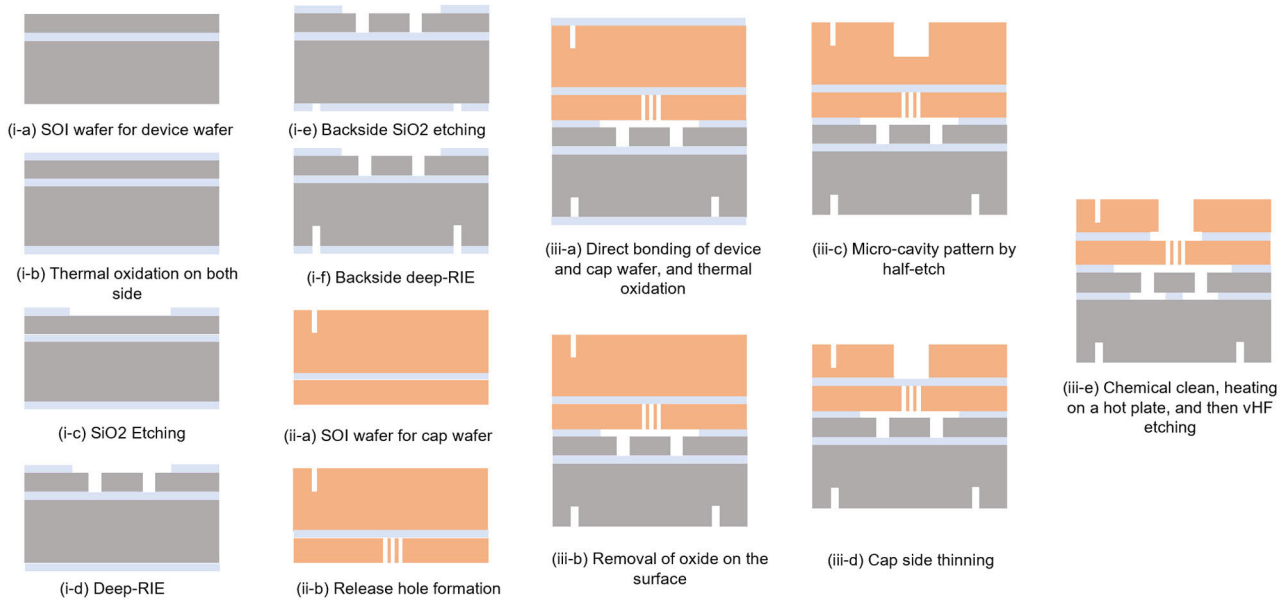

Fig. 1. Fabrication process flow of test sample [16].

The release holes are designed to be sub-microns in diameter to facilitate the subsequent sealing process, but this also leads to a reduced gas conductance. The supply of vHF and the catalyst and the removal of the etch products are limited by the release holes. In particular, water will be generated as a by-product with any type of catalyst and could be easily condensed especially in a small cavity. These factors may make the through-hole vHF etching unique from normal vHF etching. Few studies have been conducted on the vHF etching with submicron hole, with only one paper reporting that the effect of release hole size is not significant when the area is over 0.48 μm^2 [22]. Therefore, it is necessary to study the properties of vHF etching through submicron holes for a more suitable design of MEMS utilizing SMS technique.

In this paper, the properties of vHF sacrificial etching through submicron holes are reported. In this section, the background of SMS and the importance of through-hole vHF etching for SMS were described. Then, various test patterns are designed, and the test samples are fabricated. The fabrication process of test samples, the test patterns that constitute a test unit, the vHF etching equipment, and the etching recipe used in the study are described in detail. A reference group without release holes is also prepared for comparison. After vHF etching by a commercially available equipment, the results of the test samples are presented and discussed. Finally, based on the above results and discussions, the through-hole vHF etching properties are concluded.

II. Experimental

A. Sample Preparation Process

The fabrication process of the test samples used for vHF etching study follows the fabrication process of MEMS utilizing SMS technique [23]. The main difference is that MEMS structures are replaced with test patterns, which will be detailed in the following section. The fabrication process is shown in Fig. 1. As a dummy device wafer, an SOI wafer with layer thickness of 20/1/400 μm from the top is prepared (i-a) and thermally oxidized at 1100°C for 140 min to grow an oxide layer of 1 μm thickness (i-b). The buried oxide (BOX) layer of the SOI wafer is also made by thermal oxidation. Then, the oxide layer on the bonding side is partly opened for the later fabrication of the test structures (i-c), while the remaining part is used as the bonding oxide contacting the cap wafer. In the oxide-opened area, the test patterns and cavities are made by deep reactive ion etching (deep-RIE) using a photoresist mask (i-d). On the backside, dicing marks are made by SiO_2 dry etching (i-e) and deep-RIE (i-f).

For the cap wafer, a release hole pattern is firstly defined on the active layer of another SOI wafer with layer thickness of 20/1/400 μm from the top by an i-line stepper (Nikon, i14, Japan). Then, the release holes are formed by 2-step deep-RIE (ii-a) [24]. Some auxiliary marks are also made on the other side of the cap wafer (ii-b). Before wafer bonding, the two wafers are cleaned by wet chemicals including piranha solution and RCA solutions. The cleaned wafers are processed with O_2 plasma activation and mega-sonic water cleaning, and then directly bonded using a manual wafer bonder. Right after bonding, the bonded wafer is put into a furnace for thermal oxidation in order to enhance the strength of bonding (iii-a). The thermal oxidation is done at 1100°C for 140 min. The SiO_2 layer generated in the last step on the wafer surface is removed by buffered hydrogen fluoride solutions (iii-b).

Micro-cavities are formed by half etching on the cap side of bonded wafer (iii-c), and then the cap side is thinned by deep-RIE until reaching to the BOX layer (iii-d). As a result, the release hole arrays are exposed and becomes able to be penetrated in the later vHF etching. Finally, the sample is cleaned by piranha solution and RCA solutions and put on a hotplate at 180°C for 5 min to remove the moisture. At this step, the sample is ready for vHF etching test (iii-e). The test conditions are described in the following section.

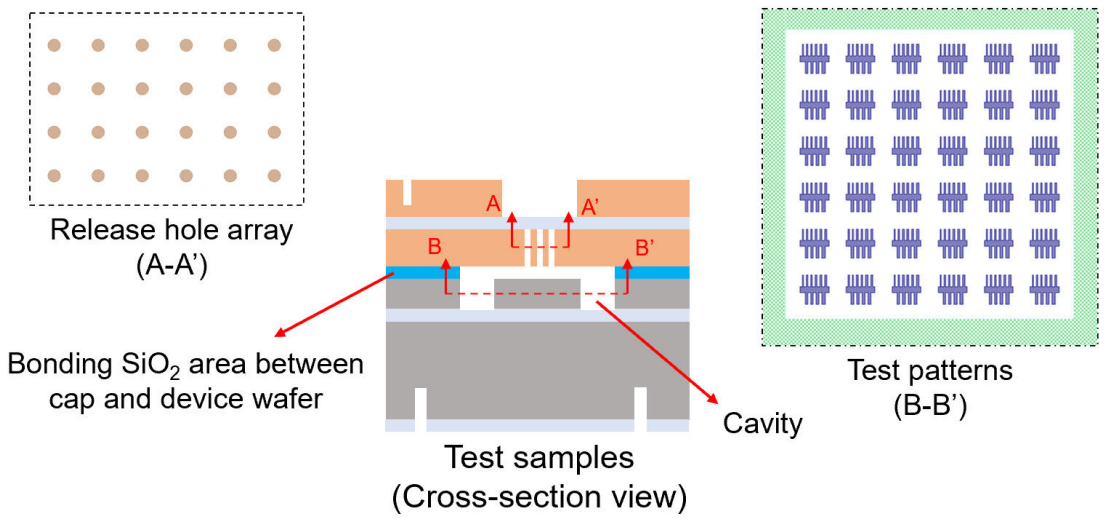

Fig. 2. Schematic figure of test sample with release holes and test patterns. The 4 × 6 release hole array is fabricated on the sealing membrane of the cap wafer. Test patterns are fabricated in the cavity of the device wafer. After the cap and the device wafer are bonded, the release holes, the test patterns and the cavity together function as a test unit that can be used to investigate vHF etching characteristics.

The device wafer with the same test patterns but without the cap wafer is also prepared as a reference group. The etching results of the reference group are used for comparison with through-hole etching results.

B. Design of Test Samples

Different test units with specific functions are included in the test sample, as shown in Fig. 2.

The characteristics to be investigated can be divided into two main categories, etch rate and stiction problem, which are directly related to the quality of structure release. The etch rate and its distribution are the most noticeable part for the fabrication. The factors which can affect the etch rate need to be studied, and they should be considered while designing the structure. Stiction of the free-standing MEMS structure to neighboring ones and the underlying surface caused by surface tension of water typically occurs when device structure is released by wet chemical method. Although vapor phase etching can overcome this problem, the condensation of by-product water in the limited space of the cavity may raise such a concern again. Therefore, it is also necessary to check about this problem.

1) Release Hole Array: The release hole array consists of some through holes inside the sealing diaphragm which is fabricated on the device layer of the cap wafer. If there is no special note, each test unit has four release hole array, and each release hole array includes 4 × 6 release holes, 24 in total. To investigate the effect of the number of release holes on the etching, some test units have one to four release hole arrays and some test units have an increased number of release holes in each array as described later.

Each release hole has a diameter of 0.5 μm as the mask dimension and a depth of 5 μm, which is fixed in this study. The diameter of the release hole needs to be submicron level to keep hydrogen annealing time for sealing within a reasonable range of a few ten minutes. On the other hand, a through hole smaller than 0.5 μm is difficult to fabricate by i-line stepper lithography and deep-RIE. After penetrating the 5 μm thick active layer, the inlet diameter is 0.51 ± 0.01 μm and the bottom diameter is 0.60 ± 0.01 μm as shown in Fig. 3.

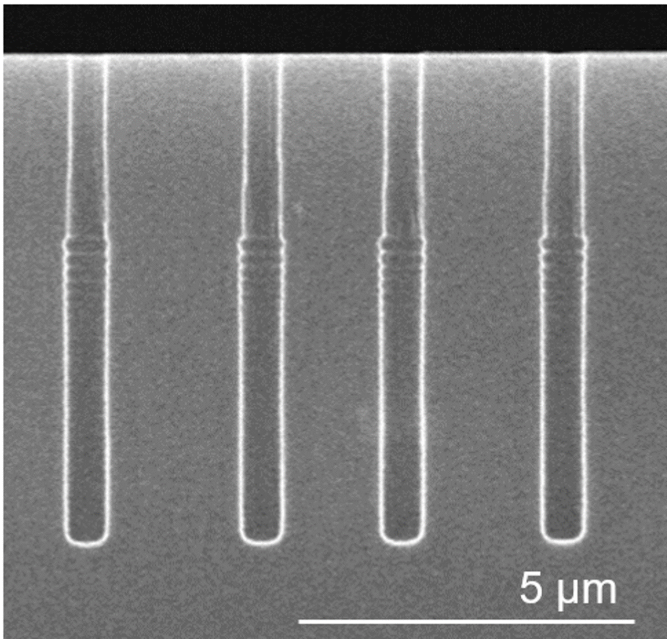

Fig. 3. Cross-section SEM image of release holes.

2) Cavity: A cavity is an independent unit which provides a space for test patterns in the device wafer (see Fig. 2). Each cavity is combined with one or more release holes array(s). After the device wafer is bonded to the cap wafer, the passageway of gases for the cavity is only the release hole array(s). Also, the cavities are supposed to be not affected by each other during vHF etching, ensuring the functions of different test units. The standard size of the cavity used in this study is 2510 μm × 2510 μm. To investigate the effect of the cavity size, cavities with enlarged size are also prepared.

3) Test Pattern: There are two kinds of test patterns, one is for etch rate test and the other is for stiction test.

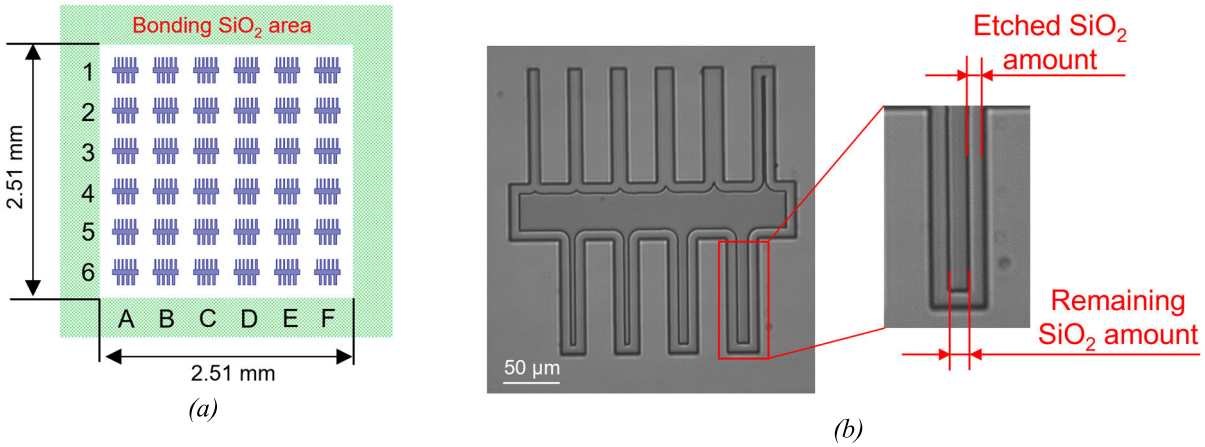

Fig. 4. Example of etch rate test patterns in cavity. (a) An example of the standard-sized cavity divided into 6 × 6 blocks with the basic pattern (b) Basic pattern after vHF etching under IR light. The etch rate is calculated based on the remaining SiO2 amount under the cantilevers.

The former test pattern is shown in Fig. 4. It consists of identical basic patterns which are the combinations of a group of short cantilevers with a fixed length of 100 μm and varying widths from 10 μm to 28 μm. The test units with a uniform distribution of basic patterns are used to evaluate the etch rate distribution in the cavity. The cavity is usually divided into many blocks, and there is one basic pattern in each block. Fig. 4 (a) shows an example of the cavity divided into 6 × 6 blocks. The etch rate in each block is represented by the etch rate of the basic pattern in that block. Fig. 4(b) shows a basic pattern after vHF etching under infrared (IR) light. By measuring the width of remaining SiO_2 beneath the cantilevers after etching, the etch rate at the position of each basic pattern can be calculated, and consequently the etch rate distribution in the cavity can be obtained. A quick check of etch rate is also possible using the cantilevers with a combination of different widths. For example, if the 10μm-wide cantilever is fully etched while the 12-μm-wide cantilever is only partially etched, it can be easily calculated that the etch amount is over 5 μm but below 6 μm, and therefore a rough etch rate can be obtained.

As for the stiction test patterns, the test units with a group of long cantilevers are used to check the stiction problem during vHF etching. As shown in Fig. 5, there are cantilevers with different widths from 10 μm to 20 μm and length from 500 μm to 2000 μm. A longer cantilever is considered to have a higher possibility to have a stiction problem.

The release hole arrays in the cap wafer are positioned directly above the test pattern in the device wafer. There is a 1 μm gap between the release hole arrays and the test pattern, which is the thickness of the thermal oxide layer. The release hole arrays are significantly smaller in size than the test patterns. During wafer bonding, there may be some misalignment between the device wafer and the cap wafer, causing the relative position of the release hole arrays and the test patterns to shift slightly. However, this shift should still be within the range of the cavity.

4) vHF Etch Tool: The vHF etch tool used in this study is Primaxx®uEtch (SPTS Technologies, UK). Ethanol is used as a catalyst, and the etching happens according to

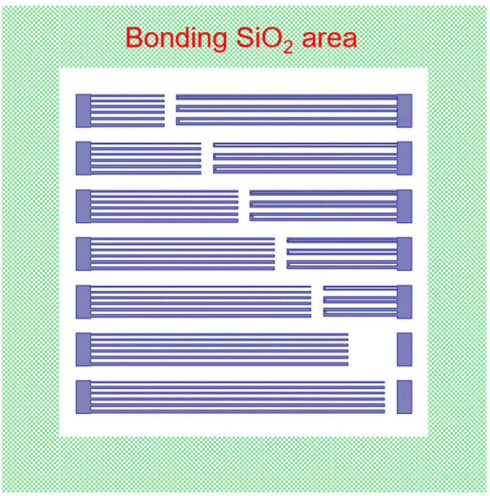

Fig. 5. Stiction test patterns.

the following reactions [25].

$$C_2H_5OH\,(g) \leftrightarrow C_2H_5OH\,(ads)$$
$$HF\ \ (g) \leftrightarrow HF\ \ (ads)$$
$$2HF\,(ads) + C_2H_5OH\,(ads) \rightarrow HF_2^-\,(ads) + C_2H_5OH_2^+\,(ads)$$
$$SiO_2\,(s) + 2HF_2^-\,(ads) + 2C_2H_5OH_2^+\,(ads) \rightarrow SiF_4\,(ads) + 2H_2O\,(ads) + 2C_2H_5OH$$

Ethanol and HF absorb to the surface, and then HF_2^- is formed by the reaction between HF and ethanol. SiO_2 is etched by reacting with HF_2^-, and the reaction products desorb from the surface. Water generated during the process accelerates the etching of SiO_2 as a catalyst according to the following reactions.

$$SiO_2 + 2H_2O \rightarrow Si(OH)_4$$
$$Si(OH)_4 + 4HF \rightarrow SiF_4 + 4H_2O$$

The vHF etching recipe used in this study is shown in Table I. For each etching cycle, the etching process is composed of

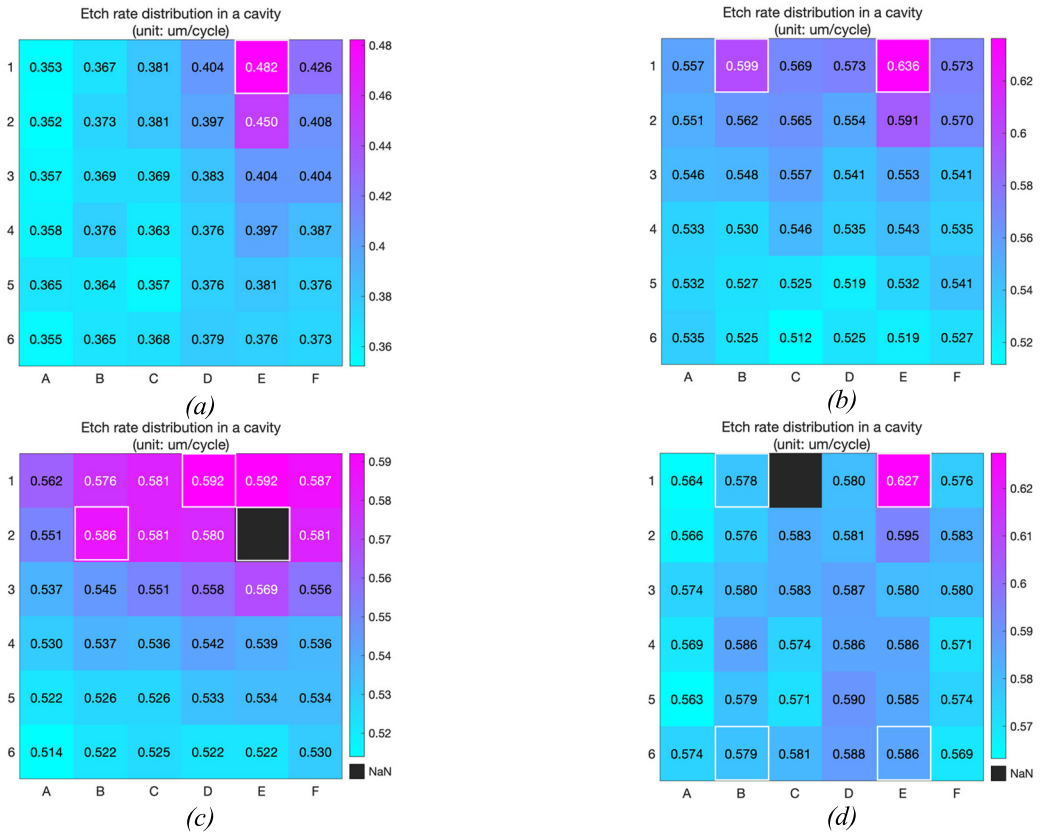

Fig. 6. Etch rate distribution in cavity with 1(a), 2(b), 3(c) and 4(d) release hole array(s) after vHF etching. Blocks surrounded by the white frame indicate the presence of a release hole array in the block. Black blocks mean that the etch rate was not successfully measured because the pattern in the block was fully covered up by the release hole array.

TABLE I
VHF ETCHING RECIPE USED IN THIS STUDY

	Time (s)	Pressure (Torr)	HF (sccm)	N_2 (sccm)	Ethanol (sccm)
Stabilization	120	50~70	0	1250	350
Etching	600	110~120	310	1250	350
Pumping	30	10~30	0	0	0

3 steps, stabilization, etching, and pumping. In the etching step, vHF and ethanol are carried by nitrogen to the etch chamber. As etching goes on, the etch rate becomes faster and the etch uniformity becomes worse as more water is produced, so the time of etching step should be well-controlled. Additionally, the partial pressure of HF is dominant factor to control the etch rate. Within a limited range, the etch rate increases by approximately two times when the concentration of partial pressure of HF is increased. The etch rate is around 0.5 μm/cycle, as our test etching showed when using a blank Si wafer with thermal dioxide.

The test samples received an etching of 20 cycles by this recipe. After the vHF etching, the etch results are observed and the etch amount are measured by an infrared microscope (IRise, MORITEX Corporation, Japan).

III. RESULTS AND DISCUSSION

A. Number of Release Hole Array and Position of Release Hole Array

In both section III-A and III-B, the etch rate distribution in each cavity is analyzed using the standard size cavity which is divided into 6 × 6 blocks by the basic patterns, as shown in Fig. 4. By combining the same patterns with different numbers of the release hole array, the dependency of etch rate on the number of the release hole arrays can be studied. Fig. 6 (a), (b), (c), and (d) show the heatmaps of etch rate distribution in the cavity with 1, 2, 3, and 4 release hole array(s), respectively. Blocks surrounded by white frames indicate the presence of a release hole array in the block. As described in section 2.3, the etch rate in each block

TABLE II
SUMMARY OF AVERAGE VALUE AND STANDARD DEVIATION OF ETCH RATE

No.	Number of release hole array	Average etch rate (Unit: μm/cycle)	Standard deviation of etch rate (Unit: μm/cycle)
1	1	0.298	0.014
2	1	0.337	0.017
3	1	0.381	0.027
4	1	0.415	0.018
5	2	0.494	0.021
6	2	0.527	0.019
7	2	0.549	0.022
8	2	0.548	0.025
9	3	0.549	0.024
10	4	0.580	0.011

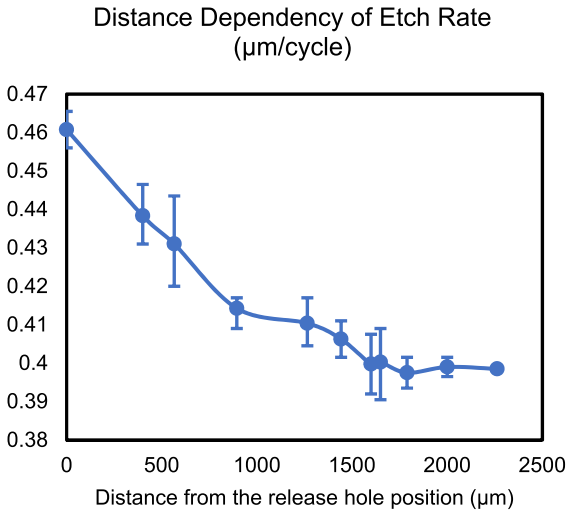

Fig. 7. Etch rate vs. distance to release hole array [16]. It is made based on the test sample with only one release hole array.

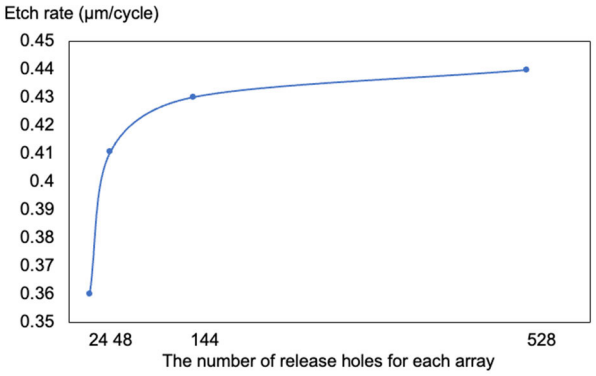

Fig. 8. Relationship between average etch rate and number of release holes for test units with only one release hole array.

is represented by the etch rate of the basic pattern in that block.

It is easy to notice that the etch rate is generally higher in the block around the release hole than in other blocks. In the test units with only one release hole array, the distance dependency of etch rate is more apparent as shown in Fig. 7. The etch rate is greatly increased as it becomes closer to the release hole, showing some dependence up to 11%/mm regarding the distance from release holes especially within the 1000 μm range. However, there is little dependence if the distance exceeds a certain value around 1500 μm, and the etch rate tends to be stable but low. During etching process, the mean free pass of the HF molecule is very close to the representative physical length scale of the release holes, which can limit the flow of HF molecules due to the small conductance of release holes. Therefore, the molecules tend to stay longer time in the areas closer to the release holes, resulting in a larger etch rate in the areas. The relation between the staying time of HF molecules and the resulting etch rate may not be linear, making etch rate looks like saturated over 1000 um as observed.

Table II is the summary of average value and standard deviation of the etch rate based on the measured data. We tested a total of ten units, including four with one release hole, four with two release holes, one with three release holes, and one with four release holes. The test units with one or two release hole array(s) were prepared as four distinct test units with the same designs. It is noted that the average etch rate increases as the number of release hole array increases and may reach saturation if the number of arrays exceeds four. The standard deviation of etch rate tends to decrease as the release hole array increases except in the cavities with only one release hole array. For the cavities with only one array, the standard deviation varies over a relatively large range, which may indicate that the etch rate distribution in this case may be unstable and susceptible to other factors. In addition, the cavity with 3 release hole arrays shows similar results to the cavity with 2 release hole arrays. This can be explained by the fact that two arrays in this cavity are so close to each other that they function like one array. The result from the cavity with well-distributed 4 arrays also indicates that uniformly distributed arrays lead to a uniform etch rate distribution.

In contrast, the test samples from the reference group with the same test patterns but without capping show a general etch rate of 0.472±0.024 μm/cycle. This value is lower than most of the data collected from the capped samples, which reveals that the sealed cavity with several release holes has the potential to accelerate vHF etching. We believe that the difference in etch rate between the capped and uncapped

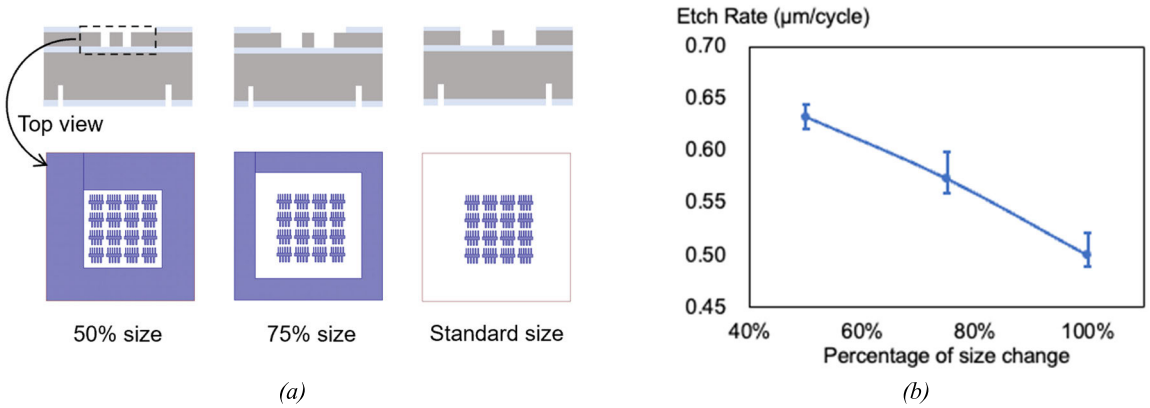

Fig. 9. (a) Variations of cavity size with same pattern. (b) Dependence of etch rate on percentage of cavity size change. The same test patterns with different sizes of sealed cavity were used. A smaller sealed area has a larger etch rate [16].

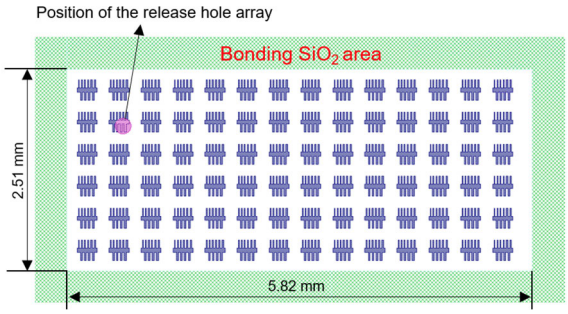

Fig. 10. Structure of larger cavity with evenly- distributed small test patterns and only one release hole array. The etch amount is almost zero after the same etching cycles as that for other test units.

samples should come from H_2O partial pressure. Limited by the conductivity of the submicron release holes, there is a higher partial pressure of H_2O (gas) generated by the reaction inside the capped cavity. Higher concentrations of H_2O (gas) near the release holes may result in higher etch rates near the release holes like a self-catalytic reaction.

B. Number of Release Holes

In this section, the number of release holes in each array is varied to investigate the effect of the number of release holes on the etch rate. Test units with only one release hole array are used, and the number of release holes is increased to 2 times, 6 times, and 22 times. As shown in Fig. 8, the etch rate increases with the number of release holes and saturates. The etch rate increases by only around 2% when the number is increased from 144 to 528. Because more release holes consumes more space and limits other functional areas, it is not a good idea to arrange too many release holes to achieve a higher etching performance. We believe that the observed saturation may be limited by the fixed etching sequence used in our recipe, which lasts for 600 seconds. If this time were increased, it is possible that the number of saturated holes could increase.

C. Cavity Size Effect

Unlike normal vHF etching, etching through submicron holes can easily cause the concentration of reactants as well as products in a small cavity. The cavity size may affect the concentration and thereby affect the etching properties. Cavity size effect was investigated by changing the size of the cavity in test units with the same test patterns. As shown in Fig. 9(a), the cavity size is set to 100%, 75%, and 50% of the standard cavity (2510 μm $\times$ 2510 μm) by adjusting the remaining outer Si area, while the test patterns (an array of the basic patterns) in the center remain the same. Fig. 9(b) shows the etch rate vs. the cavity size, which is the average value of the etch rates measured in those basic patterns. The result shows that the etch rate increases as the cavity size decreases, which is the evidence that water is concentrated more in smaller cavities during etching process and accelerates the etching. Also, we think the exposed cavity surface area should not affect the etch rate too much because the exposed oxide will be removed within several cycles, which is relatively a small number compared to 20 cycles, the total etching cycles. However, it is obviously not useful in practice to achieve a higher etch rate by reducing the cavity size because the effective space in a cavity would be greatly reduced. Due to the limitation of the etching sequence in the recipe as mentioned above, it may be necessary to optimize the recipe with time adjustments for smaller cavity sizes.

Additionally, as shown in Fig. 10, a cavity 2.3 times larger than the standard size is designed to check the etch rate. This result will be not compared with the earlier results in this section, because only one release hole array is used in this cavity and the number and distribution of the basic patterns are different. After etching cycles under the same condition, almost no etching was confirmed under the cantilever. The etch rate is so small that the buried oxide layer not covered by the patterns still exists. As a comparison, a similar design but with the standard-sized cavity in Fig. 6(a) shows an average etch rate of at least 0.3 μm/cycle. The etch rate drops to almost zero as the cavity size increases to only 2.3 times, suggesting that the etching recipe must be carefully tuned depending on the device layout.

D. Stiction Problem

As shown in Fig. 5, a series of long cantilevers with different widths and lengths were designed in the standard cavity in

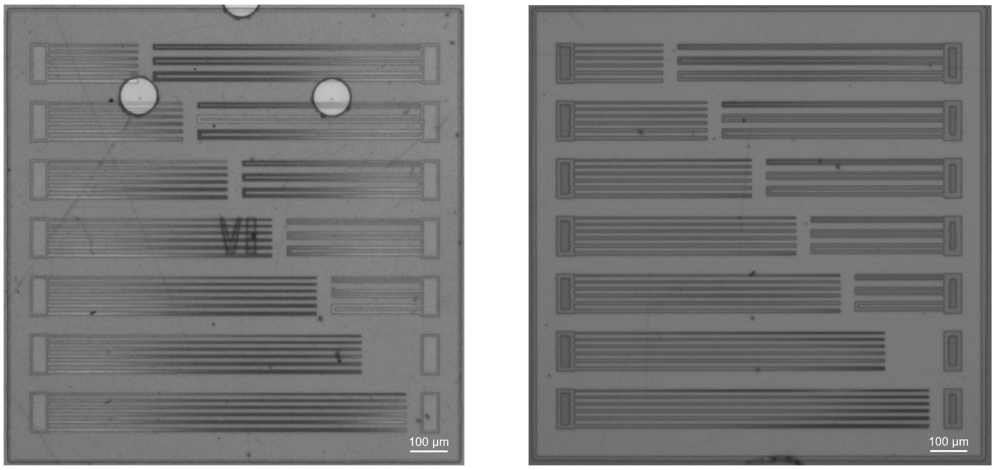

Fig. 11. Cantilevers pattern after etching. Left side is the sample processed with through -hole etching, and the right side is the reference group processed by normal vHF etching.

order to check the safe length to avoid the stiction problem. The IR images of test samples after vHF etching are shown in Fig. 11, where a capped test sample is on the left and an uncapped test sample from the reference group is on the right. Some bright and dark bands, i.e., interference fringes, can be clearly seen on the cantilevers under the IR microscope because there is a gap with varying distance between the cantilever and subsurface. These interference fringes can be used to check the bending amount of the free-standing structures [26]. The bright and dark fringes appear at the gap thicknesses given by

$$d = (n - 1/2)\lambda/2 \quad \text{and} \tag{1}$$

$$d = n\lambda/2, \tag{2}$$

respectively, where d is the gap, n is the order of fringes and λ is the wavelength of IR light, 1200 nm in this case. By calculation, in a 1 μm thick BOX layer, bright fringes may appear at 0.3 and 0.9 μm, and dark fringes may appear at 0 and 0.6 μm. Therefore, four interference fringes will appear if a cantilever has a stiction problem. In the IR images, it is found there are very few cantilevers having more than 3 fringes, which means almost no cantilever have a stiction problem in the test samples. However, compared with the result of the reference group, the cantilevers processed by through-hole etching seem to bend more because there are usually more interference fringes on them. This effect was found to increase with cantilever length. While it is difficult to conclusively determine the cause of this bending, it is worth noting that these cantilevers underwent thermal oxidation after wafer bonding, which may have contributed to the observed results.

IV. Conclusion

In this study, the characteristics of vHF etching through submicron holes are investigated by using a series of test units. In general, through-hole vHF etching showed larger etch rate than normal vHF etching when the cavity size and release hole number is enough. The etch rate exhibited a distance-dependent relationship with the release holes, with a dependence as high as 11%/mm observed for distances from the release holes, although it is not the case when the distance is over a certain value around 1500 μm. The average etch rate increases with the number of release hole array, and uniform distributed release hole arrays will lead to a uniform etch rate distribution. The number of release holes in each release hole array can also improve the etch rate, an increase in the number of release holes from 24 to 48 was found to result in an approximate 13% increase in the etch rate. But it is not recommended to design a large number of release holes because a large increase in the number can only bring about a small improvement, not to mention more release holes would consume more space. The study also revealed a relationship between cavity size and etch rate, with smaller cavities exhibiting higher etch rates. For instance, halving the size of a cavity resulted in an approximately 25% increase in the etch rate. Because the cavity size is primarily determined by the device size, the vHF etching recipe is necessary to be adjusted according to the size. As for the stiction problem, the test patterns with different long cantilevers did not show any stiction. Although the cantilevers processed with through-hole vHF etching did show a higher bending amount than the reference groups without the cap wafer, it is difficult to conclude whether this effect is attributable to through-hole etching or thermal oxidation during the fabrication process. These characteristics are meaningful for the design of MEMS using SMS process for vacuum sealing.

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