# Integration of Fault Current Limiting Function into a Single-Phase Series Compensator

A. Bahrami, R. Faranda, H. Hafezi
Department of Energy, Politecnico di Milano
Via La Masa 34, 20156, Milano, Italy
ali.bahrami@mail.polimi.it
roberto.faranda, hossein.hafezi@polimi.it

***Abstract* —Single-phase Series Compensators are very attractive electronic device for Distribution System Operator (DSO) in order to increase power quality level and load management in LV networks with reduced investment cost. One of the main important problem in LV network is due to voltage drop. The main approach to mitigate voltage drop, is employing custom power system devices as uninterruptible power supply or adapt solid-state transfer switch. Nowadays, also Dynamic Voltage Conditioners (DVC) or Dynamic Voltage Restorers (DVR) are effective apparatus and economically justified solution to compensate voltage disturbances. In contrary to the previous solutions, these devices can be efficiently used not only to solve the problem of voltage disturbance for the loads, but also to mitigate the disturbances of the upstream LV network due to a fault in the downstream by limiting the downstream fault current. Generally, there are two main strategies in order to limit downstream fault current in DVC or DVR devices: the conventional passive strategy and the innovative active one. This paper analyzes the operation principle of active solutions integrating a Fault Current Limiting (FCL) function into a DVC device, by simulation results in MATLAB environment and comparing their performance.**

***Index Terms*--Power Quality, Voltage drop, Dynamic Voltage Conditioner, Dynamic Voltage Restorer, and Fault Current Limiting.**

## I. INTRODUCTION

During last decades and together with the development of electrical energy transmission and distribution networks and by increasing the number of grid connected systems including less reliable grid connected renewable energy power plants, power quality has become a topic of great interest. Therefore several measures in order to monitor and improve the quality of power have been investigated [1]-[3]. Today power quality (PQ) is a service and many customers are paying for it, but in a simple way (in particular for continuity of service). In the near future, distribution system operators could decide or could be obliged by authorities, to supply their customers with different PQ levels and at different prices [4]. Considering several PQ surveys around the world, it is evident that short duration shallow voltage sags and long term voltage drops are by far the most prevalent power quality and reliability problems [5], [6]. The main approach toward voltage disturbances is to install a CUstom Power System (CUPS) device to suppress or counteract the disturbances [7]-[9]. The most interested CUPS device in order to mitigate voltage variation is a series-connected device used in distribution network. Injecting a voltage in series with the mains, the device counteracts voltage variations and restores the load voltage. The device capability gets to compensate any voltage variation (including voltage sag/swell, non-symmetry and harmonic distortion). The referred device in the following analysis is the Dynamic Voltage Conditioner (DVC) in [6], [7]. The single-phase DVC topology scheme is illustrated in Figure 1. where $U_s$ is the supply voltage, $U_{DVC}$ is the injected voltage by the DVC, $U_{Load}$ is load voltage and $U_{DC}$ is the DC link voltage of the DVC inverter.

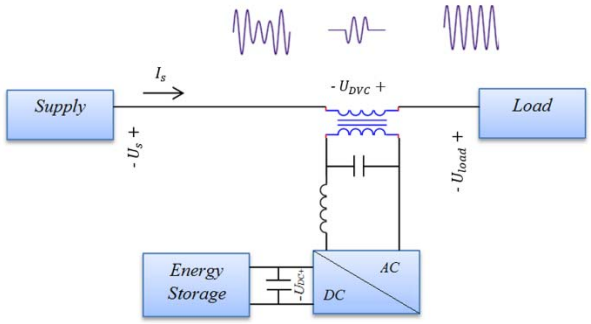


Figure 1. Scheme of a Dynamic Voltage Conditioner (DVC).

Installing a DVC would solve the problem of voltage disturbances for downstream loads. However, faults do occur on the distribution system downstream the DVC. Considering the Figure 2. the faulted point could be anywhere on the feeder connecting the DVC to the load-bus.

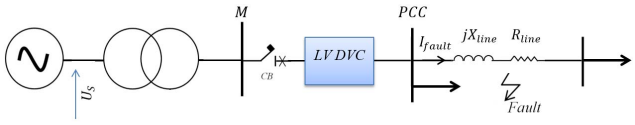


Figure 2. A configuration of radial low voltage distribution network equipped with a DVC.

978-1-5386-0517-2/18/$31.00 ©2018 IEEE

Owing to the fact that DVC is series connected to the faulted feeder, a large current will pass through the injection transformer and into the DVC converter. Generally, the main power network is designed and sized for withstanding against such short circuit transient current before the operation of the circuit breaker (CB).

Nevertheless, limiting such transient short circuit current is demanded from some points of view. In fact, without proper considerations, the high short circuit current could easily damage the injection transformer, destroy insulators and break power electronic switches which are more sensitive to high current. In order to break the fault current, one can surely trust on the CB installed upstream the DVC. However, it should be taken into account that breaking operation would take some cycles to be achieved according to protection coordination algorithm, CB type and the exact location and type of the fault incident. Still fault current during these cycles can have damaging effect on the DVC. Moreover, for the other parallel feeders connecting to the same bus in upstream substation, M bus in Figure 2. , the voltage variation event due to fault current can be harmful as it can cause equipment and loads on these feeders to fail, malfunction, or shut down. In addition, following the fault occurrence, if the DVC is not controlled properly, it might also contribute to the PCC voltage sag in the process of compensating the missing voltage, and thus it could make the fault situation more sever.

For the moment, the most likely protection scheme for series connected devices during downstream faults is based on bypassing the series device which is referred to a passive strategy in this paper and has been treated in [10]-[12] in detail.

During this study, different possible solutions to limit short circuit currents using active strategies [10], [13], [14] are treated, analyzed and compared through simulation results in MATLAB environment.

This paper is organized as following. In Section II, a short review on fault current behavior is treated. In Section III, different active strategies to integrate and control a FCL function are analyzed and compared. In Section IV simulation results in MATLAB environment are depicted and interpreted. Conclusion remarks are pointed out in Section V.

## II. SHORT CIRCUIT CURRENT

Considering several long-term PQ survey which were carried out in different countries, some interesting issues regarding voltage disturbances were revealed. For instance in PQ survey reported in [15]-[17], it is observed that voltage sags in 3-phase systems are not uniformly distributed on different phases and oftentimes there is significant accumulation of voltage sags on one phase, Figure 3. Also taking into account that some electrical consumers are more sensitive with respect to voltage disturbance rather than other consumers, they are more willing to pay for high voltage quality. In the consideration of these two mentioned issues and aiming to have a cost effective solution for voltage disturbances, DSOs would be interested in installing series voltage compensator only at single-phase configuration.


Figure 3. Distribution of voltage sags per phase in a 3-year PQ survey in Brazil [17].

Employing this concept would substitute a 3-phase DVC configuration to the usage of single-phase one. Although this configuration could eliminate the issue of voltage disturbances on a target phase, it may not compensate all types of voltage disturbances for 3-phase loads. However, the general outcome for the system is diminishing the consequences of voltage disturbances. Considering the mentioned economic benefit this study is focused on the single-phase DVC configuration. Nevertheless, the conclusions could be extended to 3-phase systems without the loss of generality.

In order to describe the fault situation, which is supposed to be handled during this survey, it is assume that the DVC in Figure 2. is bypassed. If the supply voltage is equal to $u_s(t) = \sqrt{2}U_s \sin(\omega t)$, the short circuit current due to fault at any point downstream of the M-bus can be calculated using the following equation:

$$i_{fault}(t) = \frac{\sqrt{2}U_s}{|\underline{Z}_f|}\sin(\omega t - \angle \underline{Z}_f) + I'' e^{-\frac{\omega(t-t_{fault})}{\omega\tau}} \qquad (1)$$

where $\underline{Z}_f$ is the total impedance between the supply and the fault location, $t_{fault}$ is the fault moment and $\tau$ is the time constant in the faulted network which defines the rate of decay of DC current component. The value of integration constant $I''$ depends on the fault location and the fault moment. The simulation results in MATLAB environment for maximum and minimum short circuit current in the network of Figure 2. with the parameters given in TABLE I. are illustrated in the Figure 4. Due to the network requirement of being robust enough against the inrush current of big motors, the instantaneous breaking unit of upstream CB is generally set on a value between 6-10 times the rated current.

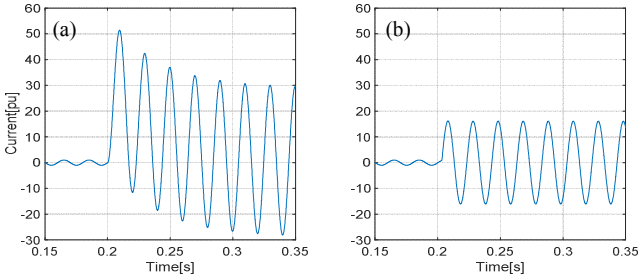


Figure 4. Single-phase short circuit current (a) maximum and (b) minimum when the single-phase DVC is by-passed.

## III. ACTIVE FCL STRATEGIES

Usually a DVC has to be equipped with a bypass device in order to avoid over voltage on the DC bus during short circuit current events. So considering these events, a common solution for protecting a DVC during a downstream fault, is enabling a bypass circuit as shown in Figure 5. Moreover, the fault current should be kept above a certain value to be detected and cleared by instantaneous tripping unit of the upstream CB. Therefore, bypassing the DVR protects it as well as avoids interfering with existing protection coordination.

However, it has to be noted that this bypass solution can only protect the DVC during a downstream fault and any upstream bus voltage drop compensation cannot be reached because a large fault current can flow into the feeder.

Therefore, in addition to protecting the DVC against high currents, limiting short circuit current is demanded in terms of avoiding voltage sag for upstream/parallel devices. For this purpose, different passive configurations can be considered.

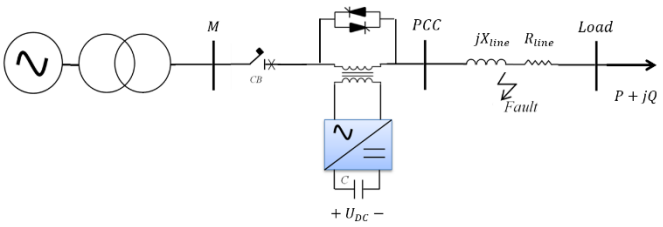


Figure 5. DVC equipped with bypass static switches.

Even though passive elements could yield considerable current limiting performance, avoiding interfering with upstream protection devices, makes these strategies less effective owing to the fact that a large current should be allowed to flow in the faulted line.

The cutting edge in FCL scenario is based on controlling the DVC actively to inject an appropriate voltage into a faulted feeder for limiting short circuit current to the rated line current, therefore the voltage of upstream bus cloud be restored to the rated value too. Active FCL strategies could be implemented in impedance and reactance modes, which are explained and analyzed in the following. The reliability, robustness and the speed response are the main evaluation criteria to compare these different strategies.

Since the most voltage sags are in the range of 60% reduction in magnitude according to different voltage surveys around the world [3], DVC sizing should be as low as possible due to economic reasons. However, active control of DVC during a downstream fault has the disadvantage of requirement for higher voltage injection capability comparing to the passive FCL schemes and leads to oversize the DVC with respect to its primary duty as a voltage compensator.

A possible active strategy could be to limit the short circuit current in the faulted feeder around 1pu, therefore in order not to interfere with protection coordination of upstream CBs it requires to implement a communication channel between the DVC and upstream protection equipment. As soon as the DVC goes to FCL mode, it is supposed to inform the upstream CB, so the instantaneous current breaking is still achievable. The most sever fault incident is a solid one, which occurs immediately after the DVC, so according to (2), in active FCL strategies, the DVC should be sized for the rated power of downstream load:

$$S_{DVR} = V_{rated} \cdot I_{rated} \tag{2}$$

To reach this result three different method are considered.

### A. First method - Active impedance FCL mode

If a fault occurs at the distribution feeder downstream the DVC, in order to limit the short circuit current through series voltage injection, the injected voltage phasor of the DVC is minimized by orientating $U_{DVC}$ to be in phase with feeder voltage drop ($V_{PCC}$). This implies that for minimal voltage injection, the DVC would act as an active impedance $Z_0$ whose $R/X$ ratio is the same as feeder impedance to the faulted point [13]. This issue also can be concluded from phasor representation of Figure 6. where $\underline{U}_S$ is the voltage phasor of the supply, $\underline{V}_{M,pre-fault}$ and $\underline{I}_{pre-fault}$ are respectively voltage phasor at M-bus (DVC supply side) and the line current phasor before the fault, $\underline{V}_{PCC}$ and $\underline{I}_{fault}$ are respectively the voltage phasor at PCC-bus (DVC load side) and line current phasors after fault occurrence.

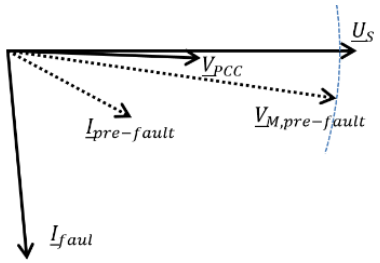


Figure 6. Phasor representation of fault condition assuming $U_{DVC} = 0$.

Even though minimal voltage injection could be an interesting approach, restoring the upstream bus voltage both in terms of amplitude and phase angle is more interested in particular when the other loads in the parallel feeders are not equipped with a DVC while they are sensitive with respect to phase jump. For this purpose, the DVC is supposed to inject a suitable series voltage in such a way that the voltage phasor of the upstream bus is restored to the same pre-fault value.

Therefore, the reference value of DVC voltage can be calculated using:

$$\underline{U}_{DVC,ref} = \underline{V}_{M,pre-fault} - \underline{Z}_f \cdot \underline{I}_f \tag{3}$$

where $\underline{Z}_f$ is equal to total feeder impedance to the faulted point. Since the fault location is unknown, its value would be unknown too but measuring the load side voltage of the DVC gives the online value of the voltage drop across the feeder:

$$\underline{V}_{PCC} = \underline{Z}_f \cdot \underline{I}_f \tag{4}$$

So according to the (5), the reference value of DVC voltage can be constructed within the control system:

$$\underline{U}_{DVC,ref} = \underline{V}_{M,pre-fault} - \underline{V}_{PCC} \quad (5)$$

Constructed $\underline{U}_{DVC,ref}$ is applied to the DVC control system depicted in Figure 7.

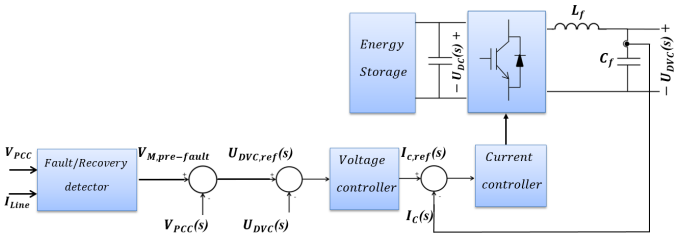


Figure 7. DVC control scheme, active impedance FCL mode.

Fast fault detection is carried out by sensing the rate of change of current and comparing it with a pre-set value. In order to avoid noise effects, a low pass filter is introduced to the measured data [12]. Recovery from the downstream fault is detected by measuring the voltage at load side of the DVC injection transformer (PCC-bus). As soon as the fault is cleared, this voltage will increase. Once $V_{PCC}$ is restored to a preset threshold level $V_{th}$, the FCL function of DVC can be terminated. Ensuring DVC FCL mode is not turned off by any measurement noises, a low pass filter is introduced to this measurement signal too which is equivalent to a delay in time domain. Therefore, the DVC FCL mode will be terminated if the condition of $V_{PCC} \geq V_{th}$ lasts for a specific time and no other downstream fault is detected during this interval.

According to (6) the voltage rate of change at DVC output can be controlled through regulating the current in filter capacitor.

$$\frac{du_{DVC}(t)}{dt} = \frac{1}{C_f} \times i_{C_f}(t) \quad (6)$$

Controlling this current properly, $u_{DVC}(t)$ can be controlled during transient interval [13]. So in addition to the outer voltage control loop, the inner current control loop is implemented to control the filter capacitance current.

The main drawback of this strategy is voltage increase in DC link during FCL mode. In fact, the resistive part of active impedance absorbs power from the grid. Considering the M-bus voltage restored to pre-fault value and the line current as well, the absorbed power approximately equals to the power delivered to the protected load before the fault event. This power is delivered to DC link and causes considerable voltage increment. Therefore, this strategy requires to break the short circuit current as fast as possible by the upstream CB which means that the reliability of communication channel between the DVC and CB as well as compatibility of the protection coordination with voltage limitation of the DVC energy storage device is extremely demanded to avoid damaging the system.

### B. *Second method - Step active reactance FCL mode*

Controlling the DVC as active inductor could ensure zero real power absorption during FCL mode thus avoids DC link voltage increase. When the phase angle restoration of upstream bus voltage is not critically demanded, following a downstream fault, this strategy seems more interesting. For this purpose a constant active reactance injection of $X_0$ using flux-charge control scheme has been treated in [14]. Considering strong limitation imposed on the fault current, AC current component is limited effectively while due to high value of ratio $X/R$, DC current component decays slowly. Consequently, the first current zero crossing is postponed which puts stress on upstream devices due to high value of let-through energy $I^2t$.

### C. *Third method - Smooth active reactance FCL mode*

Solving the mentioned issue regarding step injecting active reactance, it is possible to employ a smooth voltage injection strategy into the faulted feeder. For this purpose, a voltage-current control scheme depicted in Figure 8. has been developed.

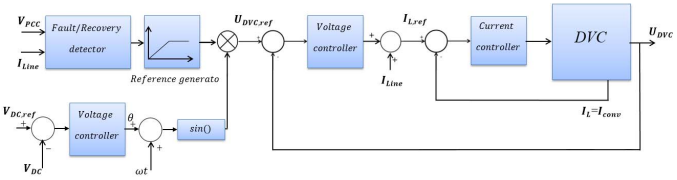


Figure 8. DVC control scheme, smooth active reactance FCL mode.

The operation principle of reference generator in control system of Figure 8. is this: the magnitude of $\underline{U}_{DVC,ref}$ is constructed using a current comparator, which compares the amplitude of rated line current with the online value. It increases $|\underline{U}_{DVC,ref}|$ until line current is limited to 1pu. In order to have pure inductance, the phase angle of $\underline{U}_{DVC,ref}$ should be constructed by:

$$\angle \underline{U}_{DVC,ref} = \angle \underline{I}_{line} + \pi/2 \quad (7)$$

where $\angle \underline{I}_{line}$ is the phase angle of line current and can be calculated employing a PLL. But as a result of switching losses and also losses in $L_f$, the DC link voltage drops during pure active inductance injection. In order to keep the DC link voltage constant, it is required to provide the phase angle $\angle \underline{U}_{DVC,ref}$ through a DC link voltage controller, consequently the DC link voltage is kept almost constant. Then constructed $\underline{U}_{DVC,ref}$ is applied to the DVC voltage controller. As depicted in Figure 8. where the outer loop controls the voltage and the inner loop controls the converter current. In order to have better control performance, the line current is added to the output of voltage controller. It reduces the duty of voltage controller.

## IV. Simulation Results

In order to validate the addressed control theories and compare the FCL performance of treated strategies, the simulation results of each strategy in MATLAB environment

for the radial low voltage distribution network of Figure 2. with the parameters given in TABLE I. are presented in this section.

Regarding the fault incident, the most sever fault in terms of short circuit current magnitude is a solid fault occurs immediately after the DVC and at the time instance, which results in the highest possible DC current component. For this purpose, a solid fault at moment of 0.2s is applied at PCC-bus. In order to observe the behavior of the network during FCL mode, it is assumed that there is no breaking operation of upstream CB before 0.35s.

TABLE I. NETWORK PARAMETERS

| Parameters | Values |
|---|---|
| Distribution supply voltage | 20kV |
| Distribution transformer ratio | 20kV/230V |
| $Z_{sc}$ Distribution transformer | 4% |
| Injection transformer ratio | 230V/230V |
| $Z_{sc}$ Injection transformer | 4% |
| Load | 50kVA, PF=0.85 |
| DC link voltage | 500V |
| DVC energy storage | 75mF |
| Filter capacitor | 0.1mF |
| Switching inductance | 0.5mH |
| Inverter switching frequency | 20kHz |

Using the first described method (active impedance FCL mode) to limit the short circuit current the simulation results for line current, upstream bus voltage (M-bus), DVC output voltage and DC link voltage are depicted in the Figure 9. and Figure 10.

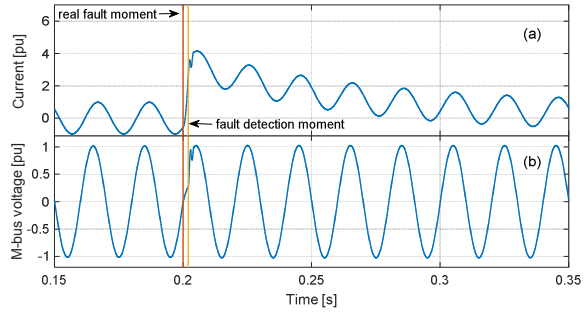


Figure 9. (a) Line current and (b) M-bus voltage waveforms using active impedance FCL mode

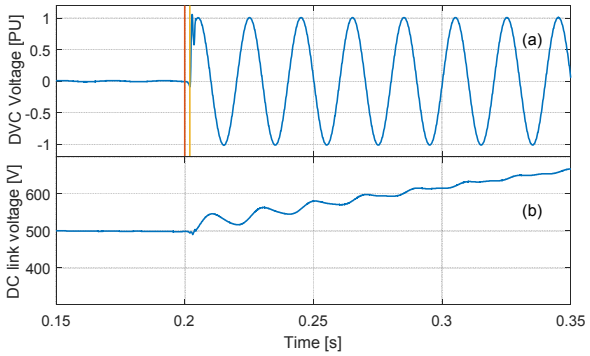


Figure 10. (a) DVC output voltage and (b) DC link voltage waveforms using active impedance FCL mode

As it is shown, the peak of line fault current is limited to 4pu and it decades to 1pu within about 5 cycles. The M-bus voltage is uninfluenced both in terms of magnitude and phase angle thanks to the FCL function of DVC inverter. Due to resistive part of active impedance, a considerable voltage increase in DC link is observed which requires to consider appropriate measure to avoid damaging effect on DVC energy storage (as dissipative solutions). Even if the voltage increasing is not so fast considering the breaker response time.

Using the second method (active reactance FCL mode) here described, the simulation results for the step injection of active reactance are depicted in Figure 11. and Figure 12.

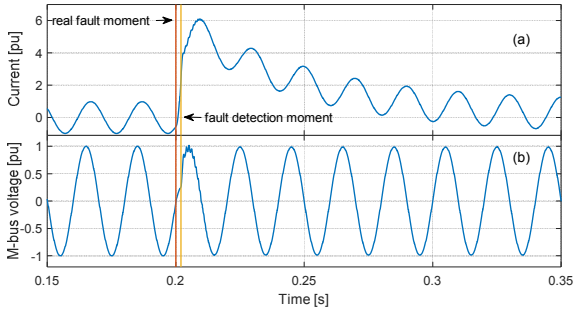


Figure 11. (a) Line current and (b) M-bus voltage waveforms using step injection of active reactance

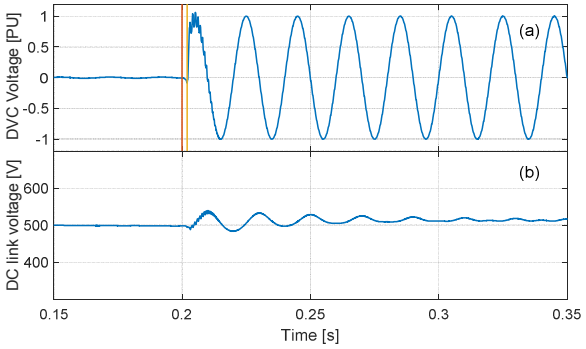


Figure 12. (a) DVC output voltage and (b) DC link voltage waveforms using step injection of active reactance

As it can be seen in Figure 11. the peak of line fault current is limited to 6pu in this case and again it takes about 5 cycles to reach 1pu. The AC component of short current is effectively limited; however, due to slow decaying DC component the first zero crossing of current waveform takes place in the 5$^{th}$ cycle which increases value of let-through energy for upstream devices.

M-bus voltage is restored to the nominal value, and as it can be noticed from Figure 12. (b), DC bus voltage is regulated effectively around the set value (500V).

Using the third described method (smooth active reactance FCL mode) the simulation results are depicted in Figure 13. and Figure 14.

As it can be seen in Figure 13. the peak of line fault current is limited to 15pu in this case and comparing to first and second method it sees higher peak value. Indeed, it takes about 2-3

cycles to reach 1pu. Both AC and decaying DC component of short current is effectively limited and the first zero crossing of current waveform takes place sooner which decreases value of let-through energy for upstream devices respect to step injection of active reactance strategy. M-bus voltage is restored to the nominal value, but it sees a small voltage sag for about two cycles. It can be noticed from Figure 14. (b), DC bus voltage is regulated effectively around the set value (500V).

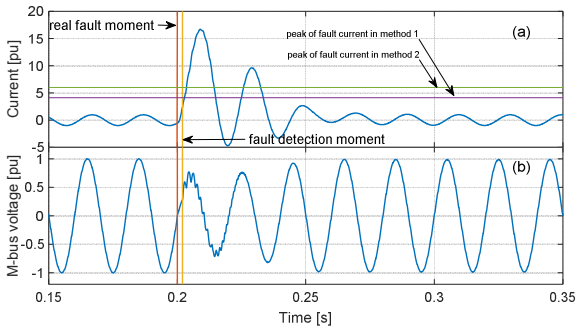


Figure 13. (a) Line current and (b) M-bus voltage waveforms using smooth injection of active reactance

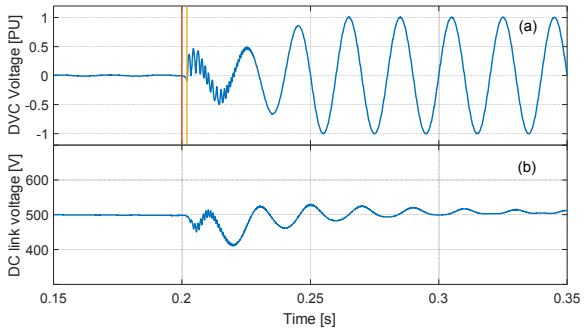


Figure 14. (a) DVC output voltage and (b) DC link voltage waveforms using smooth injection of active reactance

Comparing the short circuit current waveforms in step and smooth injection of active reactance, one may conclude that the step injection limits effectively the AC current component but slow decaying DC current component postpones the first zero crossing. While using the smooth voltage injection at cost of more sever transient in terms of current magnitude, the CB has the chance to break the current after 1-2 cycles.

## V. CONCLUSIONS

Integrating active FCL function into a DVC is possible through active impedance and reactance strategies. The active impedance FCL mode gives the benefit of complete restoration of upstream bus voltage both in terms of magnitude and phase angle while it suffers from DC link voltage increment during FCL mode; therefore, it may results in oversizing DVC energy storage system or employing a dissipative solution to avoid violating DC link voltage limitation. The active reactance FCL mode ensures a constant DC link voltage during FCL mode and could be achieved using a variable voltage injection strategy. Implementing this strategy and considering the simulation outcomes, a trade-off between the transient peak of short circuit current and the value of $I^2t$ can be seen. Based on network requirements one can optimize the rate of DVC voltage injection during FCL mode.

## REFERENCES


[1] L. Tenti, R. Chiumeo, C. Gandolfi, L. Garbero, F. Malegori, and M. Volta, "The origin of voltage dips monitored in MV network and its effect on the evaluation of MV voltage dips performances indices," in 22nd International Conference and Exhibition on Electricity Distribution, CIRED 2013, Stockholm, Sweden.

[2] A. Bracale, G. Carpinelli, P. Caramia, P. Verde, R. Chiumeo, and F. Tarsia, "System voltage quality regulation for continuous disturbances," in IEEE PES General Meeting, PES 2010, Minneapolis, MN, United States.

[3] R. Chiumeo, M. D. Nigris, C. Gandolfi, L. Garbero, and L. Tenti, "Voltage dips performance characterization by PQ indices at national and macro area level," in 14th International Conference on Harmonics and Quality of Power, ICHQP 2010, Bergamo, Italy.

[4] Morris Brenna, Roberto Faranda, and Enrico Tironi, "A New Proposal for Power Quality and Custom Power Improvement: Open UPQC," IEEE Transactions on Power Delivery, Vol. 24, No. 4, October 2009.

[5] H. Hafezi, G. D'Antona, A. Dedè, D. D. Giustina, R. Faranda, and G. Massa, "Power Quality Conditioning in LV Distribution Networks: Results by Field Demonstration," *IEEE Transactions on Smart Grid* vol. 8, no. 1, pp. 418-427, Jan. 2017.

[6] H. Hafezi, and R. Faranda, "Dynamic Voltage Conditioner, a New Concept for Smart Low-Voltage Distribution System" *IEEE Transactions on Power Electronics,* vol. 33, no. 9, DOI: 10.1109/TPEL.2017.2772845.

[7] H. Hafezi, R. Faranda and M. C. Falvo, "Single-Phase Dynamic Voltage Conditioner Control under Load Variation," Harmonics and Quality of Power (ICHQP), 2016 17th International Conference.

[8] F. Belloni, R. Chiumeo, C. Gandolfi, and A. Villa, "Performance test of a PQ universal compensator through Control Hardware in the Loop simulation," in 6th International Conference on Clean Electrical Power, ICCEP 2017, Santa Margherita Ligure, Italy pp. 502-508.

[9] G. D'Antona, D. Della Giustina, R. Faranda, and H. Hafezi, "Open UPQC Power Quality Manager within Distributed Generation Systems," in Diagnostics for Electrical Machines, Power Electronics and Drives (SDEMPED), 2015 IEEE 10th International Symposium on, Guarda, Portugal, pp. 501 - 507.

[10] A. Bahrami, "An integrated control scheme for dynamic voltage restorer to limit downstream fault currents," M.Sc. dissertation, Dept. of Energy, Politecnico di Milano, 2017.

[11] M. Farhadi-Kangarlu, E. Babaei, F. Blaabjerg, "A comprehensive review of dynamic voltage restorers," *Electrical Power and Energy Systems*, 92 (2017) 136–155.

[12] Zhikang Shuai, Peng Yao, Z. J. Shen, Chunming Tu, Fei Jiang, and Ying Cheng, "Design Considerations of a Fault Current Limiting Dynamic Voltage Restorer (FCL-DVR)," *IEEE Transactions on Smart Grid*, Vol. 6, No. 1, January 2015.

[13] S. S. Choi, Member, T. X. Wang, and D. Mahinda Vilathgamuwa, "A Series Compensator with Fault Current Limiting Function," *IEEE Transactions on Power Delivery*, Vol. 20, No. 3, July 2005.

[14] Yun Wei Li, Member, D. Mahinda Vilathgamuwa, Poh Chiang Loh, and Frede Blaabjerg, "A Dual-Functional Medium Voltage Level DVR to Limit Downstream Fault Currents," *IEEE Transactions on Power Electronics*, Vol. 22, No. 4, July 2007.

[15] D.S. Dorr. "Point of Utilization Power Quality Study Results" *IEEE Transactions on Industry Application*, Vol. 31, No. 4, pp. 658 - 666, 1995.

[16] J.J. Stanislawski "National Power Laboratory Power Quality Study 1972 to 1979 Revisited" 17th International Telecommunications Energy Conference INTELEC'95, pp. 544 - 551, 1995.

[17] Igor Amariz Pires, Filipe Dias de Oliveira, Sidelmo Magalhaes Silva, and Braz de Jesus Cardoso Filho, "On the Application of Single-Phase Voltage Sag Compensators in Three-Phase Systems" *IEEE Transactions on Industry Applications*, Vol. 53, January/February 2017