Design of Controller Using Reduced Order Modeling for LED Driver Circuit

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***Abstract*—This paper proposes a new control design strategy for Single-Ended Primary Inductor Converter (SEPIC) fed Light Emitting Diode (LED) driver circuit. The concept of model order reduction has been employed to design a proportional integral derivative (PID) controller for the SEPIC converter. In order to achieve reduced order model of the higher order SEPIC converter, operated in continuous conduction mode, cuckoo search algorithm along with Pade approximation has been utilized. Further, the unknown parameters of PID controller for reduced order model are obtained by minimizing integral square error (ISE) using cuckoo search (CS) algorithm. It was observed that the obtained results are comparable with well-known techniques and recently published work. It is revealed that the PID controller designed for reduced order model also exhibit improved performance as compared to the SEPIC converter with compensator.**

***Index Terms*—Model Order Reduction, SEPIC Converter, LED Driver Circuit, Cuckoo Search Algorithm**

I. Introduction

LED (Light Emitting Diode) lighting technology has revolutionized the global lighting industry, and this technology has exceeded in terms of lifetime, color quality, reliability, flexibility, and energy efficiency as compared to all the previous lighting technologies [1]. There has been a continuous innovation in the LED lighting industry during the last decade, and researchers and manufacturers are still working to make it more sustainable in a longer term. The driver circuit is the heart of the LED lamp which is responsible for providing dc voltage to the LEDs. The driver circuit includes a rectifier and a dc-dc converter as shown in Fig. 1. A bridge rectifier converts the ac supply to dc supply, and the dc-dc converter is accountable to convert the one level of voltage to another. There is a range of converters such as Buck, Boost, Buck-Boost, Cuk, SEPIC and Zeta which are being frequently used in the LED driver circuit [2]. The efficient and reliable operation of the converter helps the LED lamps to be reliable, efficient and free with any power quality related issues. There is a number of methods have been existing for modeling of the dc-dc converters such as signal flow graph (SFG) [3], and state-space averaging (SSA) technique [4], [5] but, the modeling complexity is the key issue with such methods. To solve such problems most efficiently and with a fast-dynamic response PID controllers have been used commonly, and nowadays, a range of techniques are available to design these controllers for various converters [6], [7]. Recently, evolutionary algorithms have been extensively used in numerous fields to design controllers for different purposes [8]-[10].

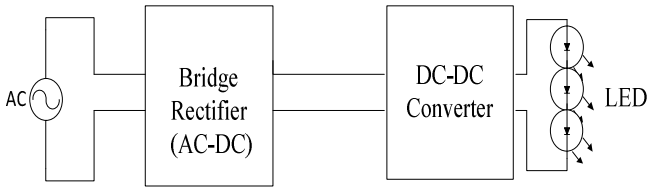

Fig1. Basic configuration of LED driver circuit

This study contributes a new controller design technique for SEPIC converter fed energy efficient LED driver circuit. The controller is designed for SEPIC converter via reduced-order modeling. A new mixed method is being proposed to obtain reduced order model of SEPIC converter. Furthermore, the unknown parameters of the PID controller are achieved by employing cuckoo search algorithm. The obtained results are compared with recently published work in term of integral square error, and it was observed that the offered controller shows the better performance.

The remainder of this paper is organized as follows: Section II discusses the SEPIC Converter and PID controller briefly. The proposed methodology has been discussed in section III. Section IV contains the results and discussion of the proposed work whereas, the paper has been concluded in section V.

II. SEPIC Converter

SEPIC is a category of dc-dc converter that gives the output voltage higher, equal or lower than the input voltage. It is essentially a boost converter followed by a buck-boost converter. This converter has an advantage of having non-inverted output and can be operated in discontinuous or continuous conduction mode. Fig.2 shows a basic circuit of the SEPIC converter which includes two inductors, two capacitors, resistors in series with the inductors and capacitors, MOSFET as a switch and a diode. Inductors and capacitors in the converter play a role to convert one level of voltage to another

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level. A SEPIC converter operates in continuous conduction mode if the current through the inductor L_1 never falls to zero. However, if the current through the inductor L_1 is allowed to decrease to the zero value, it is said to be operated in discontinuous conduction mode. For an ideal SEPIC converter, the relationship between input voltage and the output voltage is given by:

$$\frac{V_o}{V_d} = \frac{d}{1-d} \tag{1}$$

where d is the duty cycle of the switch.

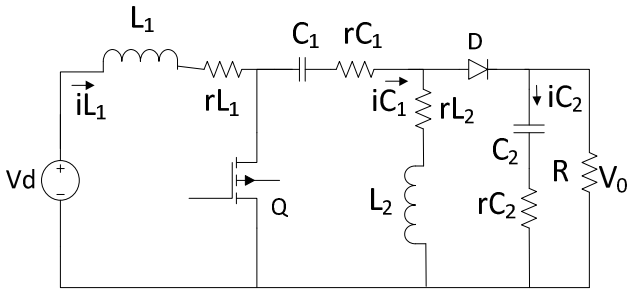

Fig2. Schematic diagram of SEPIC converter

The PID controller arrangement for the SEPIC converter is represented as:

$$G_{PID}(s) = k_p + \frac{k_i}{s} + k_d s \tag{2}$$

where, k_p, k_i and k_d are proportional, integral and derivative gains of the PID controller. The objective of this study is to achieve optimal values of these three gains.

III. PROPOSED METHODOLOGY

Some species of cuckoo birds, such as, 'Ani' and 'Guira', often lay their eggs in communal nests and generally throw others eggs to increase the hatching probability of their own eggs. The cuckoo search (CS) algorithm, population-based optimization technique, is inspired by this breading behaviour of cuckoo birds. Normally, this brood parasitic behaviour of cuckoo birds combines with the L´evy flight behaviour of fruit flies to enhance search capability of CS algorithm [11]. In order to simplify the optimization problem, CS algorithm uses following three rules[11], [12]

(a) It is assumed that the cuckoo lays one egg once only and keeps it safely in the communal nest.
(b) The nest, consisting high-quality eggs, is considered as the best nests to carry forward for the next generation.
(c) Eggs, lay by cuckoo bird, are discovered from fixed host nests with a probability pa ∈ [0, 1].

Further, the general system-equation, used in optimization, is given as: [11]-[14].

$$Y_i^{(t+1)} = Y_i^{(t)} + a \otimes Lévy(\lambda) \tag{3}$$

where a (a > 0) is a step size which is related to the level of the problems which is to be optimized, ⊗ indicates entry-wise multiplications, and 't' represents the number of the current generation. L´evy flight is described as random walk trajectories which are composed of self-similar jumps and given as [11], [12]:

$$\text{Lévy} \sim u = t^{-\lambda} \quad ; (1 < \lambda \leq 3) \tag{4}$$

here, λ represents L´evy distribution parameter[11], [12], [15]. In this study, pulse width modulation technique has been utilized through PID controller to improve the step response of the SEPIC converter. Fig. 3 shows the structure of the offered methodology for designing the controller for SEPIC converter. The unknown tuning parameters of PID controller are evaluated using CS algorithm.
The integral square error (ISE) between reference voltage, $V_{ref}(t)$ and output $V_O(t)$ is calculated as follows.

$$ISE(Z) = \int_0^\infty ((V_{ref}(t) - V_O(t))^2 \, dt \tag{5}$$

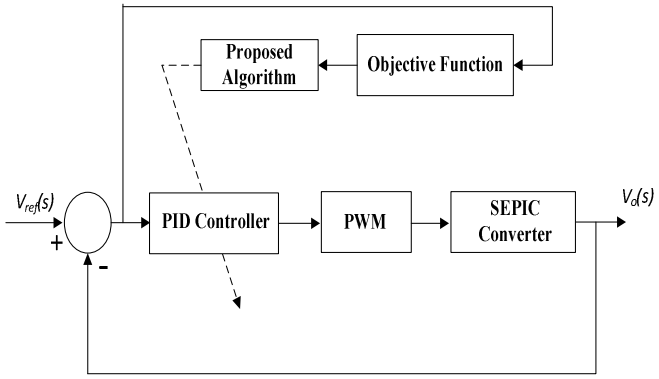

Fig3. Proposed methodology to design controller for SEPIC converter

The set of instructions to evaluate the unknown tuning parameters of PID controller is given as follows:

Step 1 Set the cost function *Z* and select the no. of variables and define their boundaries.

Therefore, the problem can be formulated mathematically as-

Minimize ISE (*Z*),
Subject to,

$$k_{pL} < k_p < k_{pU},$$
$$k_{iL} < k_i < k_{iU},$$
$$k_{dL} < k_d < k_{dU}$$

where k_{pL}, k_{iL}, k_{dL} and k_{pU}, k_{iU}, k_{dU} are the minimum and maximum values of the controller parameters.

Step 2 Choose a cuckoo (say *a*) randomly by Lévy flights, evaluate its corresponding *Za* and choose a nest out of *N* (say b) randomly.

Step 3 Exchange *b* by the newly obtained value of cost function if $Z_a > Z_b$.

Step 4 Check whether the predefined stopping condition arrives or not, if yes abandon a fraction (p_a) of the worst nest (and make a new nest at another location) and preserve the best solution otherwise go to ***step 2.***

IV. RESULTS AND DISCUSSION

A. Reduced Order Modeling:

The higher order SEPIC converter considered in this paper is represented by the following relation [16]

$$G_{SEPIC}(s) = \frac{1.998\,s^3 + 2.496 \times 10^6\,s^2 + 1.056 \times 10^8 s + 2.13 \times 10^{13}}{s^4 + 373.5\,s^3 + 8.88 \times 10^6\,s^2 + 2.91 \times 10^9 s + 3.215 \times 10^{12}} \quad (6)$$

The denominator of the reduced order model of SEPIC converter is obtained by Pade Approximation method [16] whereas the numerator is evaluated by cuckoo search algorithm as follows:

$$G_{RS\_Proposed}(s) = \frac{s + 2.508 \times 10^6}{s^2 + 341.2s + 3.786 \times 10^5} \quad (7)$$

with ISE = 7.5081 e^{-07}

On the other hand, the reduced model achieved by Pade approximation only [16] is given as follows:

$$G_{RS\_Pade}(s) = \frac{2.371s + 2.508 \times 10^6}{s^2 + 341.2s + 3.786 \times 10^5} \quad (8)$$

with ISE = 8.6748 e^{-07}

The time and frequency responses of higher and reduced order converter operating in open loop mode are plotted in Fig.4 and Fig.5, respectively, whereas Fig.6 and Fig.7 show their time and frequency responses when operating in closed loop mode. It is observed that the response of the proposed reduced model is much closer to the response of the higher order converter as compared to Pade approximation [15]. Therefore, in place of higher order SEPIC converter, its lower order model obtained by proposed method can be considered to design PID controller for the SEPIC converter. Hence the succeeding aim is to design a PID controller for the obtained reduced order converter.

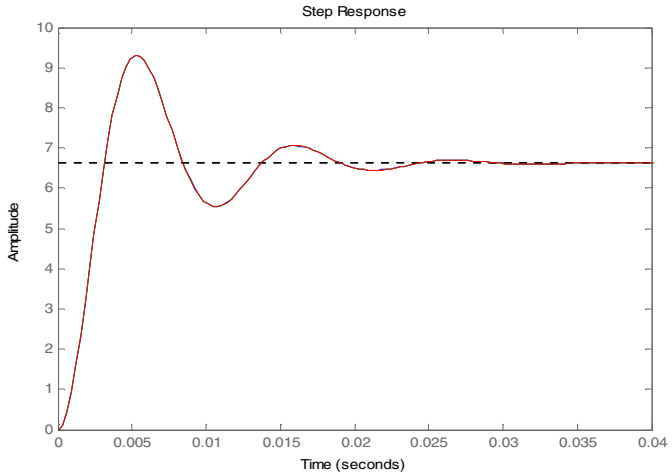

Fig. 4. Step Response of higher and reduced order converter (Open Loop)

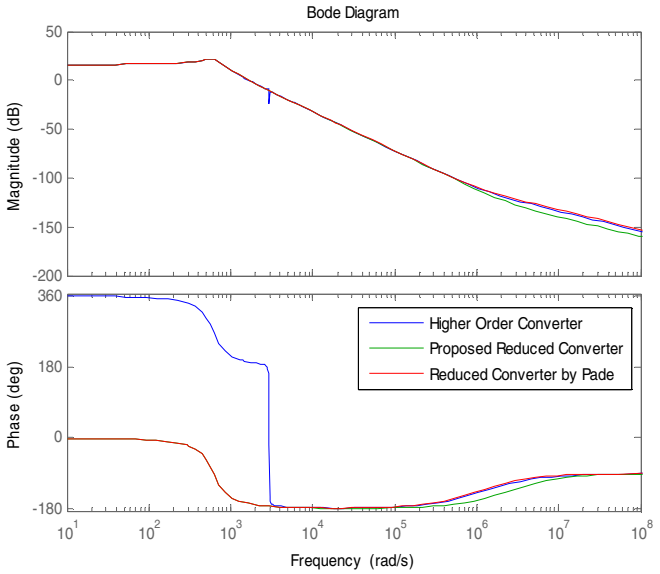

Fig5. Frequency response of higher and reduced order converter (Open Loop)

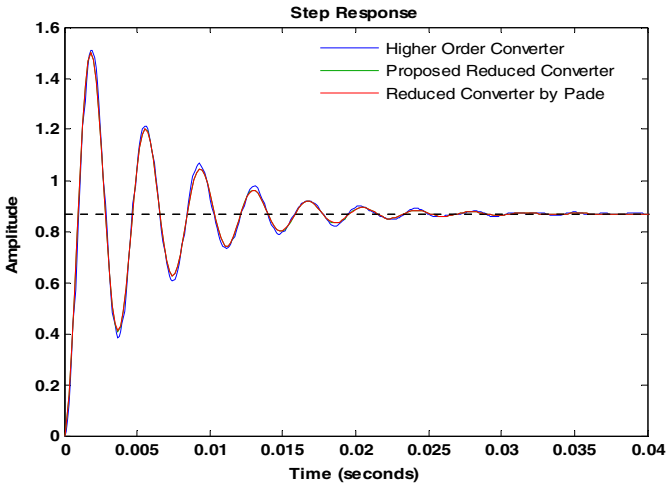

Fig6. Time Response of higher and reduced order converter (Closed Loop)

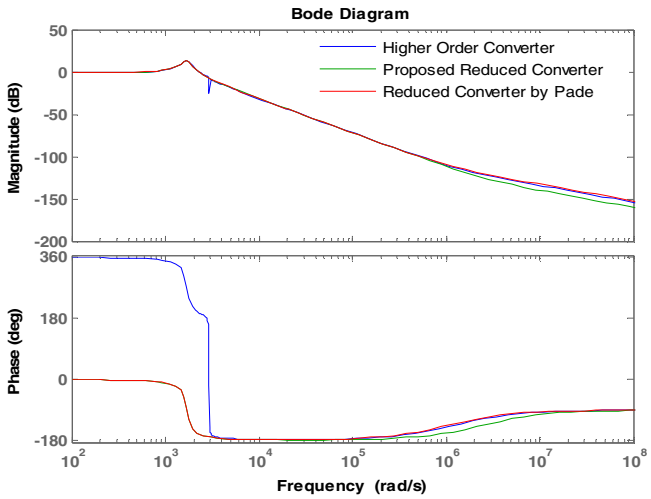

Fig7. Frequency response of higher and reduced order converter (Closed Loop)

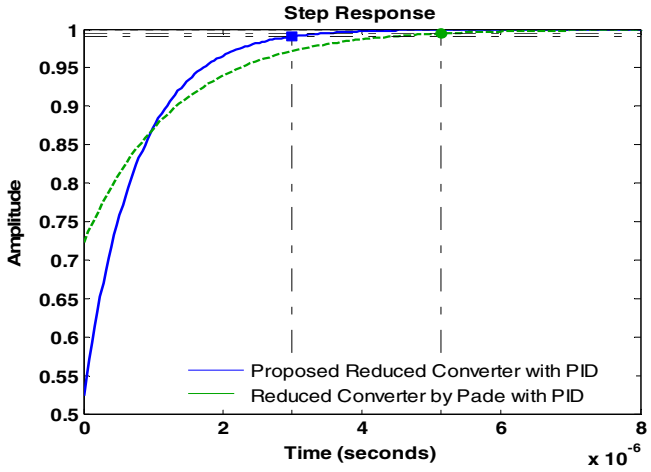

Fig8. Step response of closed loop SEPIC converter with PID controller

B. *Controller Design:*

In this section, PID controller is designed for proposed reduced order SEPIC converter and the optimal values of the gain are tabulated in Table I. In order to evaluate the performance of the proposed controller along with reduced order SEPIC converter, the performance parameters such as maximum overshoot (M_p), settling time (T_s) in second, rise time (T_r) in second and integral square error (ISE) are tabulated in Table II. Furthermore, the performance of SEPIC converter with compensator designed by Padhi et al. [16] is also observed, and the parameters are shown in Table II. It is revealed that the proposed PID controller exhibits better performance in terms of time response specifications and performance measure. The time and frequency responses of SEPIC converter with proposed PID controller when subjected to a unit step input are shown in Fig. 8 and Fig. 9, respectively. It is clearly observed from time response that the proposed SEPIC converter is faster than the Pade's converter.

TABLE I. GAINS OF PID CONTROLLER

Controller	k_p	k_i	k_d
Proposed	68.22	20.13	1.09

TABLE II. TIME RESPONSE SPECIFICATIONS OF SEPIC CONVERTER

Controller	T_s (sec)	M_p (%)	T_r (sec)	**ISE**
Proposed	$2.989\text{x}10^{-06}$	0	$1.676\text{x}10^{-06}$	$9.132\text{x}10^{-08}$
With Proposed Controller [15]	$5.143\text{x}10^{-06}$	0	$2.879\text{x}10^{-06}$	$15.325\text{x}10^{-08}$
With Compensator [15]	$7.57\text{x}10^{-02}$	26.59	$3.1\text{x}10^{-03}$	$4.2\text{x}10^{-03}$

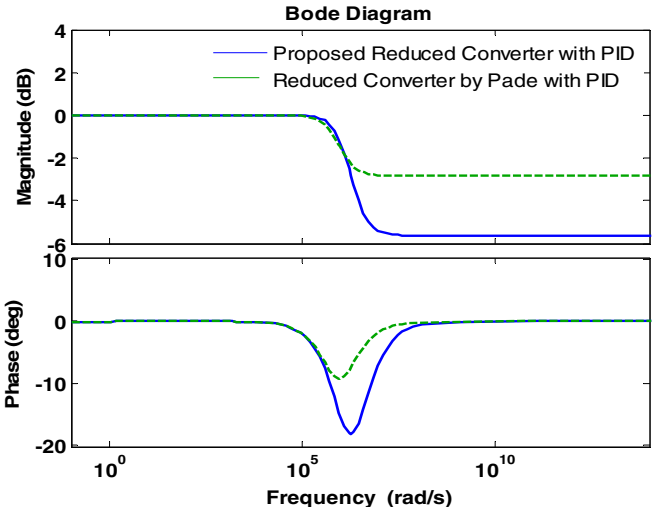

Fig9. Frequency response of closed loop SEPIC converter with PID controller

The unit step response of SEPIC converter with compensator is shown in Fig10. It is observed that the response exhibit damping oscillation along with the maximum overshoot 26.59% whereas maximum overshoot is zero in case of proposed PID controller. Also, the response of the SEPIC converter with PID controller is faster than the SEPIC converter with compensator.

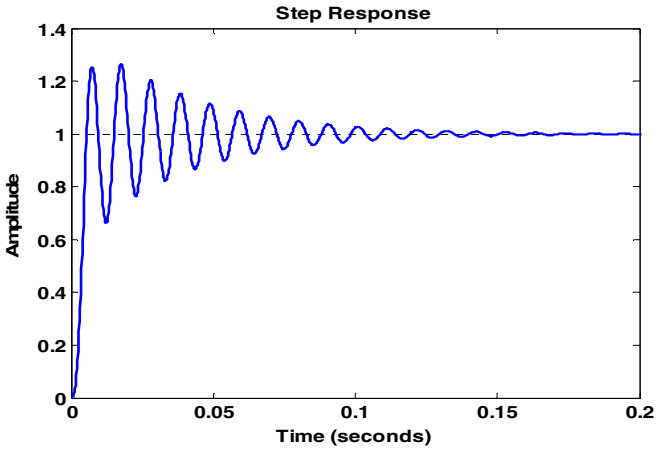

Fig10. Step response of closed loop SEPIC converter with compensator

V. CONCLUSION

In this study, reduced order modeling has been employed to design PID controller for SEPIC converter operated in continuous conduction mode (CCM). Reduced order modeling is achieved through optimization technique along with Pade approximation. Furthermore, the PID controller is designed for proposed reduced order SEPIC converter model. The performance of PID controller is tested on the SEPIC converter available in the literature. It is revealed that the proposed method for coefficient determination results in a better performance, and also, the response of the SEPIC converter with proposed PID controller is found faster than the response of SEPIC converter with compensator. The testing of the proposed controller fed SEPIC converter with LED driver circuit is currently being undertaken, and this will be published in our future work.

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