Challenges forTest and Fault-Tolerance due to Convergence of Electronics, Semiconductor Systems and Computing

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Abstract: Convergence of electronics, semiconductor systems and computing are rapidly transforming society at much faster pace than incorporation fault-tolerance and test methodologies in the systems. Further, underlying hardware and software in communication, security, quality of life, health, economic or financial well-being systems are increasingly being used for making decisions that influence individual and society. Consequently, it is imperative that the underlying hardware and software perform correctly and be defect free. However, to achieve zero defect through testing, screening and incorporation of redundancies is extremely challenging. This is what exactly the theme of my talk. During my presentation I will touch upon the mechanisms and issues to cope with the challenges.

Semiconductor, Fault-tolerance, Reliability, Test methodology, Dual function, Modular redundancy, Design for Testability (DFT), Built-In Self-Test, Linear Feedback Shift Registers (LFSRs) Keywords

I. INTRODUCTION

In process of miniaturization of Integrated Circuits (ICs) as the level of integration moves from Small Scale Integration (SSI), to Medium-Scale Integration (MSI), to Large Scale Integration (LSI), to Very Large Scale Integration (VLSI), to Very-Very Large Scale Integration (VVLSI), and to Ultra-Very Large Scale Integration (UVLSI), the complexity of integration provides many opportunities. Semiconductor device fabrication is the process adapted to create the IC. Figure 1 shows that how semiconductor process technology of 1971 moved from 10-µm process to 5-nm in 2017 [1] – [3]. Table 1 depicts some more attributes such as increase of functions per chip and operating frequency along with decrease of operating voltage. These attributes are above to the miniaturization as shown in Fig. 1.

Intel announce on March 30, 2017 that we pack 100.8 Million Transistors in each Square Millimetre [4]. This is Intel's latest-and-greatest chip generation: 10 nanometres (see Fig. 2). Intel says that this opportunity also emphasizes about the importance of another opportunity for the chipmaker to declare that Moore's Law (see Fig. 3) is alive and well—at least for Intel [4].

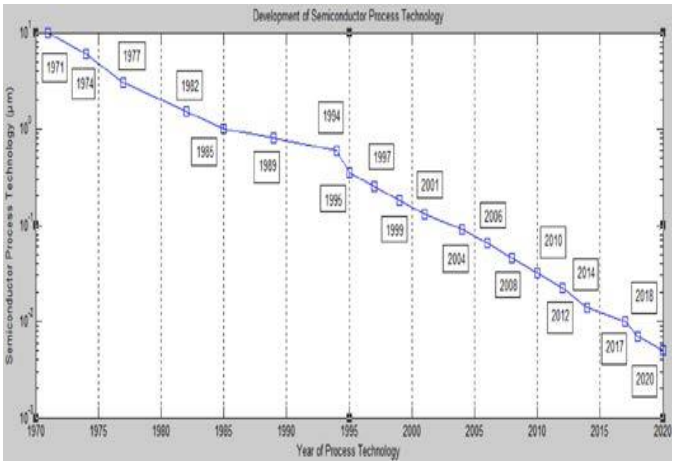

Fig. 1. Timeline of development of semiconductor process technology

TABLE I: TIMELINE: TECHNOLOGICAL DEVELOPMENT OF SEMICONDUCTOR PROCESSES

Year of Production	Functions per chip at production (million transistors)	Chip Frequency (MHz) On-chip local clock	Vdd (volts)
2003	153	2976	1.2
2004	193	4171	1.2
2005	243	5204	1.1
2006	307	6783	1.1
2007	386	9285	1.1
2008	487	10972	1.1
2009	614	12369	1.1
2010	773	15079	1.1
2012	1227	20065	0.9
2013	1546	22980	0.9
2015	2454	33403	0.8
2016	3092	39683	0.8
2018	4908	53207	0.7

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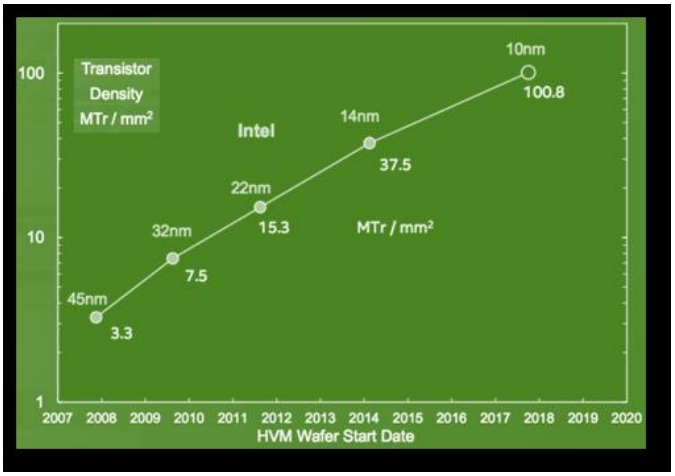

Fig. 2. Timeline: Technology development of semiconductor process for transistor density

The foundational force of Moore's Law has driven breakthroughs in modern cities, transportation, healthcare, education, and energy production. In fact, it's quite difficult to envision what our modern world might be like without Moore's Law. Moore's observation transformed computing from a rare and expensive venture into a pervasive and affordable necessity. This development not only enhanced existing industries and increased productivity, but it has spawned whole new industries empowered by cheap and powerful computing. Moving forward, Moore's Law and related innovations are shifting toward the seamless integration of computing within our daily lives. This vision of an endlessly empowered and interconnected future brings clear challenges and benefits. Privacy and security are persistent and growing concerns. But the benefits of ever smarter, ubiquitous computing technology, learning to anticipate our needs, can keep us healthier, safer, and more productive in the long run [5].

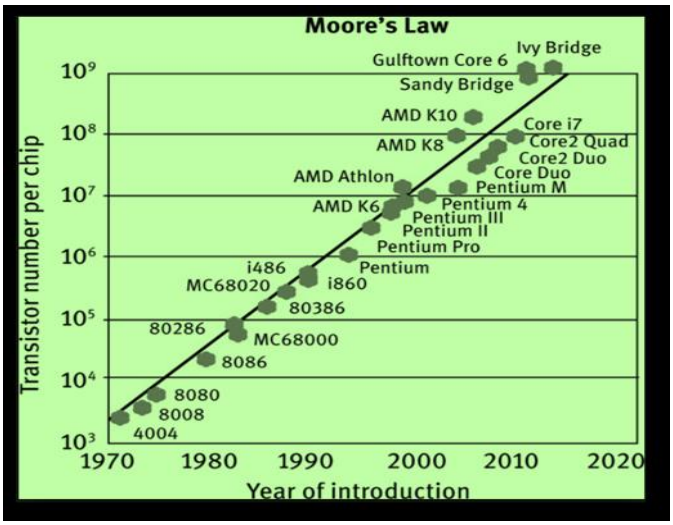

Fig. 3. The Moore's Law applicability

As an example of the impacts; in Fig. 4 the statistic depicts the total number of smartphone users worldwide from 2014 to 2020. For 2016, the number of smartphone users is forecast to reach 2.1 billion. Literature [6] reports that there will be an estimated 6.1 billion smartphone users by 2020]. It is roughly and estimation concludes that about more than 400 million transistors for each one of the 7.6 Billion people on earth [7] - [9].

"All these things are difficult, but once they're done they seem normal. And that's the magic of Moore's Law." – Intel's Kaizad Mistry [5]. Also, Kaizad Mistry told IEEE Spectrum [4] that "Moore's Law's future is difficult and requires inventions." In ensuing section, we look for attributes and consequences.

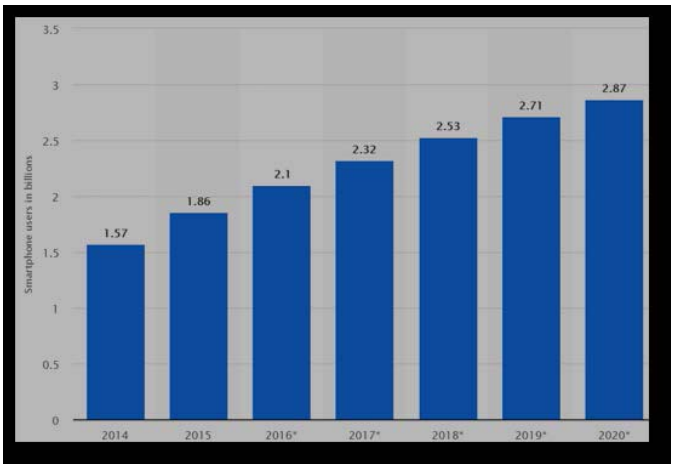

Fig. 4. The statistic depicts the total number of smartphone users worldwide from 2014 to 2020. For 2016

II. ATTRIBUTES

Delivering more transistors in the same area means the circuitry can be made smaller, saving on cost, or it means that more functionality can be added to a chip without having to make it bigger. The circuits are becoming more complex but compact. The ICs are growing with more depth and density. Hence, allows us to put more circuitry in a smaller and more reliable package.

The consequences are:

- As the level of integration increases, the common faults are moved from the pins and the package to the semiconductor material.
- The increased complexity of design increases the probability of design errors.
- Lower operational voltages decrease the noise margins and increases the frequency of transient faults.
- Due to the movement of the common faults from the pins and the package to the semiconductor material makes

physical access for test purpose either difficult or even impossible.

- Further, the ICs growth along with its increasing complexity encounters the problem of large amount of test data also, number of access ports remains constant hence forcing towards long test application time.
- High speed ICs further complicates the testing problem enforces the high demand on tester's driver/sensor mechanism and more complicated failure mechanism.

The section below is dedicated to look into the prospects of the technological developmental from the angle of Fault-tolerance and testing.

III. OPPORTUNITIES FAULT-TOLERANCE AND TEST DUE TO TECHNOLOGICAL CHALLENGES

Fault-Tolerant approaches that were not cost effective in the past [11] – [42] can now be used because, due to reasons

- That duplicated processors can now be placed on a single chip that was previously available on multiple boards.
- That implementation of n-modular redundancy becomes less costly.
- That fault detection and fault location can now be provided within the IC itself. Previously, these provisions were on board or the system level.
- That detecting faults closer to the site of their origin minimizes the propagation of errors throughout the system.
- That it is possible to use redundancy to improve the yield of circuits, often the yield of complex ICs is less than 10%. Low yield implies high cost of circuit
- That IC can be made usable if additional circuitry is included to replace some, or all, defective modules with spares
- That duplication with complementary logic to combat common mode faults.
- That the implementations of effective and efficient Cyclic Redundancy Checks (CRC) and other fault detecting techniques have become feasible.
- That the implementations effective Redundant Arrays of Inexpensive Disks (RAID) combinations become possible to utilize.
- That the concepts of Design for Testability (DFT), Built-In Test (BIT) and Built-In Self-Test (BIST) have become more feasible. An architecture of BIST is shown in Fig. 5.
- That the algorithmic test generation and fault insertion can be applied easily.
- That the path sensitization method and Boolean difference can be utilized effectively.
- That the length of Linear Feedback Shift Register can be increased for the purposes of generation of Pseudo-random test patterns and compression of response data using Signature analysis method.
- That the implementation of multimode testers in cost effective manner becomes possible.
- That the implementations effective Redundant Arrays of Inexpensive Disks (RAID) combinations become possible to utilize.

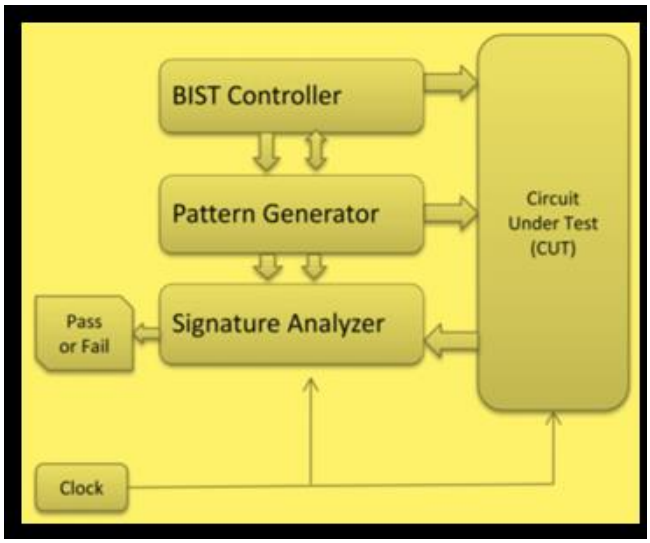

Fig. 5. The BIST architecture

IV. CONCLUSIONS

Through this presentation author wants to show the impact of present technology on Fault-Tolerance and test technology. Chemically Assembled Electronic Nanotechnology (CAEN), an emerging base technology in developing nanoscale devices show horizons of a new era in digital circuit design. Since defect rates are relatively high for nanofabric technology, work continues to improve the defect detection and novel ways to deal with defects.

Procedures for nanofabrics based on chemically-assembled electronic nanotechnology BIST need more attention in this era. There is need to study for devising recovery procedures to identify defect-free nanoblocks and switchblocks in the nanofabric under test. It is expected that the BIST architectures and recovery procedures that are based on the reconfiguration of the nanofabric can be targeted to achieve complete fault coverage of different types of faults. Large fraction of defect-free blocks can be recovered using a small number of BIST configurations. Further, emphasis is needed to bring BIST procedure that will be well suited for regular and dense architectures that have high defect densities.

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