A Mixer-First Receiver With Class-F Adiabatic Switching

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***Abstract*—This letter introduces the use of *class-F adiabatic switching* in a mixer-first 2.45-GHz ISM-band receiver. By using the principle of adiabatic switching with a class-F VCO, a resonant multiharmonic drive for an N-path-based mixer-first receiver is generated, resulting in a reduced power consumption while maintaining a good mixer noise figure (NF). To optimize the area, coupled inductors in the VCO are used. By employing a switched capacitor (SC) feedback network in the baseband (BB) amplifier, a proper input matching and flexible common-mode (CM) bias is achieved. A packaged chip implemented in 28-nm CMOS achieves a low-power consumption of 3.5 mW with a gain of 22 dB and an NF of 7.4 dB.**

***Index Terms*—Adiabatic, class-F, CMOS, low power, mixer first, N-path filter, receiver, RF.**

I. Introduction

Numerous N-path filter or mixer-first designs that offer excellent linearity, flexibility, and filtering behavior have recently been developed. As shown in [1], where a fully passive design was introduced, very low-power N-path or mixer-first designs that require power only for mixer drive generation can be realized. The remaining power consumption could potentially be minimized by using a resonant mixer drive, for instance, based on a quadrature oscillator [2]. However, the bulky oscillators and matching network, and the potential VCO-to-RX coupling make this approach unfavorable. As a result, N-path-based mixers with a resonant drive, as presented in [3], were introduced, incorporating a single VCO at twice the RF frequency and reducing chip area and design complexity. This approach further decreases the power consumption of mixer-first designs, but the design described in [3] must be improved upon, since it requires several mm^2 of chip area and consumes about 10 mW.

This work presents a 2.45-GHz ISM band receiver in 28-nm CMOS that exploits the principle of adiabatic switching by reshaping the oscillator signal, using a class-F VCO with chopped baseband (BB) transimpedance amplifiers (TIAs) to achieve a three-times less overall power consumption of 3.5 mW compared to previous resonant designs [3]. The receiver concept is shown in Fig. 1, where the key building blocks are highlighted.

The following section describes the advantages of this *class-F adiabatic switching*. Afterward, the key circuits, such as the VCO and switched-capacitor (SC) BB TIA, are described. Finally, measurement results are presented and compared to state-of-the-art mixer-first receiver designs.

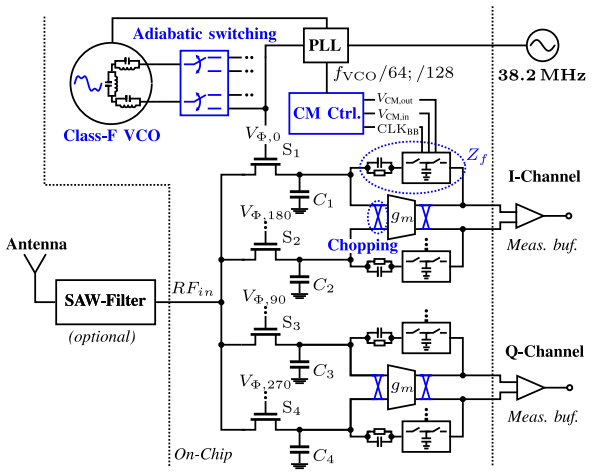

Fig. 1. Overview of the realized receiver with class-F adiabatic switching.

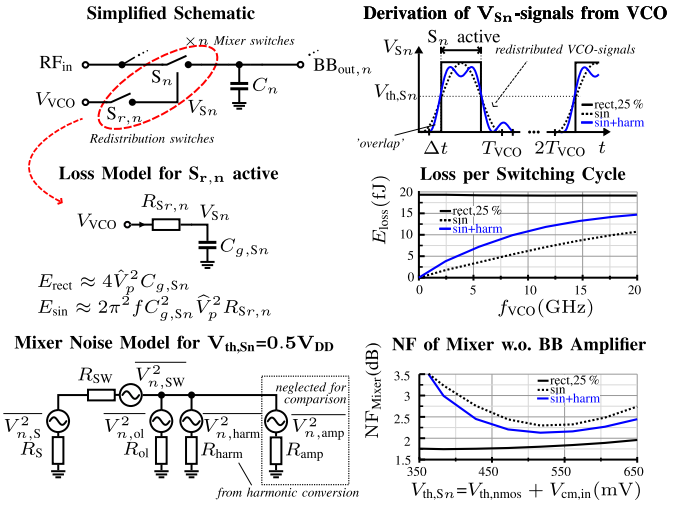

Fig. 2. Loss model and LTI noise model for the mixer-first receiver with adiabatic switching.

II. Consequences of Class-F Adiabatic Switching

This section describes how adiabatic switching with a sinusoidal waveform, where the energy needed to charge capacitive nodes is recovered when discharging the same node [4], can be beneficially used in N-path-based mixers to reduce power consumption. It then shows that this sinusoidal switching negatively affects the noise figure (NF) performance, but this can be improved using class-F LO signals where power consumption can be lowered as buffering stages become unnecessary. First, the losses due to adiabatic switching are derived, before explaining the NF behavior and the impact of adding class-F switching.

The losses of the resonant drive are caused by the resistance of the redistributing network and can be estimated employing the model shown in Fig. 2. The sine-wave current, caused when the oscillation of the VCO tank drives the switch S_n, flows through the (assumed) constant equivalent series resistance $R_{Sr,n}$ of the VCO redistribution network, so the thermal losses E_{sin} per VCO period T (which are

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directly linked to the average power consumption) can be approximated similar to [4] by ($I_\mathrm{p} = 2\pi f C_{g,\mathrm{S}n}\hat{V}_\mathrm{p}$) with $\hat{V}_\mathrm{p}$ being the peak amplitude to reach a swing between 0 V and V_DD

$$E_\mathrm{sin} = R_{\mathrm{S}r,n}\int_0^T I_\mathrm{p}^2 \sin^2(2\pi f t)dt \approx 2\pi^2 f C_{g,\mathrm{S}n}^2 \hat{V}_\mathrm{p}^2 R_{\mathrm{S}r,n}. \quad (1)$$

Equation (1) shows the adiabatic property. For an infinitely long VCO period $T_\mathrm{LO} = f^{-1}$, the charging losses approach a minimum [4], however, these losses increase with frequency. Superimposing multiple sine waves results in a summation of the losses for each wave.

In comparison, an ideal rectangular switching signal (or charging and discharging of a gate capacitance) leads to a total loss per period of

$$E_\mathrm{rec} \approx \left(2\hat{V}_\mathrm{p}\right)^2 C_{g,\mathrm{S}n} \quad \text{for} \quad T_\mathrm{LO} \gg R_{\mathrm{S}r,n} C_{g,\mathrm{S}n}. \quad (2)$$

Both (1) and (2) are verified via simulation and compared in Fig. 2, where it can be seen that, as long as the timing constant $\tau = R_{\mathrm{S}r,n}C_{g,\mathrm{S}n}$ allows proper settling, the adiabatic case always results in less losses.[1]

This sine-wave-based approach was already utilized in [3], however, using a single sine wave causes an increased NF. To improve the mixer NF, class-F adiabatic switching is proposed. This is achieved by using a class-F VCO [5] with additional third harmonic content in the oscillation waveform to produce a more rectangular signal that directly oscillates onto the mixer switches. The improved waveform decreases the overlap between LO switching phases as well as the effective resistance of the mixer switches, compared to a regular sine-wave approach.

To prove the NF benefits of class-F switching, the linear time-invariant (LTI) noise model previously derived in [3] is adapted as shown in Fig. 2, where

$$\mathrm{NF} = 1 + \frac{R_\mathrm{SW}}{R_\mathrm{S}} + \frac{(R_\mathrm{S}+R_\mathrm{SW})^2}{R_\mathrm{S}R_\mathrm{harm}} + \frac{(R_\mathrm{S}+R_\mathrm{SW})^2}{R_\mathrm{S}R_\mathrm{ol}} + \ldots \quad (3)$$

Due to nonrectangular switching of the mixer switches, R_SW is larger compared to regular mixer-first implementations, and consequently constitutes the main contributor to the mixer NF, followed by R_harm caused by harmonic conversion [3] and an additional R_ol to account for the noise caused by effective overlap of the switching phases (for simplicity, the impact of the following BB amplifier is left out, as it is assumed to be identical in sine wave and class-F case). To derive the benefit of harmonic switching, the impact of a more rectangular waveform on R_SW and R_ol is observed in the following.

For creating the noise model, it was assumed that the timing constant for the BB signals is larger than the switching period T_LO, such that $V_{C,n}$ can be viewed as constant during the *on* phase of a mixer switch. Consequently, the voltage across the switch (V_SW) can also be viewed as constant, and an equivalent resistance for R_SW can be formed by applying the conservation of charge to both the equivalent resistance and time-dependent resistance as follows:

$$Q_\mathrm{trans} = \frac{V_\mathrm{SW}\cdot T_\mathrm{LO}/4}{R_\mathrm{SW,eq}} = \int_0^{T_\mathrm{LO}/4} I_\mathrm{SW}(t)dt. \quad (4)$$

In this design, a single nMOS transistor switch is used, so that $I_\mathrm{SW}(t)$ can be replaced with an approximation for the drain–source current in the linear region (with $K = \mu_n C_{ox} W/L$), resulting in

$$R_\mathrm{SW} \approx \frac{T_\mathrm{LO}}{4K}\left[\int_0^{T_\mathrm{LO}/4}\left[V_\mathrm{GS}(t) - V_\mathrm{th}\right]dt\right]^{-1} \quad (5)$$

[1]We assume that the circuit for steering the clock redistribution barely changes between both cases and consumes the same amount of power.

$$V_{GS}(t) = \hat{V}_A \tfrac{4}{\pi}\textstyle\sum_{x_n=1,3,\ldots}^{n} \tfrac{1}{x_n}\sin(2x_n\omega_\mathrm{LO}t) + V_\mathrm{b,th} \quad (6)$$

To recognize the difference between an ideal rectangular and a sinusoidal waveform, $V_\mathrm{GS}(t)$ is replaced with the Fourier series approximation for a rectangular signal with a peak-to-peak amplitude of $V_\mathrm{DD} = 2\hat{V}_A$, shown in (6). With parameter n, the number of harmonic frequencies can be set. First, $V_{b,\mathrm{th}}$ is set to V_th. This results in a general expression for the resistance, where a minimum resistance $R_\mathrm{rect} = 2/(KV_\mathrm{DD})$ is weighted according to the number of harmonics used:

$$R_\mathrm{SW} \approx \frac{T_\mathrm{LO}}{4K}\left[\int_0^{T_\mathrm{LO}/4}\frac{V_\mathrm{DD}}{2}\frac{4}{\pi}\sum_{x_n=1,3,\ldots}^{n}\frac{1}{x_n}\sin(2x_n\omega_\mathrm{LO}t)dt\right]^{-1}$$
$$\approx R_\mathrm{rect}\frac{1}{4}\left(\sum_{x_n=1,3,\ldots}^{n}\frac{2}{\pi^2 x_n^2}\right)^{-1} \quad (7)$$

The formula was verified via simulation, where 12, 10.6, and 3.5 Ω were determined for one, three, and infinite harmonics, respectively, at a switch-W/L ratio of 1280.

The remaining off-resistance R_off between mixer-paths (caused by the larger overlap of the switching signals compared to rectangular signals) is also affected by the additional harmonic. R_off is located in parallel to the series switch resistance R_SW, and for $R_\mathrm{SW} \ll R_\mathrm{off}$, $R_\mathrm{off} \propto R_\mathrm{ol}$. For estimating the *off* resistance the same procedure as for R_SW applies, but this time, the transistor is not operating in the linear region, requiring an adapted formula for the drain current from weak through strong inversion for small V_DS according to [6]

$$I_\mathrm{DS} = \alpha_1 V_\mathrm{DS}\ln\left[1 + e^{\alpha_2[V_\mathrm{GS}(t)-\beta V_\mathrm{th}]}\right]^2 \quad (8)$$

where α_1 accounts for technology parameters and scaling, α_2 accounts for substrate factor and thermal voltage, and β accounts for threshold variations. The remaining integral of (4) cannot be solved using standard mathematical functions and needs to be calculated numerically. Nevertheless, it can be seen that transistor scaling has an inverse effect on the effective *off* resistance. Numerically solving the integral for the mentioned waveforms shows that (in our case) a harmonically enriched sine wave improves the resistance by a factor of 1.88 compared to a single sine wave, while being nearly independent of α_2 or β.

Fig. 2 shows the simulated impact of different waveforms on the NF. Regulating the input common mode (CM) $V_\mathrm{cm,in}$ affects the transistor overdrive voltage and thereby allows the threshold of the switch $V_{\mathrm{th},S,n}$ to be adjusted such that (6) can be manipulated for optimizing the mixer NF. Consequently, using the class-F switching results in a tradeoff between improved mixer NF by adding additional losses of the harmonic contend [see (1)]. In our realization, however, we were able to break this tradeoff by driving the LO divider resonantly, as the enriched waveform now allows proper switching without buffering. This addition resulted in an overall power consumption reduction (compared to a VCO without a class-F *LC* core) of roughly 18% to 360 μW, while maintaining the benefit for the NF performance. The following section describes how the resonant path of the receiver was designed to achieve a successful class-F adiabatic switching.

III. Realizing the Resonant Path

Fig. 3 shows the generation of the harmonically enriched LO signal by a class-F VCO. The oscillator coil is realized in an area-efficient way using coupled inductors and forms three resonant tanks. The structure is equivalent to a transformer approach with two tanks [5] and was chosen due to slightly relaxed design rules. The quality factors and coupling of the tanks were matched to achieve the desired

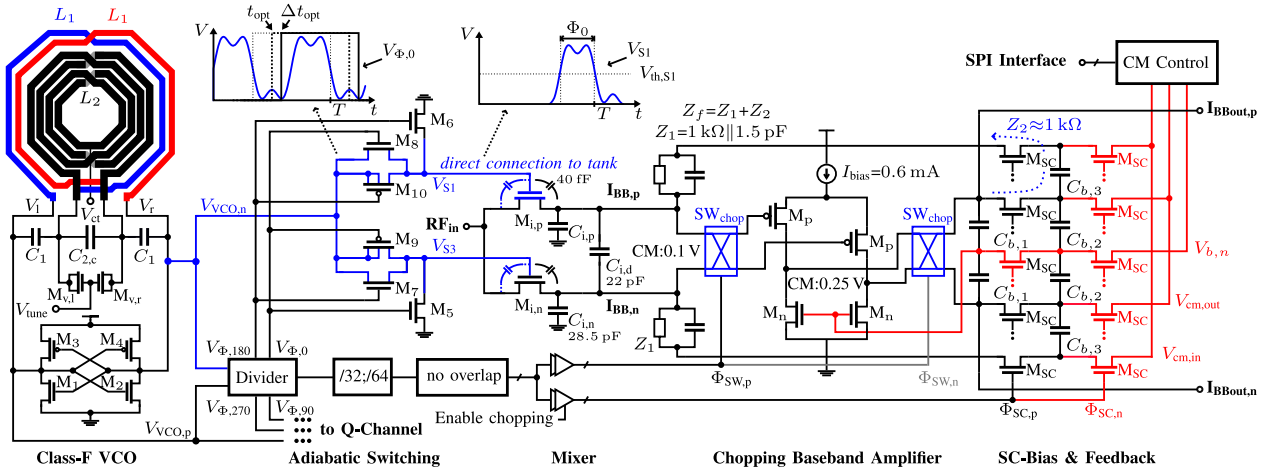

Fig. 3. Simplified circuit diagram of the realized class-F adiabatic switching path, including BB amplification.

amplitude ratio of the oscillations. To frequency tune the VCO, tuning the center tank capacitance is sufficient, as the coupled tanks follow it reasonably well with negligible impact on the phase-noise performance. The tank is directly connected to the mixer switches via the highlighted redistribution network, which is controlled by four phase-shifted 50% duty-cycle signals derived from the VCO via a divider. This divider omits input buffering, as the class-F VCO signal provides sufficient drive. The delay of the divider outputs is designed to hit an adiabatic-switching point Δt_{opt} (Fig. 3) by decreasing transistor W/L ratios and thereby minimize the switching losses. A proper off-state is ensured by adding minimum-sized transistors M_5/M_6 to remove the remaining charge, and adding negligible energy loss. A 0.065-mm^2 capacitor array is used to achieve a bandwidth of 4.1 MHz for a desired Bluetooth EDR variant with 8 Mb/s and 4-MHz channels.

Two BB TIAs (see Fig. 3) generate 21 dB of voltage amplification with a g_m of 16.5 mS while consuming 1.3 mW including biasing. SC-biasing was used to separately control the input and output CM, so that the mixer NF can be improved compared to the results from Section II. The lower input CM allows for using nMOS core devices as mixer switches M_i, to achieve a low on-resistance and less parasitic capacitance. The clock for the SC network (and for the chopping) is derived from the VCO by division by 64 or 128. Separation of both CM loops is achieved by splitting the feedback impedance Z_f into two parts (Z_1 and Z_2), where Z_2 is formed by an SC resistor. The feedback impedance is designed to provide a 50-Ω input impedance at the RF input, with effective resistances for harmonic mixing and overlapping. To maintain a low-power design, the bias current for a single TIA needs to be limited to less than 1 mA. By doing so a tradeoff between NF, power consumption, and linearity was made, limiting the overall NF to 7 dB while maintaining an IIP3 above −17 dBm, meeting the minimum linearity requirements of the Bluetooth standard while maximizing the SNR for higher data rates and increased range. Additional chopper switches are used to reduce the Flicker noise impact of the transistors M_p/M_n and improve the NF for narrowband signals by adding 100 μW of power.

IV. Measurement Results and Comparison

A test chip (shown in Fig. 4) with an active area of 0.25 mm^2 was fabricated in a 1P8M 28-nm CMOS technology and packaged in a QFN 5×5 housing. An external 38 -MHz reference clock was used to lock the center frequency of the receiver to 2.45 GHz via the on-chip PLL. In this prototype, an integer-N PLL has been integrated,

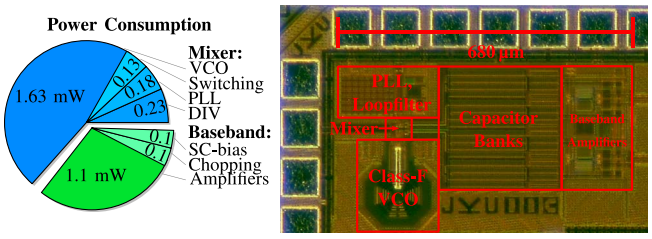

Fig. 4. Power consumption breakdown and micrograph (active area: 0.25 mm^2).

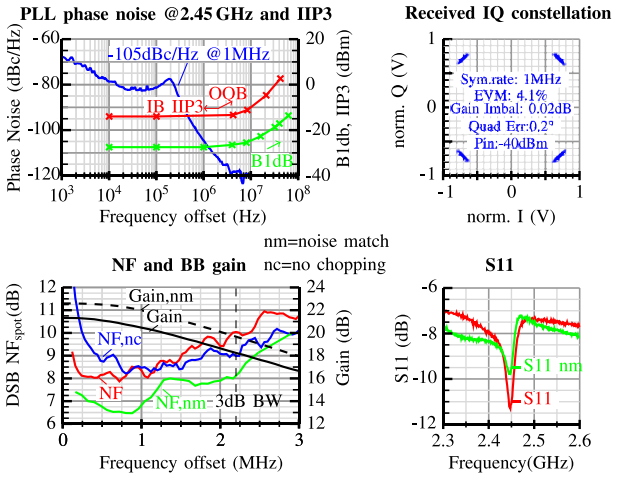

Fig. 5. Measurement results of the fabricated receiver.

which can be extended to fractional-N operation in a straightforward way. Fig. 5 summarizes the main measurement results. The phase noise of −105 dBc/Hz at 1-MHz offset and 2.7-ps RMS jitter was determined from a VCO leakage signal measured at the RX input at a power level of −62 dBm. With an external dc-blocking capacitor an S_{11} of −10.9 dB, a gain of 21 dB, an IIP2 of 30 d Bm and a 3-dB bandwidth of 4.1 MHz were achieved. The in-band IIP3 of −16.5 dBm was dominated by the BB amplifiers, while the out-of-band (OOB) IIP3 with a carrier offset of 41 MHz was increased to 2.5 dBm which is sufficient to fulfill the minimum requirements for Bluetooth. The simulated double-sideband (DSB) NF of 7 dB for an RF bandwidth of 4 MHz was not reached due to a degraded S_{11}, caused by additional packaging parasitic of the bond wires. By

TABLE I
COMPARISON OF RECENTLY PUBLISHED N-PATH OR MIXER-FIRST RECEIVERS

	This Work	**JSSC'20 [1]**	**JSSC'13 [3]**	**JSSC'20 [7]**	**ISSCC'17 [8]**
Architecture	mixer-first +TIA	mixer-first fully passive	mixer-first +harm. rej.	mixer-first +TIA	N-path based
Technology	28 nm	28 nm FDSOI	65 nm	28 nm	28 nm
Supply (V)	0.9	0.8	1.3	1.2	1.2/1
Area (mm^2)	0.25	0.23	2.9	0.16†	0.49
Freq (GHz)	2.45	0.6–1.3	0.7–3.2	0.5–2	0.1–2
Power(mW)	1.7$^{\#}$	1.44*	—	21.6	—
incl. VCO(mW)	3.5	—	10–12$^{\sim}$	37.2'	38–96
IIP3 (dBm)	−16.5	—	−43	−12	<5
OOB IIP3 (dBm)	2.5	25	10	25	44
Δf/BW	10	10	>10	13	6
Gain (dB)	22	9–14	36	32.4	13'
NF (dB)	7.4	5–9	7–13	5.5	10'
BB BW (MHz)	4.1	16	0.1–20	260	13
Input	single-ended	differential	single-ended	differential	differential

$^{\#}0.46\,\mathrm{mW}$ wo.LNA, $^{*}1.6\,\mathrm{mW}$ expected for 2.45 GHz, $^{\sim}$without PLL, †without LO, 'at 2 GHz

adapting the bias of the amplifier and the CM voltages, the receiver can be digitally tuned to a noise match to achieve an improved NF of 7.4 dB with 22-dB gain by relaxing the S_{11} toward −9.5 dB. The total power consumption is 3.5 mW in both cases, where the main contributors are the VCO (1.6 mW) and the IQ BB amplifiers including SC circuitry (1.3 mW).

Table I compares the proposed receiver with one of the earliest resonant mixer-first RX in [3] and designs from other recent publications in scaled technology nodes. In direct comparison with [3], the added class-F VCO results in a similar NF for 2.45 GHz while lowering the power consumption to 3.5 mW at a tenth of the chip area, showing the power-saving potential of the class-F adiabatic switching. In comparison with the fully passive design in [1], where an NF of $>$ 9 dB and a power consumption of 1.6 mW (estimated for a 2.45-GHz realization) is achieved, the presented design offers a better gain and NF at a similar power consumption. However, the reduced power and chip area come at the price of a degraded RX linearity and VCO tuning range, as can be seen in comparison with other approaches, such as [7] and [8], which, in turn, consume 10× more power.

V. CONCLUSION

This letter introduces the idea of class-F adiabatic switching for realizing low-power receivers, demonstrated at a 28-nm CMOS mixer-first-based design. The necessary switching signals are directly generated in the harmonically enriched VCO, using area-efficient coupled inductors, while a BB amplifier with SC-feedback ensures a flexible CM bias to optimize NF performance of the mixer-first RX. An integrated PLL and TIA complete the mixer, resulting in a receiver for the 2.45-GHz ISM band for Bluetooth-like applications. Measurements confirm a low-power consumption in comparison with similar mixer-first approaches while maintaining a maximum of integration.

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