A 55.9-fs Integrated Jitter (100 kHz–100 MHz) Hybrid LC-Tank PLL in 5-nm FinFET Using Programmable Phase Realignment and Dynamic Coarse Tuning

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***Abstract*—We propose a hybrid LC-tank PLL realized in 5-nm FinFET CMOS for radar and 5G mobile applications. The oscillator has three input ports: 1) a conventional arrangement of phase/frequency detector and charge pump controls the oscillator via its tuning voltage; 2) a programmable phase realignment injects ultranarrow and ultrasharp complementary reference pulses into the oscillator to adjust the timing of its waveform's peaks and valleys; this improves the in-band phase noise and helps to mitigate the worsening flicker noise in advanced process nodes; and 3) a dynamic coarse tuning digitally extends the oscillator's tracking range by allowing it to quickly recenter the varactor. The PLL achieves 55.9-fs integrated jitter (from 100 kHz to 100 MHz).**

***Index Terms*—Dynamic coarse tuning (DCT), fast settling, hybrid PLL, injection locking, realignment, reference spur.**

I. Introduction

A PLL for multi-GHz clock synthesis needs to employ an LC tank in its oscillator to meet the sub-120-fs integrated jitter performance [1], [2] for radar and 5G mobile applications. In conventional charge pump (CP) PLLs, LC-VCOs are typically tuned by a parallel bank of switched MOM capacitors for coarse frequency selection and an accumulation-mode varactor for fine control. Once the coarse frequency band is calibrated, the varactor must have sufficient tunability to maintain the phase lock across the allowable supply voltage (V_{DD}) and temperature fluctuations. Unfortunately, the strife for wide tuning range (TR) degrades the varactor's quality (Q) factor, which worsens phase noise (PN), thus increasing integrated jitter, especially at higher VCO frequencies. As a solution, we propose dynamic coarse tuning (DCT) to extend the effective tunability of the narrow analog varactor while maintaining its high Q-factor.

Furthermore, the flicker noise becomes worse with the process technology migration [3], which degrades the noise of a CP, thus impacting the in-band PN of PLL. The effect of CP noise on the PLL PN can be calculated as

$$\mathcal{L}_{\mathrm{PUMP(dB)}} = 20\log\left(\frac{F_{\mathrm{VCO}}}{F_{\mathrm{REF}}}\right) + 10\log\left(8\pi^2 \cdot \frac{\overline{i_n^2}}{I_{\mathrm{PUMP}}^2} \cdot \frac{T_{\mathrm{reset}}}{T_{\mathrm{FREF}}}\right)$$

where T_{reset} is a reset pulse width of a phase/frequency detector (PFD), and $i_n{}^2$ is the current noise through the PLL loop filter. Constraining all devices of the CP to be of the same dimension, the simulated CP noise at 1-MHz offset degrades by ~8 dB when going from the 28- to 7-nm node, while experiencing further worsening at 5 nm. Although the 5- and 7-nm devices can offer shorter latency to improve the CP noise, the reset pulse of PFD should stay wider than 20 ps due to the fact that a level shifter typically used to convert the PFD's output from the analog to digital domains may suffer failures across process, voltage, and temperature (PVT) corners. Fortunately, in a 5-nm process, a larger driving current can be provided by a smaller FinFET device in order to achieve faster transition times and narrower pulse widths. This can benefit the phase realignment [4] and injection locking [5] techniques to help fighting the worsening flicker noise. In [5], the LC-VCO's PN at lower frequency offsets is suppressed via a switch that shorts the VCO's differential output. That shorting ("horizontal") switch is driven by a "shorting pulse," which comes from a high-quality reference clock. However, the reference spur is *degraded* by the insufficiently narrow shorting pulse. In [4], the VCO's in-band PN is improved by using a buffer to "drag" the VCO edge toward the correct position for suppressing the memory of past errors. That buffer is driven by a high-quality reference clock with a suitable pulse width. In our previous work [6], we used the phase realignment to improve in-band PN in a ring-type oscillator-based PLL. However, it is not possible there to adjust the delay between the F_{REF} and realignment clock edges, the realignment pulse width or the driving strength of realignment devices. Consequently, that work is far from achieving optimized integrated jitter and reference spurs.

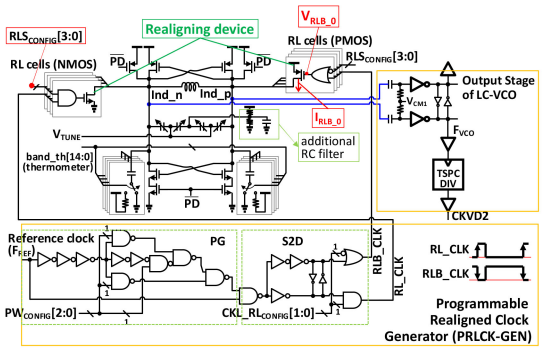

Fig. 1. Proposed LC-VCO with programmable phase realignment.

In this letter, we propose a *programmable* phase realignment of the LC-tank oscillator with a programmable injection of narrow and sharp reference pulses (Fig. 1). To solve the troublesome issue of delay mismatch between the conventional F_{REF} and realignment clock domains, we first identify the paths for the skew cancellation (Fig. 3) and then propose a simple circuit solution that avoids any complex calibrations [e.g., a delay-locked loop (DLL)], thus simplifying the overall

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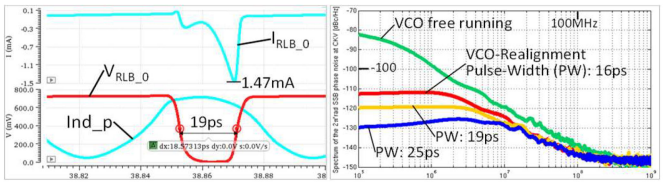

(a) (b)

Fig. 2. LC-VCO post-layout simulations at 13.92 GHz in a typical corner: (a) waveforms and (b) PN.

design and layout. The DCT, programmable phase realignment, and skew cancellation are built in the digitally intensive hybrid LC-PLL architecture realized in 5-nm FinFET CMOS to achieve low jitter and wide tuning range.

II. Architecture and Circuit Design

The proposed LC-VCO with a programmable realignment, as shown in Fig. 1, is composed of a complementary cross-coupled LC-tank oscillator, programmable complementary realignment cells (RL cells, including pMOS pull-ups and nMOS pull-downs for pulse injections), and a programmable realignment clock generator (PRLCK-GEN). The MOM-cap array provides wide tuning from 11.9 GHz to 14.4 GHz. In the chosen configuration, the fine-tuning varactor would need a TR of 1.4× of the coarse step size to cover the V_{DD} and temperature fluctuations. The proposed arrangement of varactors embeds an additional RC filter to shunt any ac current originating from the left/right tank mismatch, thereby suppressing stray currents from flowing back to the loop filter control voltage (V_{TUNE}) node. The capacitance of the additional RC filter is designed 10× larger than the fine-tuning varactor while its resistance is over 50 kΩ to minimize the dc current. The programmable RL cells are composed of four nMOS devices with NAND and four pMOS devices with NOR gates that are driven by RL(B)_CLK; their strength is controlled by RLS_{CONFIG}[3:0]. The injecting transistors are of minimal dimensions but of high performance for minimizing the parasitic capacitance of wire connections of the resonating nodes "Ind_p/n." From post-layout simulations at the typical condition, the gate transition time at V_{RLB_0} is <3 ps and the injecting current I_{RLB_0} reaches 1.4 mA, as shown in Fig. 2(a). PRLCK-GEN consists of a pulse generator (PG) and a single-to-differential (S2D) circuit. The PG provides a choice of three pulse widths, controlled by PW_{CONFIG}[2:0], where 1st, 2nd, and 3rd levels, respectively, achieve 16, 19, and 25 ps to meet the injection-locking criterion of under the half LC-VCO period. S2D provides either RL_CLK or RLB_CLK or both, as controlled by CLK_RL_{CONFIG}[1:0]. However, the realigning strength can be adjusted by the combination of CLK_RL_{CONFIG}[1:0], RLS_{CONFIG}[3:0], and PW_{CONFIG}[3:0]. From simulations, the PN of VCO at 1-MHz offset is −100 dBc/Hz; however, the PN there can be improved by 10 dB, to −110 dBc/Hz after applying the setting of RLB_CLK "ON," RL_CLK "OFF," pulse width at 16 ps and one RL cell, as shown in Fig. 2(b).

Fig. 3(a) shows the proposed hybrid LC-PLL with the DCT and skew cancellation for phase realignment. The proposed DCT is integrated in the "oscillator controller" and monitors the candidate binary oscillator tuning word (band_bin[3:0]) and analog V_{TUNE}. DCT then adjusts the oscillator's thermometer tuning word (band_th[14:0]) if V_{TUNE} is out of the specified range. The limited continuous frequency TR (FTR) of the small varactor can be thus arbitrarily extended by DCT without sacrificing the *Q* factor of the LC-VCO. The CP

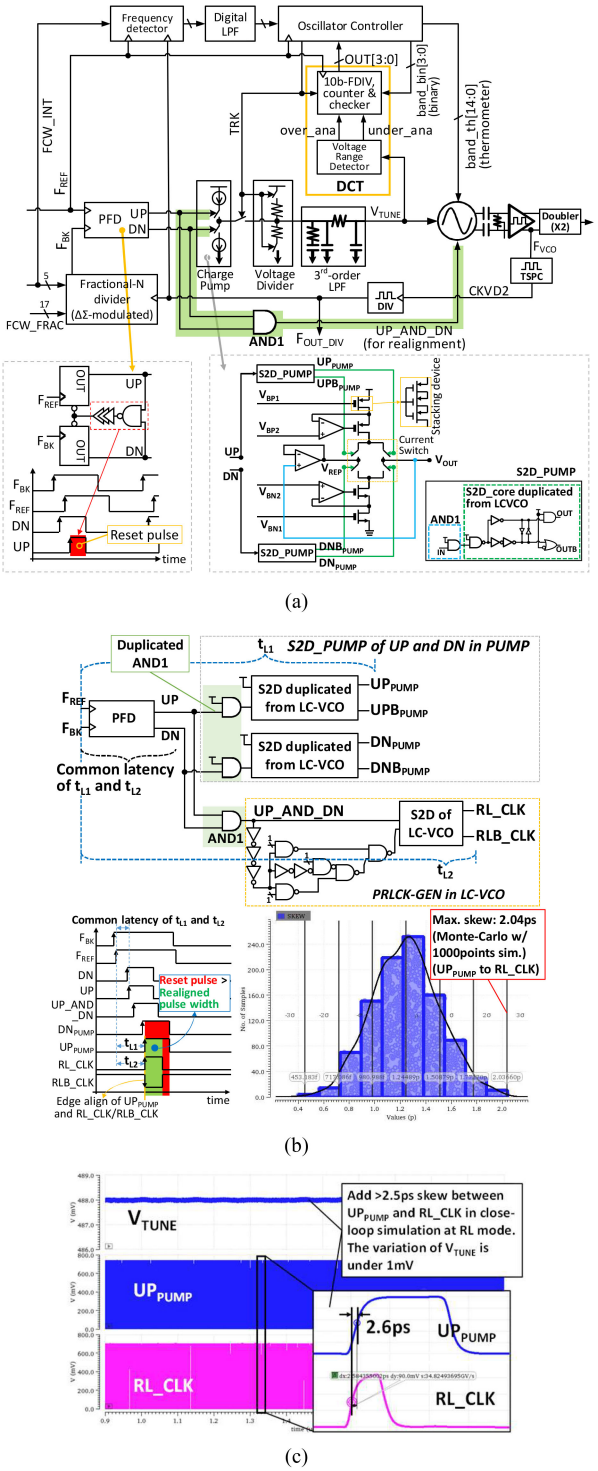

Fig. 3. Proposed LC-PLL architecture with DCT and skew cancellation: (a) block diagram, (b) timing diagram and MC simulation of skew cancellation, and (c) V_{TUNE} variation of closed loop in RL mode with 2.6-ps skew between UP_{PUMP} and RL_CLK.

uses a regulating wide-swing current mirror combined with current switching and stacking devices to ensure its PLL's in-band PN contribution is well below −100 dBc/Hz and F_{REF} is >200 MHz. The latency from F_{REF} to the UP/DN signal inside the CP (UP_{PUMP}/DN_{PUMP}), named t_{L1}, is a sum of "F_{REF} to UP/DN of PFD" and "UP/DN to UP_{PUMP}/DN_{PUMP}," where the path of "F_{REF} to UP/DN" is implemented by an auto-place-and-route (APR) and it is optimized for propagational time. In [6], an equivalent of "F_{REF} to RL/RLB of

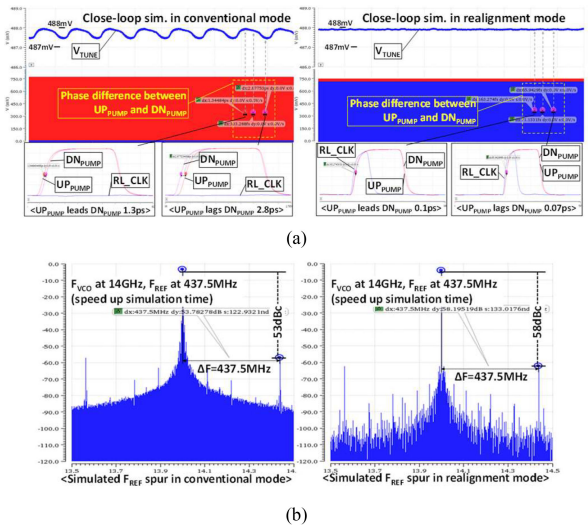

Fig. 4. Comparison between conventional and RL modes in closed-loop simulations: (a) V_{TUNE} variation and phase error of UP_{PUMP}/DN_{PUMP} and (b) simulated F_{REF} spur (left: conventional mode; right: realignment mode).

LC-VCO (RL(B)_CLK, see Fig. 1)" named t_{L2} would be adjusted by a DLL to be the same as t_{L1} for preventing the degradation of reference spurs under realignment. In the proposed skew cancellation method, as shown in Fig. 3(b), gate AND1 combines UP and DN of PFD to generate a new realigning clock (UP_AND_DN) to ignore the common latency of t_{L1} and t_{L2} and it does not require any latency matching with the APR results. However, to ensure the edge of UP_{PUMP} aligns with RL_CLK, the block S2D_PUMP of UP and DN in the CP integrates the duplicated AND1 and LC-VCO's S2D. From a 1000-point Monte Carlo (MC) simulation, the maximum skew between UP_{PUMP} and RL_CLK is 2.04 ps. Fig. 3(c) shows that the variation of V_{TUNE} is under 1 mV when forcing a 2.6-ps skew (from MC sim) into the PLL's closed-loop simulation in the realignment mode. In [4] and [5], the clock injected into the LC-VCO and the clock aligning the VCO edge are both directly derived from a very clean reference signal. However, in this work, the clock used to align the VCO edge can conveniently come from the PFD (or other combinational circuits).

Fig. 4 compares the conventional and realignment modes in closed-loop simulations. Note, to speed up the simulation time, F_{REF} is set at 437.5 MHz for a 14-GHz F_{VCO}. In the conventional mode, the PLL finely tunes the VCO frequency through the PFD, CP, and LPF during the phase tracking to finally adjust the F_{BK} edge to align with F_{REF}; after PFD, DN_{PUMP} corresponds to F_{BK}, and UP_{PUMP} corresponds to F_{REF}. However, due to the limited PLL bandwidth, DN_{PUMP} keeps on repeatedly leading and lagging UP_{PUMP} to generate the ripple of 1.3 to −2.8 ps which causes the ∼1 mV V_{TUNE} ripple, as shown in Fig. 4(a)-left, ultimately responsible for the −53-dBc F_{REF} spur in Fig. 4(b)-left. Also shown are the PLL simulation results in the realignment mode, where UP_{PUMP} and DN_{PUMP} feature a nearly "perfect" alignment (0.1–0.07-ps phase error), exhibiting fairly flat V_{TUNE}, thus lowering the F_{REF} spur by 5 dB.

The proposed DCT circuit of Fig. 5 extends the effective tunability of the narrow analog varactor for the reduced PN. DCT senses when V_{TUNE} falls outside an allowable range to flag the varactor exhausting its tunability, and accordingly increments or decrements the coarse-tuning band (expressed as band_bin), which in turn recenters V_{TUNE}. DCT comprises a voltage range detector, frequency divider (10-b FDIV) with a pause

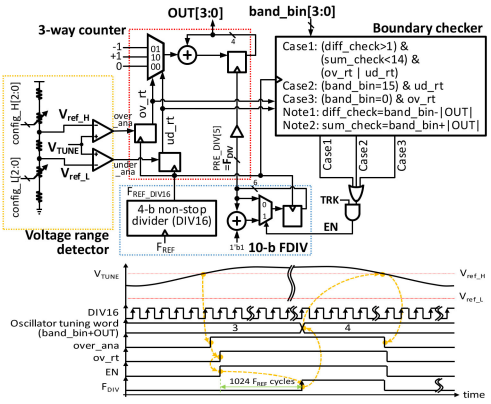

Fig. 5. Proposed DCT: schematic (all flip-flops are reset on power-up) and timing diagram.

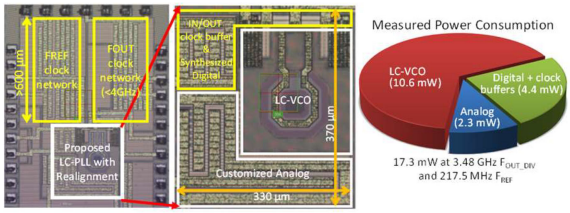

Fig. 6. Die photograph of the proposed PLL and measured power consumption.

function, 3-way counter, and boundary checker. In the voltage range detector, two comparators with low hysteresis compare V_{TUNE} against high- and low-voltage thresholds (V_{ref_H} and V_{ref_L}) generated by the programmable resistive divider. The boundary checker prevents the overflow or underflow of the final VCO tuning words by detecting "band_bin," "sum_check" (= band_bin + |OUT|) and "diff_check" (= band_bin − |OUT|); the enable signal ("EN") for the 6-b divider is released if the criteria are satisfied. The 3-way counter provides three directions of "+1," "−1," and "0," in which "0" stops counting when V_{TUNE} is between V_{ref_H} and V_{ref_L}. The 10-b FDIV is composed of a 4-b nonstop divider and a 6-b divider with a pause function, where the latter is shut down for power saving when V_{TUNE} is between V_{ref_H} and V_{ref_L}. In the DCT's timing diagram, V_{TUNE} crosses V_{ref_H} to trigger the over_ana to a high level and to enable the 6-b divider of the 10-b FDIV. After 1024 F_{REF} cycles, the oscillator tuning word [band_bin and OUT are combined in Fig. 3(a)] is increased to 4 from 3 if the V_{TUNE} is still higher than V_{ref_H}. The new oscillator tuning word increases the frequency of LC-VCO and this frequency change is detected by PFD and CP to pull down V_{TUNE}. When V_{TUNE} recenters between V_{ref_H} and V_{ref_L}, the most circuits of DCT are shut down for power saving and only the voltage range detector and 4-b nonstop divider of 10-b FDIV are active. However, in [6], the PLL would fail the lock if the initial V_{TUNE} is set at V_{DD} or V_{SS}. The above failure is readily solved by the proposed DCT.

III. Measurement Results and Conclusion

The die micrograph of the proposed LC-PLL and its power breakdown are shown in Fig. 6. The total consumed power is 17.3 mW with 10.6 mW for the LC-VCO, 2.3 mW for the analog circuits, and 4.4 mW for the digital logic and clock buffers. It is implemented in 5-nm FinFET CMOS and occupies a core area of 0.122 mm^2. The 11.9–14.4-GHz F_{VCO} is divided by 4 as F_{OUT_DIV} to be able to drive the IC pad and 50-Ω line for the measurements. In order to take advantage of a common

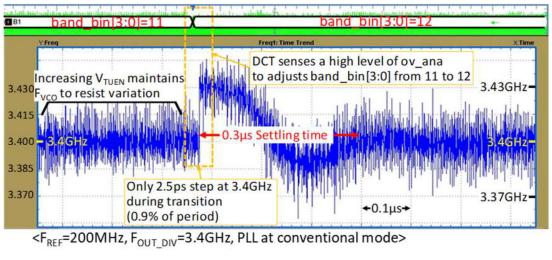

Fig. 7. Measured actuation of DCT against temperature variation.

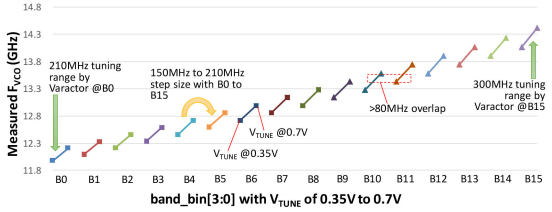

Fig. 8. Measured FTR of LC-VCO.

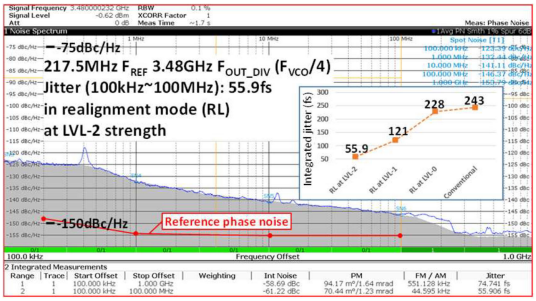

Fig. 9. Measured PN in the conventional and realignment modes with different realigning strengths (F_{REF}: R&S SMA100A signal generator).

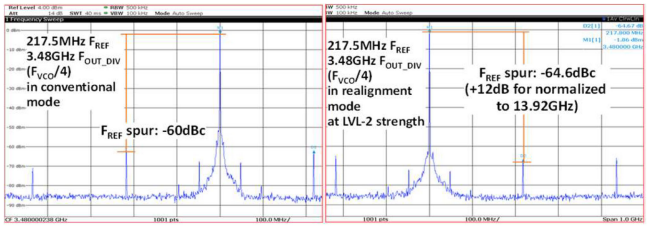

Fig. 10. Measured reference spurs in the conventional and realignment modes.

testing environment from different products and process nodes, the F_{REF} and F_{OUT_DIV} clocks are transported by the clock networks over a 600-μm distance at the test-chip level.

Fig. 7 demonstrates the measured perturbation due to the actuation of DCT against a temperature shift. In this measurement, the PLL operates in the conventional mode with 200-MHz F_{REF} and 3.4-GHz F_{OUT_DIV}. When the PLL is exposed to a temperature drift, the DCT changes band_bin from 11 to 12 and only experiences a 0.3-μs settling time for maintaining F_{OUT_DIV} at 3.4 GHz (F_{VCO} at 13.6 GHz), while merely inducing a 2.5-ps step during the transition. Fig. 8 shows the measured FTR of LC-VCO from 11.9 to 14.4 GHz. The varactor's TR at B0 and B15 (band_bin = 15) ranges from 210 to 300 MHz; the step size ranges from 150 to 210 MHz with B0–B15 and the overlap range between the frequency bands is at least 80 MHz. Fig. 9 shows the measured integrated jitter in the conventional and realignment modes with different realignment strengths in an integer-N mode. The maximum strength (denoted "LVL-2") is defined at the maximum level of realigned pulsewidth (RLPW), realignment strength (RLS), and RL(B)_CLK "on"; the "LVL-1" is defined at the middle level of RLPW, RLS, and RL(B)_CLK on; and the "LVL-0" is defined at the minimum level of RLPW, RLS, and RLB_CLK on/RL_CLK "off." However, the LC-PLL with the LVL-2, LVL-1, and LVL-0 achieves the integrated jitter of 55.9, 121, and 228 fs, respectively; the LC-PLL in conventional mode achieves 243 fs. Fig. 10 shows the measured spectrum with reference spurs in the conventional and realignment modes. The reference spur is −48 and −52.4 dBc in the conventional and realignment modes, respectively, when normalized to the F_{VCO} carrier frequency. Table I compares the proposed hybrid LC-PLL with published state of the art.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TO STATE OF THE ART

	This Work	[9]	[2]	[7]	[8]
Technology	5nm	65nm	28nm	28nm	28nm
Architecture (LC-PLL)	Hybrid Realignment	Digital Injection	Digital Charge-Sharing	Digital BB-PD	Analog Sampling
F_{REF} (MHz)	217.5	125	250	500	500
F_{VCO} (GHz)	11.9 to 14.4	6.75 to 8.25	21.7 to 26.5	12.8 to 15.2	11.9 to 14.1
Bandwidth (MHz)	3	0.2	0.3	2	10
F_{REF} spur (dBc)	-52.4 (*)	-43	-45	-80.1	-73.5
Power consumption (mW)	17.3	3.25	16.5	19.8	18
Dimension (um^2)	330 X 370	420 X 650	920 X 960	570 X 300	570 X 310
Integrated jitter (fs)	55.9	105	75.9	59	51.7
Integrated range (Hz)	100k to 100M	10k to 30M	10k to 30M	1k to 100M	1k to 100M
FoM* (dB)	-252.7	-254.4	-250.2	-251.6	-253.2

FoM: $10*\log(\sigma_{Jitter}{}^2 * P_{DC}/1mW)$, (*): normalized to carrier frequency*

In this work, we exploit a new paradigm in designing PLLs: the devices in advanced FinFET CMOS are much more nonlinear and noisy but are significantly faster. They are more difficult to use for analog and RF circuits, yet their digital capabilities are unmatched. Hence, we exploit the time-domain techniques, such as the realignment of a (noisy) oscillator by super-sharp and ultranarrow pulses derived from the reference clock. The resulting PLL achieves the best-in-class integrated jitter and FoM of 55.9 fs and −252.7 dB, respectively.

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