A Millimeter-Wave ADPLL With Reference Oversampling and Third-Harmonic Extraction Featuring High FoM$_{\text{jitter-N}}$

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Abstract—This letter proposes a mm-wave fractional-N reference-oversampling (ROS) all-digital phase-locked loop (ADPLL) for 5G wireless applications utilizing a relatively low but standard reference frequency. The 4× ROS phase detector (PD) increases the phase-detection rate 4× in a power-efficient manner in order to reduce the in-band phase noise contributed from the PD. This improves the overall figure of merit (FoM) and locking speed. A class-F$_3$ oscillator generates both ~10 GHz and its third harmonic. The former is fed to the feedback divider, while the latter is extracted to generate the ~30-GHz output. The fractional phase and reference distortions are compensated in digital with the assistance of DACs. The proposed ROS-ADPLL is implemented in 28-nm CMOS. Using a standard 50-MHz reference frequency, it achieves 237-fs rms jitter while consuming only 11.9 mW, reaching best-in-class FoM$_{\text{jitter-N}}$ of −269.3 dB.

Index Terms—All-digital phase-locked loop (ADPLL), fifth-generation (5G), low jitter, low power, reference oversampling (ROS), SAR ADC.

I. INTRODUCTION

To support the ever-increasing data rates of wireless communications, the fifth-generation (5G) mobile systems target new frequencies in the 24–40-GHz mm-wave (mmW) bands, promoting wide bandwidth and high-order modulation (e.g., 64/256 QAM). However, this puts an enormous burden on frequency synthesizers to ensure low spurious emissions while consuming limited power. The phase noise (PN) of a phase-locked loop (PLL) is contributed by 1) in-band PN, dominated by the reference signal and phase detector (PD), and 2) out-of-band PN, dominated by the oscillator. PN of the reference low-noise buffer (LNB)/slicer and PD is strictly dependent on its power budget and is upconverted to the mmW PN with the PLL multiplication factor N, resulting in high in-band PN in low-power mmW PLLs.

To achieve low jitter with high power efficiency, leading to a high figure of merit (FoM), subsampling/bang-bang (SS/BB) PDs are usually adopted [1]–[3]. They exploit the intrinsically high time-to-voltage gain provided by the high slope of the oscillator waveform and sharp edges of the reference clock to reduce the PD noise at the expense of a narrow locking range. As the sampling clock of the comparator input, the reference signal S_{ref} needs to translate its "gentle" sinusoidal waveform into sharp edges through an LNB, but that consumes significant power. To reduce the PD noise contribution to the output, a higher reference frequency (f_{ref}) is typically employed as it gives lower N [2]. However, a >100-MHz low-PN
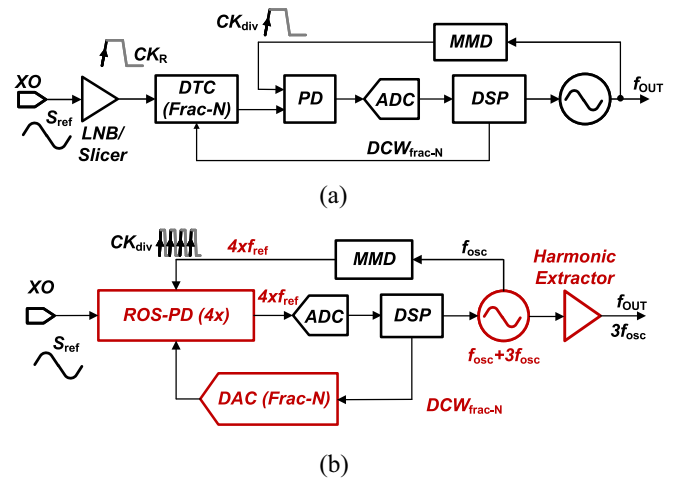
Fig. 1.   (a) Conventional DTC-based fractional-N PLL. (b) Proposed mmW ADPLL adopting a 4× ROS and class-F$_3$ oscillator with harmonic extraction (the blocks highlighted in red are detailed in this letter).

crystal oscillator (XO) burns high power and costs more than the standard 40/50 MHz ones. Even higher reference frequencies (e.g., 500 and 800 MHz) will require an additional reference doubler/quadrupler or cascaded PLLs, likely necessitating a duty-cycle calibration [4]. Alternatively, the information contained in the reference sinusoidal XO waveform, S_{ref}, can be extracted by sampling it by the oscillator clock edges [5], [6]. This allows to increase the PD rate, consequently N, by oversampling [7]–[10].

In this letter, we propose an mmW fractional-N all-digital PLL (ADPLL), shown in Fig. 1(b), which exploits the reference waveform oversampling (ROS) PD and class-F$_3$ digitally controlled oscillator (DCO) with third-harmonic extraction (H3E) to boost the multiplication number N while using a standard 50-MHz XO [9]. The prototype is fabricated in 28-nm CMOS and produces low 237-fs rms jitter while consuming only 11.9 mW.

II. PHASE DETECTOR NOISE IN SUBSAMPLING VERSUS REFERENCE SAMPLING/OVERSAMPLING PLLs

Fig. 2 shows the detailed considerations of PN associated with the subsampling PD (SS-PD) and reference-sampling PD (RS-PD) when using a standard XO providing a sinusoidal waveform as the reference [3], [6]. Assuming an ideal reference clock edge (CK$_R$), the PD noise in SS-PD can be kept negligible [1]. This is because the sampled thermal voltage noise and input-referred noise (IRN) of the gain stage G are converted to time jitter through a steep slope of $2\pi A_{\text{osc}} f_{\text{osc}}$, where A_{osc} and f_{osc} are the oscillator's output amplitude and frequency. Note that the LNB plays an important role in translating the relatively slow sinusoidal input waveform into "super"-sharp clock edges for sampling but the consideration of the on-chip
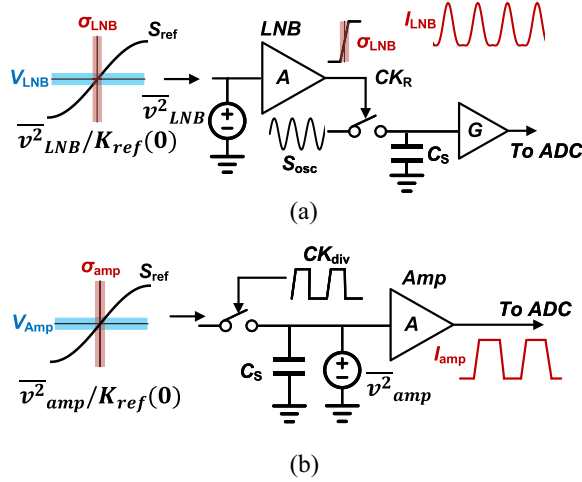
Fig. 2. Comparison of PN contributions in (a) SS-PD and (b) RS-PD.

TABLE I
SINGLE SAMPLING VERSUS 4× OVERSAMPLING

Para.	Single Sampling Equation	Single Sampling Value	4x Oversampling Equation	4x Oversampling Value
$I_{D,rms}$	$\gamma I_{D,rms}$	I_1	$4\gamma I_{D,rms}$	$4I_1$
σ_{amp}	$\dfrac{\overline{v}_{amp}}{2\pi A f_{ref}}$	σ_{amp1}	$\dfrac{\overline{v}_{amp}}{2\pi A f_{ref}\sin\frac{\pi}{4}}$ *	$\sqrt{2}\sigma_{amp1}$
σ_{t-amp}	$\dfrac{\overline{v}_{amp}}{2\pi A f_{ref}\sqrt{f_{ref}}}$	σ_{t-amp1}	$\dfrac{\sqrt{2}\overline{v}_{amp}}{2\pi A f_{ref}\sqrt{4f_{ref}}}$	$\dfrac{\sqrt{2}}{2}\sigma_{t-amp1}$
P_{PD}	$\gamma V_{DD} I_{D,rms}$	P_{PD1}	$4\gamma V_{DD} I_{D,rms}$	$4P_{PD1}$
σ_t^2 **	$\sigma_{PD}^2 + \sigma_{OSC}^2$	σ_{t1}^2	$\dfrac{1}{2}\sigma_{PD}^2 + \sigma_{OSC}^2$	$\dfrac{3}{4}\sigma_{t1}^2$
P_{DC}	$P_{PD} + P_{HS}$	P_{DC1}	$4P_{PD} + P_{HS}$	$P_{DC1} + 3P_{PD}$

*4x Oversampling PD samples the slope at four ± π/4 positions
**Under optimum bandwidth, the jitter contributed by PD and OSC are equal.

Fig. 3. Detailed implementation of (a) proposed reference 4× oversampling PD and (b) its corresponding waveforms.

Fig. 4. Schematics of (a) class-F$_3$ DCO and (b) third-harmonic extractor ($M_{3,4}$) and output buffer ($M_{5,6}$).

LNB is usually neglected. The IRN of the LNB ($\overline{v^2}_{LNB}$) can actually dominate the SS-PD jitter due to the gentle slope of $2\pi A_{ref}f_{ref}$, where A_{ref} is the reference waveform amplitude. The total PD jitter in SS-PD can be derived as

$$\sigma_{SSPD}^2 = \frac{\overline{v^2}_{LNB}}{(2\pi A_{ref}f_{ref})^2} + \frac{KT/C_S + \overline{v^2}_{IRN-G}}{(2\pi A_{osc}f_{osc})^2}. \quad (1)$$

In contrast, in RS-PD [Fig. 2(b)], the sampling clock is obtained from the multimodulus divider (MMD) in the oscillator feedback path (CK$_{div}$), which naturally features sharp edges. The reference sinusoidal waveform is now directly sampled with the sampling capacitor C_S without any buffer. Due to the slow slope of $2\pi A_{ref}f_{ref}$ in the incoming S_{ref}, an isolation buffer is employed with amplification A to help with quantization noise downstream. The total jitter in RS-PD can be derived as

$$\sigma_{RSPD}^2 = \frac{\overline{v^2}_{amp} + KT/C_S}{(2\pi A_{ref}f_{ref})^2} \quad (2)$$

where $\overline{v^2}_{amp}$ is the IRN of the amplifier. When using a sufficiently large capacitor C_S (~pF), its thermal noise can be neglected compared to the IRN of LNB or Amp. The PD noise will affect the PLLs output PN with a factor of $N_L = f_{out}/f_{PD}$, where f_{PD} ($= f_{ref}$ in this case) is the phase-detection rate. The output jitter contributed by the SS-PD and RS-PD can be derived as

$$\begin{cases} \sigma_{t\text{-}SSPD}^2 \approx \dfrac{\overline{v^2}_{LNB}}{f_{ref}} \cdot \dfrac{f_{out}}{4\pi^2 A_{ref}^2 f_{ref}^2} \\ \sigma_{t\text{-}RSPD}^2 \approx \dfrac{\overline{v^2}_{amp}}{f_{PD}} \cdot \dfrac{f_{out}}{4\pi^2 A_{ref}^2 f_{ref}^2}. \end{cases} \quad (3)$$

It can be observed that jitter in both SS-PD and RS-PD can be dominated by the LNB and Amp, respectively. Therefore, the jitter and power consumptions of both architectures are fundamentally the same.

The RS-PD architecture has been recently gaining interest thanks to its natural capability of beneficially [see (3)] increasing the phase-detection rate f_{PD} beyond f_{ref} [7], [8]. In this work, a 4× oversampling chooses four points at $\pm\pi/4$, $\pm3\pi/4$ positions on S_{ref}, which keep the PD gain (i.e., sampling slope) at $\sqrt{2}A_{ref}f_{ref}$. Taking advantage of the 4× PD rate, the output jitter in ROS-PD is

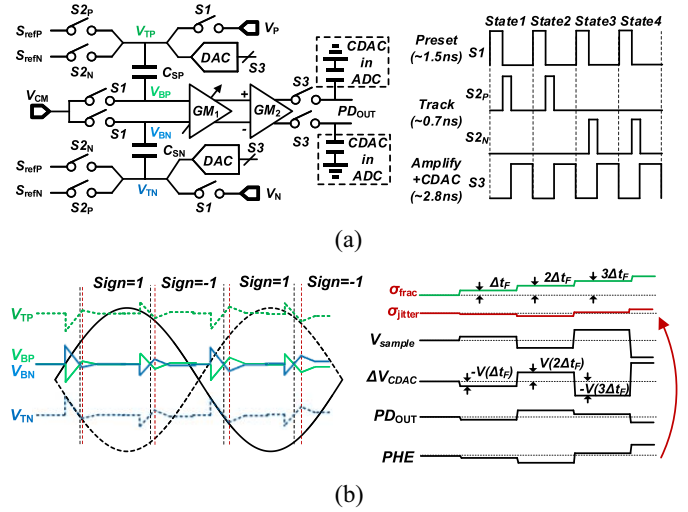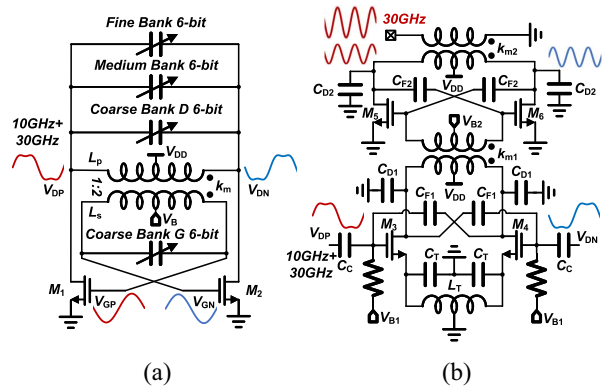$$\sigma_{t\text{-}ROSPD}^2 \approx \frac{\overline{v^2}_{amp}}{4f_{ref}} \cdot \frac{f_{out}}{2\pi^2 A_{ref}^2 f_{ref}^2}. \quad (4)$$

The net result is a 2× improvement in jitter power compared to a single-sampling RS-PD. Table I summarizes the theoretical jitter and power consumption numbers in the 1× sampling and 4× oversampling PLLs. Under the 4× ROS, the Amp consumes 4× higher power. The Amp amplifies the sampled voltage and charges the ADC's capacitor. This operation can be gated off outside of the tracking phase, thereby allowing a power saving by a factor γ (i.e., 0.5 in this work). Comparing FoM$_{jitter}$ in Table I, which is defined as $10\log_{10}(\sigma_t^2) + 10\log_{10}(P_{DC})$[1], the first jitter term in ROS-PD is lowered by a factor of 1/4 (-1.25 dB), while the second power
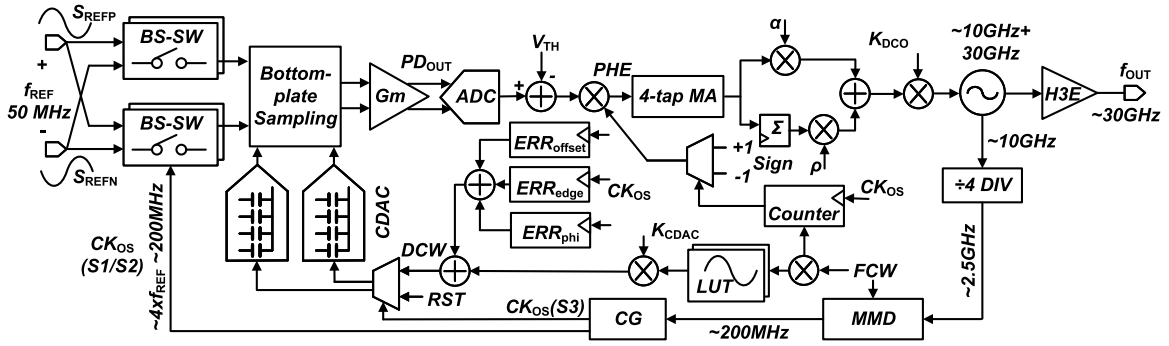
Fig. 5.   Top-level diagram of the proposed ROS ADPLL.

term is increased by $10 \log_{10}(1 + 3\beta)$, where $\beta = P_{PD}/P_{DC}$ represents the fraction of the *full* PD path power to the total. In this work, $P_{PD} \approx 0.22$ mW (PD, ADC, and digital) of the $1\times$ sampling and $P_{DC} \approx 12$ mW. As a result, the FoM$_{jitter}$ improvement can be $1.25 - 10 \log_{10}(1 + 3 \cdot 0.22/12) = 1.01$ dB.

III. PROPOSED ARCHITECTURE

A. Reference $4\times$ Oversampling Phase Detector

A simplified schematic of the ROS-PD is shown in Fig. 3. The $4\times$ oversampling is achieved by sampling S_{ref} at the angles of $\pi/4$, $3\pi/4$, $5\pi/4$, and $7\pi/4$. There are three PD operational phases. 1) The top and bottom plates of sampling capacitors C_{SP} (C_{SN}) are, respectively, preset to V_P (V_N) with the expected value of $V_{CM} \pm A_{ref} \sin(\pi/4)$ and V_{CM}, where $V_{CM} = 0.5$ V is the common-mode (CM) voltage of the reference waveform. 2) The differential reference waveforms, S_{refP}, S_{refN}, are directly sampled by bootstrapped switches, S2$_P$, S2$_N$. By means of the bottom-plate sampling, the bottom-plate voltages V_{BP} (V_{BN}) follow the same trajectory as V_{TP} (V_{TN}) with different dc voltage levels. 3) Two-stage amplifier consisting of GM$_{1,2}$ amplifies the sampled voltage and charges it into the DAC's capacitor of the subsequent SAR-ADC. In the meantime, the capacitive DACs (CDAC) connected to the top plates (V_{TP}, V_{TN}) are adjusted through the DAC code to compensate for the accumulated fractional voltage and preset errors [see Fig. 3(b)]. Due to the different sampling positions along the waveform, the sign of the digitized phase error (PHE) is compensated in the digital domain.

B. Class-F_3 DCO and Third-Harmonic Extractor

The sampling clocks for the PD are generated from the divided DCO output by means of the MMD [see Fig. 1(a)]. A $\sim$30-GHz divider would consume high power and it might require an additional bulky passive inductor. Therefore, we chose a class-F_3 DCO operating at $\sim$10 GHz but which also inherently generates a third harmonic by properly setting the primary and secondary tanks, as shown in Fig. 4(a) [11]. The gate node voltages (V_{GP}, V_{GN}) exhibit a large amplitude of the $\sim$10-GHz fundamental waveform, which is fed into MMD. On the other hand, the drain nodes (V_{DP}, V_{DN}) are ac-coupled to the subsequent H3E [see Fig. 4(b)]. This keeps the MMD input frequency at $\sim$10 GHz, thus operating at much lower power as an inductor-less structure. The LC-tank at the drain of M$_{3,4}$ exhibits a high differential impedance at $\sim$30 GHz to amplify the third-harmonic component in V$_{DP}$ and V$_{DN}$, while a common-source tank is implemented by L_T and C_{CT}. This provides a high impedance at the fundamental $\sim$10 GHz, preventing the $\sim$10-GHz current flow. As a result, the fundamental component can be attenuated [12]. The second-stage nMOS-based buffer is used for further amplifying the $\sim$30-GHz signal and for driving the 50-Ω measurement equipment.

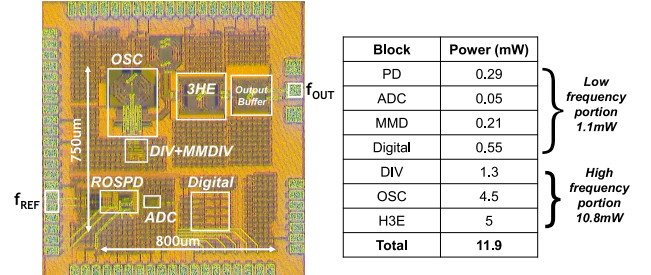
Fig. 6.   Chip photograph and power breakdown of the ROS-ADPLL.

C. Proposed Fractional-N ADPLL With ROS-PD and H3E

The top diagram of ADPLL is shown in Fig. 5. After quantizing the PD output by a SAR-ADC, the PHE is calculated in the digital signal processor, which includes the programmable proportional and integral (PI) loop filter and the DCO gain normalization K_{DCO}. The FCW controls the MMD and the accumulated fractional phase which is fed into a preprogrammed sinusoidal lookup table (LUT) to generate the corresponding fractional DAC-controlling word DCW$_{frac}$. The periodic error patterns arising from a nonideal reference waveform are preestimated in the ERR compensation block and added to DCW$_{frac}$ [9].

IV. EXPERIMENTAL RESULTS

The proposed mmW ROS-ADPLL was fabricated in TSMC 28-nm LP CMOS. Fig. 6 shows the chip microphotograph. The active area is $\sim$0.3 mm^2 and the total power consumption P_{DC} is 11.9 mW under a 1-V supply (except for the DCO and H3E, which run at 0.6 V), where the high-frequency portion (DCO, H3E, and divider) consumes 90% of the total P_{DC}. A standard 50-MHz XO (Crystek CVSS-945) is used as the reference. Fig. 7(a) and (b) shows the PN in integer-N ($\sim$28.8 GHz) and fractional-N ($\sim$28.809275 GHz) modes, respectively, with rms jitter of 199 and 237 fs. The worst-case fractional spur is -40 dBc. After applying the CDAC-assisted calibration and MA filter, the reference spur and its harmonics are reduced below -65 dBc [Fig. 7(c)]. Thanks to the large monotonic range of the ROS-PD, the proposed ADPLL can provide robust locking and settles within 15 μs in face of a 62-MHz frequency step [Fig. 7(d)]. Due to the ROS-PD and H3E techniques, our system achieves an FoM of -241.7 dB with a large N of 576. The proposed techniques enable to break through the FoM-versus-N barrier shown in Fig. 8 for the state-of-the-art landscape of PLLs with large N. Compared with other >10-GHz digital PLLs in Table II, this work achieves excellent FoM while consuming lower power. The large value of N brings the FoM$_{jitter-N}$ to a record number of -269.3 dB for single-stage PLLs.

TABLE II
COMPARISON TABLE OF STATE-OF-THE-ART FRACTIONAL-N DIGITAL PLLs

	This work	Santiccioli, ISSCC'20	Liao, JSSC'20	Grimaldi, ISSCC'19	Weyer, ISSCC'18	EK, JSSC'18	Hussein, ISSCC'17	Kim, ISSCC'19
Architecture	4xROS-PD+ Class-F$_3$+H3E	BBPD +DTC	RSPLL +ILFM	Digital SSPD	ADPLL	Analog PLL	ADPLL	Digital SSPLL+IL
Cascading PLLs?	No	No	Yes	No	No	No	No	Yes
FLL Required?	No	Yes	No	Yes	Yes	No	Yes	Yes
Tech (nm)	28	28	45	65	40	28	65	65
Ref (MHz)	50	500	80	100	120	491.5	100	100
Freq. (GHz)	24-31	12.8-15.2	33.6-36	30.6-34.2	36.3-38.2	23.3-30.2	50-64.8	28-31
N	576	27	448	306	317	53	656	285
Jitter (fs)	237	66	251	197	577	115.6	223	76
Power (mW)	11.9	19.8	20.6	35	68	31	46	41.8
FoM$_{\text{jitter}}$ (dB)	-241.7	-250.6	-238.9	-238.6	-226.4	-244	-236.5	-246.1*
FoM$_{\text{jitter-N}}$(dB)	-269.3	-265.2	-265.3	-263.65	-251.5	-261	-264.6	-270.6*
Ref. spur (dBc)	-65	-73.5	-60	NA	-55	-65	-59	-58
Frac. Spur (dBc)	-40	-61	N.A.	-42.2	N.A.	-30	-54.6	N.A.
Area (mm^2)	0.3	0.1	0.41	0.55	0.18	0.11	0.45	0.32

FoM$_{\text{jitter}}$=10log($\sigma_t^2 P_{DC}$/1mW)   FoM$_{\text{jitter-N}}$=FoM$_{\text{jitter}}$+10log(f_{ref}/f_{out})   *Integer-N
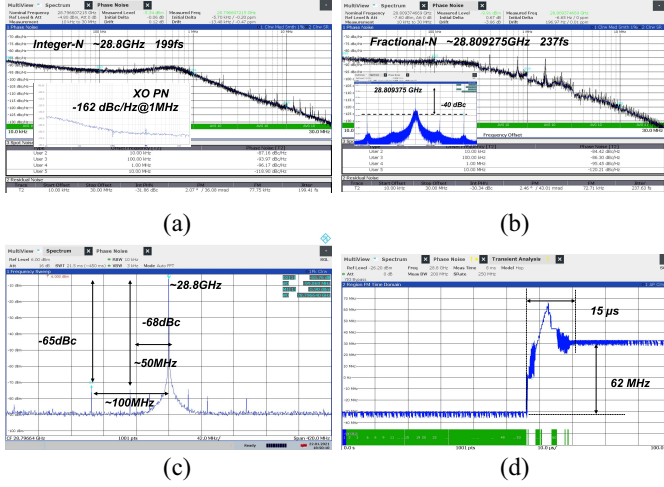

Fig. 7. Measured plots by R&S FSW signal and spectrum analyzer: (a) integer-*N* PN (insert: PN of XO at 49.993 MHz); (b) fractional-*N* PN (insert: close-in spectrum); (c) integer-*N* mode spectrum; and (d) relocking behavior.
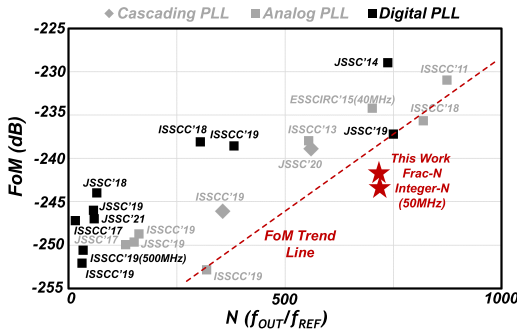

Fig. 8. Landscape of state-of-the-art RF/mmW PLLs.

V. CONCLUSION

In this letter, we show that a reference-sampling-PD can fundamentally achieve the same FoM as in the subsampling PLLs. The FoM can be further improved by employing oversampling in the PD. The proposed mmW ROS ADPLL attains excellent FoM$_{\text{jitter}}$ under a standard 50-MHz reference frequency, thus tolerating a large frequency multiplication ratio $N \approx 600$. A class-F$_3$ DCO followed

by a third-harmonic extractor simultaneously generates the ~30-GHz output and ~10-GHz feedback clock to improve the power efficiency of the high-speed circuits. The entire ADPLL consumes 11.9 mW leading to an FoM$_{\text{jitter-N}}$ of −269.3 dB.

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