Correction to "A 32–42-GHz RTWO-Based Frequency Quadrupler Achieving >37 dBc Harmonic Rejection in 22-nm FD-SOI"

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IN THE above article [1], Fig. 1 was incorrectly provided. The correct figure and full caption appear here.

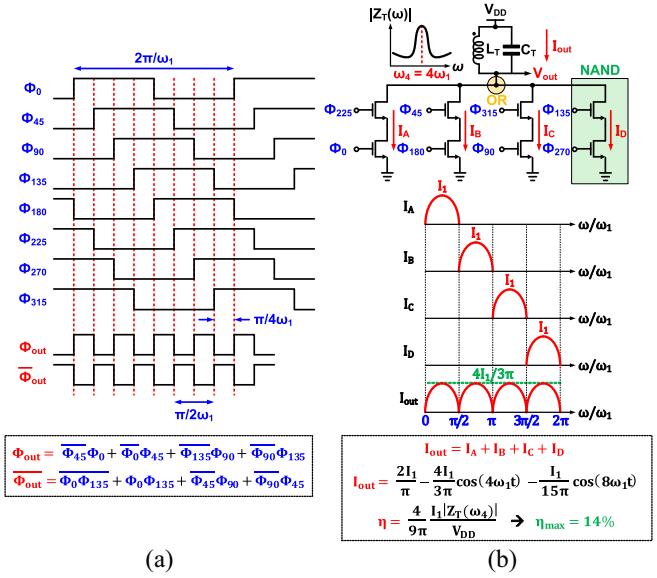

Fig. 1. Logic-based frequency quadrupler: (a) operation and (b) conceptual single-ended implementation.

REFERENCE

[1] M. A. Shehata, V. Roy, J. Breslin, H. Shanan, M. Keaveney, and R. B. Staszewski, "A 32–42-GHz RTWO-based frequency quadrupler achieving >37 dBc harmonic rejection in 22-nm FD-SOI," *IEEE Solid-State Circuits Lett.*, vol. 4, pp. 72–75, 2021, doi: 10.1109/LSSC.2021.3055628.

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