A 3.2-to-3.8 GHz Harmonic-Mixer-Based Dual-Feedback Fractional-N PLL Achieving −65 dBc In-Band Fractional Spur

Masaru Osada, *Graduate Student Member, IEEE*, Zule Xu, *Member, IEEE*, and Tetsuya Iizuka, *Senior Member, IEEE*

***Abstract*—A harmonic-mixer-based dual-feedback loop architecture for fractional frequency synthesis is proposed in this letter. By performing frequency subtraction instead of frequency division by using the harmonic mixer in the feedback path, the proposed phase-locked loop (PLL) achieves a unity feedback coefficient, which avoids ΔΣ noise amplification by the loop. This leads to low phase noise and low spurs without the use of complex calibration schemes. The proposed architecture is demonstrated with a 3.2-to-3.8 GHz fractional-N PLL prototype in a 65-nm bulk CMOS process that achieves a worst-case in-band fractional spur of −65 dBc.**

***Index Terms*—ΔΣ noise, cascaded phase-locked loop (PLL), dual feedback, fractional spurs, fractional-N PLL, harmonic mixer (HM), noise amplification.**

I. Introduction

Fractional-N frequency synthesizers are commonly used in applications, such as wireless communications where high-resolution control of the carrier frequency is essential. However, the design of fractional-N phase-locked loops (PLLs) generally faces two issues: 1) phase noise peaking due to the shaped quantization noise from the ΔΣ modulator (DSM) in the multimodulus divider (MMD) and 2) in-band fractional spurs caused by the quantization noise interacting with the charge-pump (CP) nonlinearity [1]. Suppressing these forms of noise is not a trivial task. Employing a narrow PLL bandwidth to suppress the quantization noise results in less suppression of the VCO phase noise, while the fractional spurs cannot be filtered out easily because of their low offset frequency.

Many different approaches have been proposed to tackle these issues. Works such as [2]–[4] attempt to cancel the deterministic noise from the DSM by using a current DAC [2] or by using a digital-to-time converter [3], [4]. This approach requires gain matching as well as high linearity for the circuit components, which leads to complex calibration schemes, such as a least mean square (LMS) algorithm.

Although a cascade of integer-N and fractional-N PLLs can be used to raise the operating frequency of the DSM to achieve better noise shaping [5], this makes it difficult to increase the bit length and the order of the DSM. In addition, as the quantization step of the DSM in the second-stage PLL increases due to the reduced division ratio, the in-band fractional spurs caused by the loop nonlinearity remains unresolved with this approach.

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Masaru Osada is with the Department of Electrical Engineering and Information Systems, University of Tokyo, Tokyo 113-0032, Japan (e-mail: osada@silicon.u-tokyo.ac.jp).

Zule Xu and Tetsuya Iizuka are with Systems Design Lab, School of Engineering, University of Tokyo, Tokyo 113-0032, Japan (e-mail: xuzule@vdec.u-tokyo.ac.jp; iizuka@vdec.u-tokyo.ac.jp).

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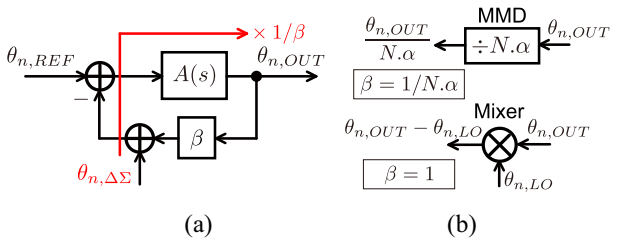

Fig. 1. (a) Noise amplification in a feedback system and (b) two different ways of performing feedback: an MMD with $\beta = 1/N.\alpha$ and a mixer with $\beta = 1$.

Adding deliberate randomization to lower the periodicity of a signal can be used to lower fractional spurs. Ho and Chen [6] take advantage of this fact by using reference dithering. This approach, however, could lead to high power consumption and design complexity that comes with the circuitry required to perform dither noise cancelation.

Avoiding noise amplification is another possible approach. As illustrated in Fig. 1(a), any noise generated at the input node of a feedback system is amplified by the inverse of the feedback coefficient when the feedforward gain is sufficiently large. This is why the ΔΣ noise and the fractional spur are amplified by the division ratio $N.\alpha$ in a typical fractional-N PLL with MMD feedback. However, as in a frequency-translation loop or an offset PLL [7], if the feedback can somehow perform frequency subtraction using a mixer, for example, the feedback coefficient can be made unity as shown in Fig. 1(b), which means that we no longer have the noise amplification. The triple-loop architecture proposed in [8] takes advantage of this concept and achieves low phase noise and spurs without complex calibration schemes. The drawback of the triple-loop architecture is the need for two auxiliary PLLs, which can lead to increased power, area, and design complexity.

This letter proposes a harmonic-mixer-based dual feedback loop architecture for fractional-N PLLs that can avoid the noise amplification using only a single auxiliary PLL with no complex calibration schemes, such as the LMS algorithm [9]. With the proposed loop architecture, low phase noise and low fractional spurs are achieved in an efficient and robust manner.

II. Proposed Architecture

A block diagram of the proposed dual-feedback architecture is shown in Fig. 2. The output signal of the PLL is fed to two feedback paths; one based on frequency division using an MMD, and the other based on frequency subtraction using a harmonic mixer (HM). A cascade of a static frequency divider N_I and the HM is used in lieu of a simple mixer in order to separate the VCO frequencies of the main PLL and the auxiliary PLL so as to avoid frequency pulling that can occur if the two frequencies are too close to each other [8].

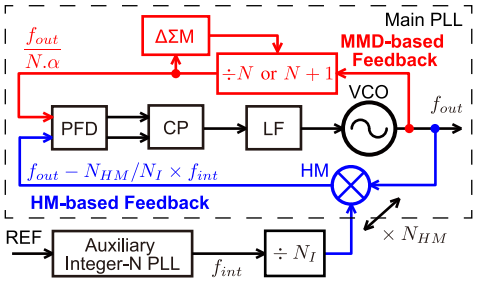

Fig. 2. Block diagram of the proposed architecture.

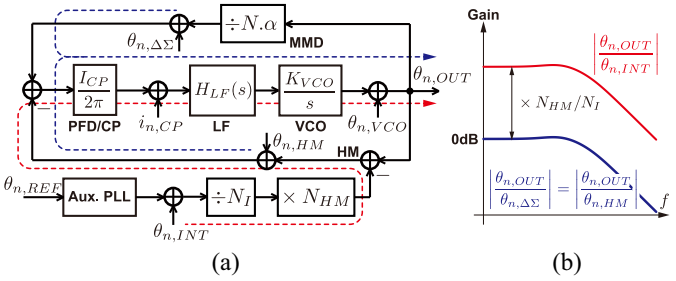

Fig. 3. (a) Linear model of the proposed architecture with some key noise sources and (b) transfer functions from $\theta_{n,\Delta\Sigma}$, $\theta_{n,\mathrm{HM}}$, and $\theta_{n,\mathrm{INT}}$ to the output.

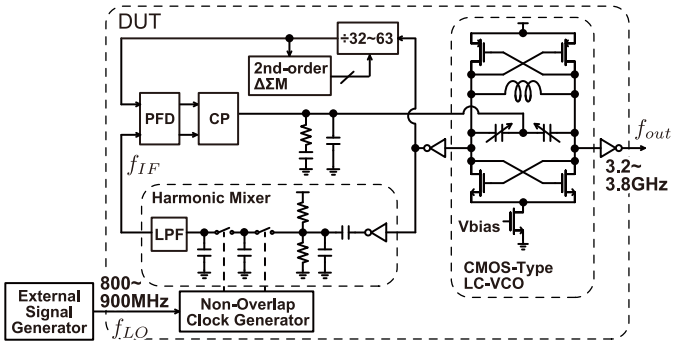

Fig. 4. Detailed block diagram of the prototype.

The PLL locks when the signals from the two feedback paths have the same frequency. Therefore, the output frequency f_{out} is given by

$$\frac{f_{\mathrm{out}}}{N.\alpha} = f_{\mathrm{out}} - \frac{N_{\mathrm{HM}}}{N_I} f_{\mathrm{int}} \Rightarrow f_{\mathrm{out}} = \frac{N_{\mathrm{HM}}}{N_I}\frac{N.\alpha}{N.\alpha - 1} f_{\mathrm{int}} \tag{1}$$

where f_{out}, f_{int}, $N.\alpha$, N_I, and N_{HM} respectively denote the main PLL output frequency, the auxiliary integer-N PLL output frequency, the effective division ratio of the MMD, the division ratio of the static divider, and the harmonic index used in the HM. The detail of the HM operation will be explained in Section III.

A linear model of the proposed PLL with some key noise sources is illustrated in Fig. 3(a). The phase noise fed back from the output $\theta_{n,\mathrm{OUT}}$ to the PFD is given by $(1-1/N.\alpha)\theta_{n,\mathrm{OUT}}$, thus the feedback coefficient of this system is recognized as $\beta = 1 - 1/N.\alpha \approx 1$. In other words, the MMD-based feedback allows fractional frequency synthesis, while the noise amplification is avoided because the feedback gain is dominated by the HM-based feedback, which is unity. Since the frequency change through the HM feedback path is $\times N$ larger than that in the conventional loop, the lock-in process of the proposed loop tends to take more time for a large frequency shift as it may lead to nonidealities, such as cycle slips. This can be mitigated by an additional coarse tuning loop if fast lock-in is necessary.

The noise transfer functions from $\theta_{n,\Delta\Sigma}$ and $i_{n,\mathrm{CP}}$ to the output phase noise $\theta_{n,\mathrm{OUT}}$ are, respectively, given by

$$\frac{\theta_{n,\mathrm{OUT}}}{\theta_{n,\Delta\Sigma}} = \frac{N.\alpha}{N.\alpha - 1}\frac{H_{ol}(s)}{1+H_{ol}(s)} \approx \frac{H_{ol}(s)}{1+H_{ol}(s)} \quad \text{and} \tag{2}$$

$$\frac{\theta_{n,\mathrm{OUT}}}{i_{n,\mathrm{CP}}} = \frac{2\pi}{I_{\mathrm{CP}}}\frac{N.\alpha}{N.\alpha - 1}\frac{H_{ol}(s)}{1+H_{ol}(s)} \approx \frac{2\pi}{I_{\mathrm{CP}}}\frac{H_{ol}(s)}{1+H_{ol}(s)} \tag{3}$$

where $\theta_{n,\Delta\Sigma}$ is the quantization noise from the DSM, $i_{n,\mathrm{CP}}$ is the noise generated by the CP and $H_{ol}(s) \triangleq (I_{\mathrm{CP}}/2\pi)H_{\mathrm{LF}}(s)(K_{\mathrm{VCO}}/s)(1 - 1/N.\alpha)$ is the open-loop gain. Equation (2) proves that the quantization noise from the DSM is not amplified at the output as the blue line in Fig. 3(b) has 0 dB DC gain. This means that the proposed PLL can achieve phase noise contribution from the DSM that is $N.\alpha - 1$ times lower than that in the conventional fractional-N PLL. Equation (3) shows that the noise generated in the CP is not amplified either. Since the noise source $i_{n,\mathrm{CP}}$ contains nonlinearity-induced fractional spurs and reference spurs due to the nonideal operation of both the PFD and the CP, the proposed PLL can achieve $N.\alpha - 1$ times lower spurs than the conventional fractional-N PLL.

The noise transfer function from the phase noise of the auxiliary integer-N PLL $\theta_{n,\mathrm{INT}}$ to $\theta_{n,\mathrm{OUT}}$ has the same frequency response as (2) except that it is multiplied by N_{HM}/N_I as shown in Fig. 3(b) with the red line. Thus, the phase noise of the auxiliary PLL goes through the low-pass filtering function of the main PLL. This implies that any out-of-band spurs contained in $\theta_{n,INT}$ are heavily attenuated at the output. Since the auxiliary PLL is an integer-N, it is relatively straightforward to achieve a wide bandwidth [10]. Therefore, by making the bandwidth of the auxiliary PLL sufficiently wider than that of the main PLL, it is possible to filter out a large portion of $\theta_{n,\mathrm{INT}}$ so that the phase noise contribution from the auxiliary PLL is negligible, and to achieve low phase noise without consuming a large amount of power.

The HM contributes kT/C noise and potentially some in-band tones due to noise folding at the PLL output. Because the transfer function from the HM noise $\theta_{n,\mathrm{HM}}$ to the output is the same as (2), $\theta_{n,\mathrm{HM}}$ is not amplified either. As a result, the HM noise contribution is not dominant compared to other noise sources, while in-band tones can be avoided by employing proper LPFs as will be explained in Section III.

The phase noise generated by the main VCO $\theta_{n,\mathrm{VCO}}$ experiences high-pass filtering similar to that in the typical PLL, while the reference phase noise $\theta_{n,\mathrm{REF}}$ goes through the low-pass filtering both from the auxiliary integer-N and main PLLs along with the amplification equal to the ratio between the reference and output frequencies.

III. Circuit Implementation

We implemented the main PLL of the proposed architecture in TSMC 65-nm bulk CMOS process as a proof-of-concept. Figs. 4 and 5 show the details of the circuit building blocks and the chip micrograph, respectively. An 800-to-900 MHz f_{LO} signal for the HM, which corresponds to f_{int}/N_I in Fig. 2, is provided by an external signal generator. An analog CP-based architecture is used for ease of implementation. The VCO uses a CMOS type LC-oscillator. The DSM is of 2nd order and has 16 bits. The second-order architecture was chosen because the quantization noise contributed by the DSM at the output is already negligible with second-order noise shaping thanks to the proposed architecture. The HM is composed of a sample-and-hold (S/H) circuit and an LPF as shown in Fig. 4 for the implementation simplicity. The operation principle of the HM in

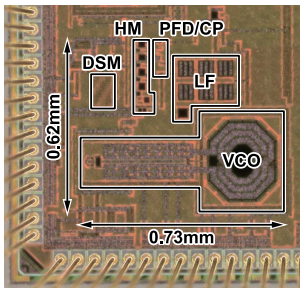

Fig. 5. Chip micrograph.

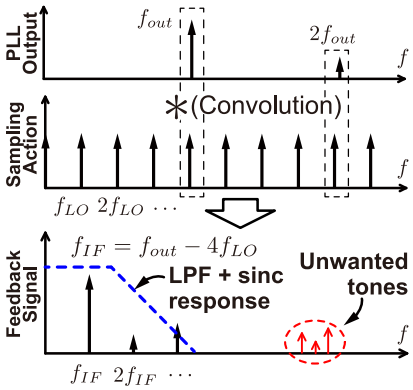

Fig. 6. Operation principle of the HM.

this prototype is summarized in Fig. 6. A square-wave clock drives the S/H circuit and its fourth harmonic is used to downconvert the main PLL output, where $N_{\mathrm{HM}} = 4$ that leads to the output frequency of the HM $f_{\mathrm{IF}} = f_{\mathrm{out}} - 4f_{\mathrm{LO}}$. Because the downconversion is performed through the S/H action, unwanted tones can arise to cause both in-band and out-of-band spurs at the output after the sampling with PFD/CP. These spurs are mitigated by placing the LPF before and after the S/H circuit to filter out unwanted tones before and after the frequency downconversion, respectively.

IV. Simulation and Measurement Results

We first show behavioral simulation results that demonstrate the characteristics of the proposed PLL derived in Section II. Fig. 7 compares the phase noise contributions from the DSM in the conventional and the proposed architectures. The design parameters have been chosen so that both architectures have the same bandwidth (800 kHz) and the MMDs have the same input and output frequencies (3.588 GHz and 77.97 MHz, respectively). The difference of the noise contribution is ∼33 dB, which corresponds to $20\log_{10}(N.\alpha - 1)$ where $N.\alpha \sim 46$. This clearly proves that the $\Delta\Sigma$ noise is not amplified in the proposed loop architecture. Fig. 8 shows the fractional spurs observed in both architectures with the CP nonlinearity being represented by a 5 % current mismatch between UP and DOWN current sources. Similarly in this simulation, the fractional spur in the proposed architecture located at 77.97 MHz×0.00386 = 301 kHz is ∼33 dB lower than that in the conventional architecture, proving that the nonlinearity-induced fractional spur is not amplified either. The elevated noise floor in Fig. 8(a) corresponds to the amplified quantization noise from the DSM as is also observed in Fig. 7.

Fig. 9 shows the measured output phase noise spectrum in integer and fractional modes along with the expected phase noise contribution from the DSM in the conventional and the proposed architectures. Since the difference in the phase noise between two modes

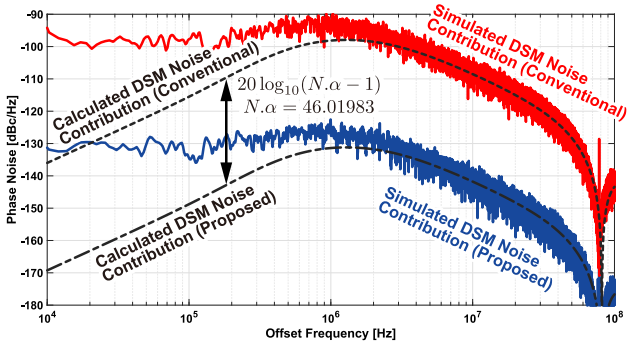

Fig. 7. Comparison between the DSM phase noise contributions in the conventional and the proposed architectures.

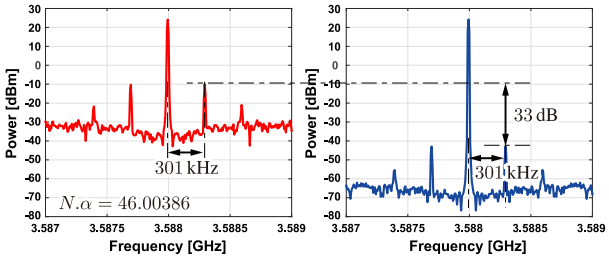

Fig. 8. Simulated output spectra with fractional spurs in (a) conventional and (b) proposed architectures.

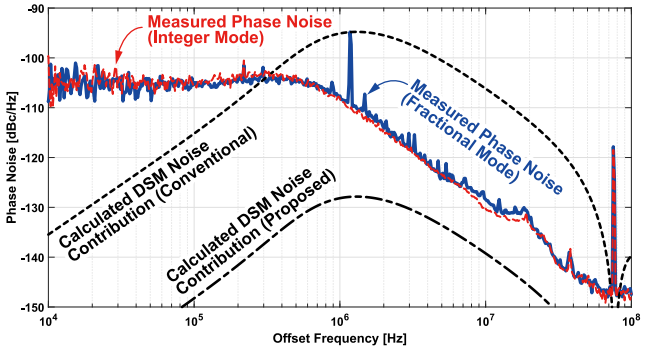

Fig. 9. Measured phase noise spectra in integer ($N = 46$) and fractional ($N.\alpha = 46 + 2^{-6}$) modes along with the expected DSM noise contributions.

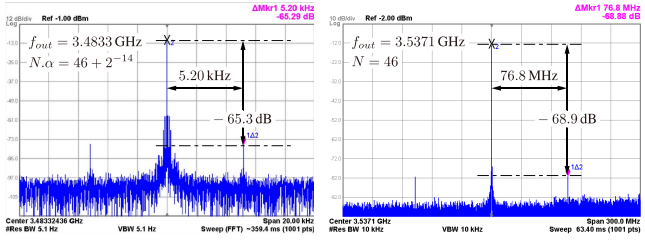

Fig. 10. Measured output spectra that show (a) fractional spurs at $\alpha f_{IF} = 5.2$ kHz and (b) spurs at the PFD input frequency $f_{\mathrm{IF}} = 76.8$ MHz.

corresponds to the phase noise contributed by the DSM, this measurement result also proves that the proposed loop does not amplify the noise from the DSM. Here, we can see the fractional spur at $\alpha f_{\mathrm{IF}} \sim 1.2$ MHz only in the fractional mode, and the spur at the PFD input frequency $f_{\mathrm{IF}} \sim 77$ MHz in both fractional and integer modes. Fig. 10(a) and (b) show the measured output spectrum with

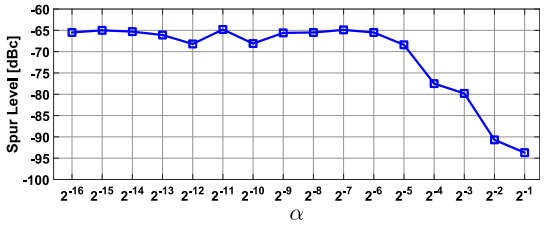

Fig. 11. Plot of the measured fractional spur for different values of α.

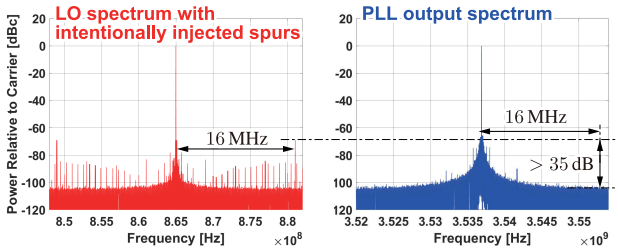

Fig. 12. Low-pass filtering of out-of-band spurs from the auxiliary PLL.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

Reference	**This work**	Wu JSSC'19 [3]	Yang ISSCC'19 [8]	Ho ISSCC'18 [6]	Raczkowski JSSC'15 [4]
Architecture	Dual Feedback	DTC SPLL	Triple loop	Reference Dithering	DTC SSPLL
Freq. [GHz]	3.2-3.8	5.5-7.3	7.0-9.0	3.0-5.2	9.2-12.7
Calibration	**no**	yes	no	yes	yes
# of aux loops	**1**	N/A	2	N/A	N/A
Frac. Spur [dBc]	**<-65**	<-64	<-70	<-62.5	<-43
Ref. Spur [dBc]	**-69**	-70.2	<-66	-102	-60
RMS jitter [fs] (Integ. Range)	503 (10k~100MHz)	75 (10k~10MHz)	131 (10k~10MHz)	1780 (10k~100MHz)	280 (10kHz~60MHz)
IPN [dBc] (Integ. Range)	-42.2 (10k~100MHz)	-54 (10k~10MHz)	-46.9† (10k~10MHz)	-30.9† (10k~100MHz)	-39.8 ~ -38.1 (10kHz~60MHz)
Power [mW]	6.9*	18.9	13.4	18.1	13
Area [mm^2]	0.24	0.45	0.25	0.338	N/A
Process [nm]	65	28	16	65	28

*excluding the auxiliary PLL and I/O buffers †calculated from RMS jitter

−65 dBc fractional spurs at αf_{IF} and that containing −69 dBc spurs at f_{IF}, respectively. Fig. 11 plots the measured fractional spur levels for different fractional values of α in the MMD division ratio of $N.\alpha$. The fractional spur level is lower than −65 dBc throughout the fractional values from 2^{-16} to 2^{-1}. Finally, in order to demonstrate the low-pass filtering action of the main PLL, we deliberately injected spurs into the 800-to-900 MHz signal from the external signal source to mimic the reference spurs from the auxiliary integer-N PLL. Fig. 12 shows the output spectrum of the input signal contaminated with spurs and that of the resulting PLL output. The spurious tone at 16 MHz offset is attenuated by more than 35 dB, which is expected by the −40 dB/dec roll-off characteristic of the main PLL. A performance comparison is given in Table I. The proposed circuit achieves spurious comparable to that of the state-of-the-art, while it requires just 1 auxiliary PLL with no complex calibration.

V. CONCLUSION

In this letter, we proposed the dual-feedback architecture for fractional frequency synthesizers, which achieves low phase noise and spurs without using any complex calibration schemes by avoiding the noise amplification in the feedback loop with only a single auxiliary PLL. The measurement results demonstrated that the contribution of the quantization noise from the DSM is negligible to the phase noise at the output thanks to the proposed loop architecture.

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