A Single-Electron Injection Device for CMOS Charge Qubits Implemented in 22-nm FD-SOI

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***Abstract*—This letter presents a single-electron injection device for position-based charge qubit structures implemented in 22-nm fully depleted silicon-on-insulator CMOS. Quantum dots are implemented in local well areas separated by tunnel barriers controlled by gate terminals overlapping with a thin 5-nm undoped silicon film. Interface of the quantum structure with classical electronic circuitry is provided with single-electron transistors that feature doped wells on the classic side. A small 0.7 × 0.4 μm^2 elementary quantum core is co-located with control circuitry inside the quantum operation cell which is operating at 3.5 K and a 2-GHz clock frequency. With this apparatus, we demonstrate a single-electron injection into a quantum dot.**

***Index Terms*—Cryogenic circuits, fully depleted silicon-on-insulator (FD-SOI), position-based charge qubit, quantum computer, quantum dot (QD), quantum operation cell, quantum point contact (QPC), single-electron injection device (SEID).**

I. Introduction

The qubit is a fundamental building block of a quantum computer that can be realized in superconducting circuits, semiconductor quantum dots (QDs), photons, and trapped ions, to name a few. Among these, the superconducting quantum computing is most prevalent and is currently deployed for commercial use [1], [2]. Superconducting qubits are placed inside a dilution refrigerator (cost >$300 k) operating at 20 mK under a very stringent thermal budget of 20 μW that does not allow any meaningful integration with control electronic circuitry on a large scale. In addition, issues, such as frequency collision and crowding [1], are unavoidable when integrating a large number of qubits. To compensate for such effects, the quantum array has to be properly structured and wired according to a meticulous frequency plan. Moreover, the qubit junctions have to be annealed by a focused laser beam in order to tune their respective frequencies (f_{01}) into a discrete set with sufficient guard-band in between in order to minimize the gate error rates. Such techniques have been used in [1] to build quantum processors comprising 32–64 qubits. However, a practical quantum computer may require substantial qubit overhead for error correction schemes in order to improve operational fidelity [3].

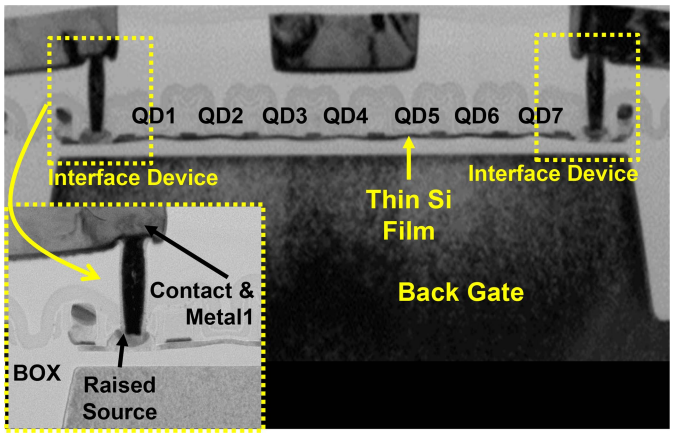

Fig. 1. Cross-sectional view of the proposed coupled QD array together with the end-of-row injection and extraction interface devices. The inset figure shows the zoomed-in view of the SEID. The Metal1 contact terminates into a raised source region.

On the other hand, in semiconductor qubits [4], the electrons are confined within QDs made with layers common in nanoscale CMOS foundry process. The electron's spin is manipulated to build quantum gates. With this approach, the control electronics can be integrated with a large array of qubits on the same silicon [5]–[9] easing some of the challenges with cable and thermal management in the cryocooler. A similar approach is proposed in this letter with one distinction: exploiting the electron's position to realize quantum states at operating temperature of 4 K. That approach relaxes the thermal budget to 1.5 W and, therefore, a large array of qubits and processing circuits can be built on-chip. The required temperature can be achieved with a two-stage Gifford–McMahon cooler at the cost of ∼$60 K and a reasonable low footprint for a server-size quantum computer. The following sections will describe the quantum structure and the control circuitry in detail. The last section will describe the experimental setup and measurement results of the single-electron injection device (SEID) operation which is the main objective of this letter.

II. Overview of CMOS Charge Qubits

This letter is based on the position-based charge qubits [10] that utilize low-power electrostatic gate control, thus enabling the scaling to higher qubit counts. In terms of process technology, the physical structures realizing the proposed qubits and their control circuitry have been designed in 22FDX fully depleted silicon-on-insulator (FD-SOI) technology from GlobalFoundries, as shown in

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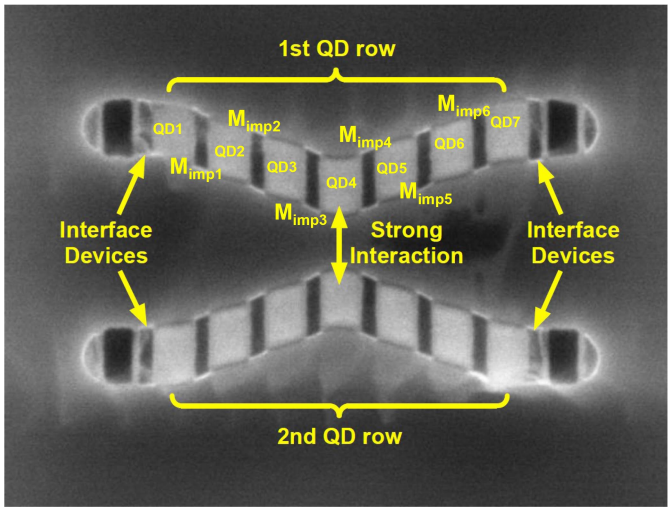

Fig. 2. Top view of 2-D semiconductor charge-qubit array with upper (annotated) and lower rows coupled electrostatically through an interaction gate and connected to classical electronics through interface devices (SEID).

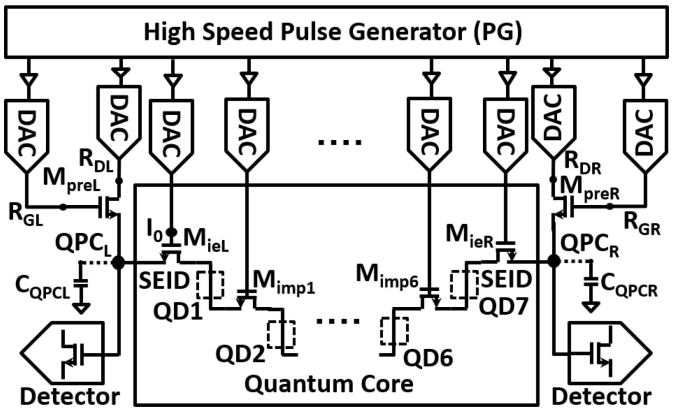

Fig. 3. Quantum structure control circuitry comprising a high-speed PG and amplitude DACs (24 for two rows). The control circuitry drives the SEIDs M_{ieL} and M_{ieR}, imposer devices M_{imp1}–M_{imp6}, and precharge devices M_{preL} and M_{preR}. The electrons are confined within QDs QDx.

Fig. 1 transmission electron microscopy (TEM) photograph. In contrast to bulk process, FD-SOI provides a thin semiconductor layer isolated vertically from the substrate by a buried oxide (BOX) layer. Therefore, a quantum particle can be strictly confined inside a 5-nm thin semiconductor film where it follows the gate control. Building a semiconductor quantum gate requires two types of structures: 1) a quantum device that implements qubits using coupled QDs separated by tunneling barriers controlled by gate terminals (imposers) and 2) an interface device that provides proper connection between the classic and quantum devices. Electrons are injected into a coupled QD array by the interface SEID shown in the inset of Fig. 1. Once a particle is in the first QD, its evolution is controlled by a sequence of gates that impose a potential distribution across the wells [10].

The overhead view of the proposed quantum structure in Fig. 1 is shown in Fig. 2 TEM photograph. The structure has two rows of QDs in a staircase arrangement also called "double-V" shape. The bright regions inside are the QDs while the dark shades in between are the gates acting as imposers. Each row has seven QDs where electrons are confined and six imposers that control the barrier level and tunneling rate between two adjacent QDs in addition to the potential energy profile in the quantum structure [10]. The interaction between two rows is the strongest in the middle where the QDs are in close proximity to each other. The double-V elementary structure can be used to implement more complex quantum circuits having multiple spatially distributed interaction locations. The area of the QD is $< 100 \times 100$ nm^2.

III. Quantum Control Circuitry

Specific sequences of control signals with precise amplitude and pulse width need to be applied to the quantum structure in order to perform the intended functions, such as reset, electron injection, transfer, extraction, and detection. As shown in Fig. 3, the amplitude control is performed by digital-to-analog converters (24 DACs for two rows) while the pulse width control is done by the high-speed pulse generator (PG) [11]. The symmetrical structure has two quantum point contacts (QPCs) labeled QPC_L and QPC_R that serve as sense nodes for the presence or absence of an electron. The precharge devices, namely, M_{preL} and M_{preR}, initialize the QPC to a known voltage before the quantum operation and isolate the QPC during the quantum operation. The DACs connected to R_{GL}, R_{GR}, R_{DL}, and R_{DR} nodes perform that operation while the input clock frequency determines the resolution of pulse width control. The transistors connected to the QPC node are designed with minimum dimensions in order to limit C_{QPCL} and C_{QPCR}. The smaller this capacitance, the larger the voltage step as a result of electron injection or extraction by the SEID. The resulting voltage step needs to be a factor of 10 above the (kT/q) limit of 300 μV. The detector chain is designed such that its input-referred noise is lower than this limit.

The precharge process is followed by an electron injection that is facilitated by the SEID, namely, M_{ieL} and M_{ieR}. The injection of an electron from the $\text{QPC}_{L/R}$ into QD1/7, respectively, requires a gate control pulse having its amplitude versus the reference level commensurate with the Coulomb blockade voltage. The reverse process of electron extraction operates on a similar principle. The quantum operation commences once the electron is placed in QD1 or QD7. That operation consists of initiating and stopping a Rabi (occupancy) oscillation of one (or multiple) electrons between two or more intermediate QDs, namely, QD1–QD7 [10]. These operations are controlled by imposers M_{imp1}–M_{imp6}. The imposer DACs generate the required pulse amplitude, while a digitally controlled pulse width sets the evolution of the electron's wave function resulting in a specific spatial distribution between the QDs. The manipulation of the spatial degree of freedom of the electron's quantum state can realize various rotations in the charge qubits. Once the quantum operation concludes, the SEID extracts the electron (assuming it is there at the completion of quantum operations) from QD1 or QD7 and injects it into QPC_L or QPC_R, respectively, for subsequent detection.

The 8-bit DACs in Fig. 3, the double-V structure (quantum core) in Fig. 2, and the detectors are integrated inside the quantum operation cell shown in Fig. 4. A snapshot of the voltage at QPC is taken by the detector chain before and after the quantum operation. The difference between these two measurements is amplified by the analog buffers during the readout process and the output V_{DET} signal is subsequently sampled by the external ADCs for statistical processing. The pattern generator block controls the timing between various processes in the quantum operation cell. Its internal memory is loaded with instructions that are decoded into waveforms driving the various control blocks, such as the high-speed PG, DACs, and the detectors.

IV. Experimental Results

The quantum operation cell is fabricated in 22-nm FD-SOI CMOS and the die photograph is shown in Fig. 5(right). The cell dimensions are 500×250 μm^2. The QCORE block is the double-V structure in

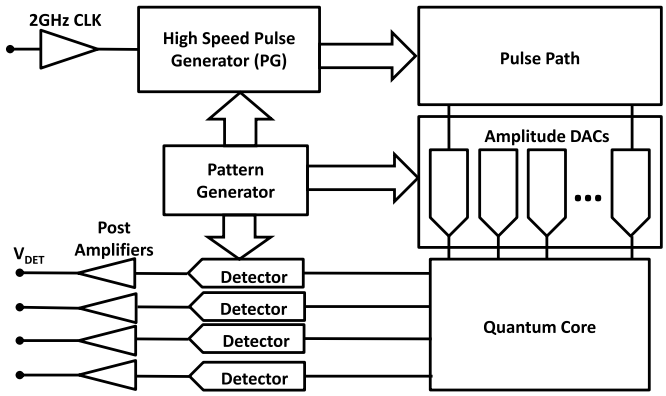

Fig. 4. Top-level block diagram of the quantum operation cell comprising a quantum core, control circuitry, and detectors. The connectivity of the pattern generator block to all control circuits that synthesize and detect signals in the quantum core underscores its "command-and-control" aspect. The detector output voltage V_{DET} is passed to external ADCs for statistical processing.

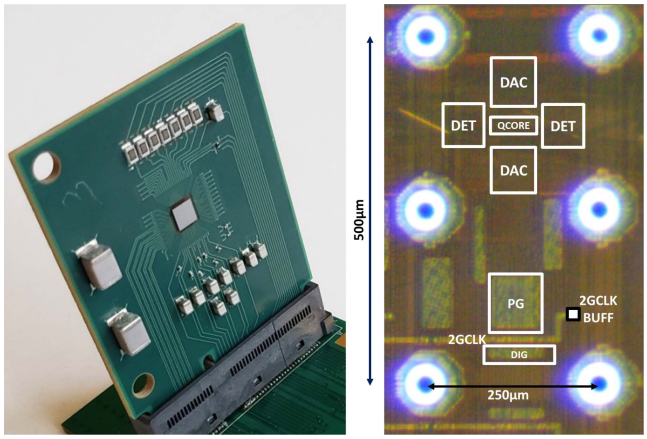

Fig. 5. Flip-chip packaged IC mounted on PCB (left); die photograph of the quantum operation cell (right). The quantum core (QCORE) comprising an array of qubits is surrounded by amplitude DACs and detectors. The high-speed PG is located at the bottom next to the 2 GHz clock buffer.

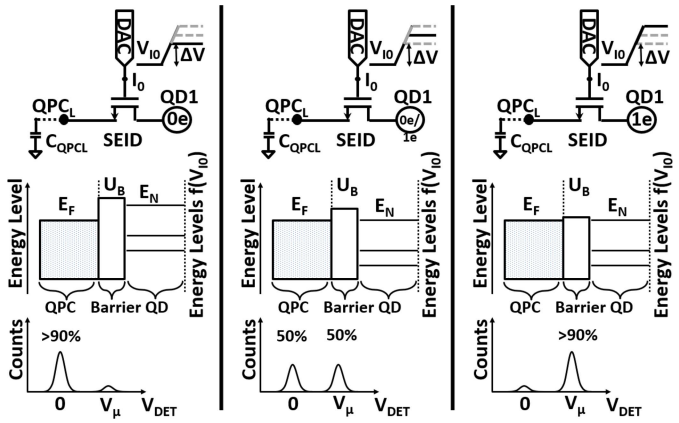

Fig. 6. Illustration of SEID operation by manipulating the barrier (U_B) and discrete energy levels (E_N) in the QD through the amplitude DAC. Three scenarios as described: probability of electron transfer 10% (left); 50% (middle); and 90% (right). V_μ is the average detected voltage when electron transfers.

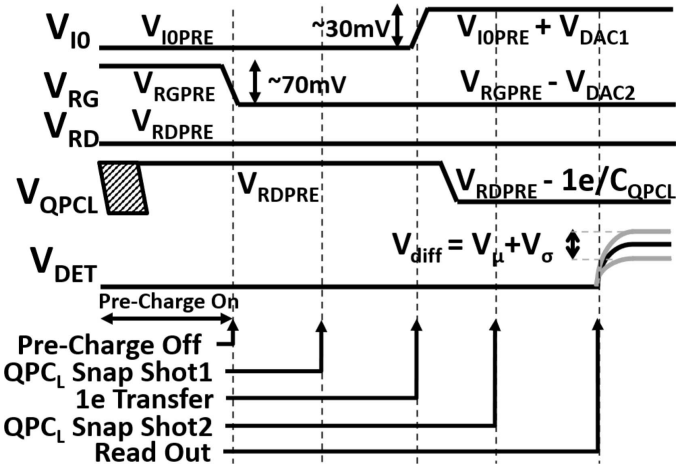

Fig. 7. Time-domain waveform of signals in Fig. 3 associated with the SEID operation described in Fig. 6. In this experiment, two snapshots of QPC$_L$ node are taken before and after U_B energy is lowered. When the electron tunnels into QD, the loss of charge on QPC$_L$ results in a differential voltage output from the detector with an average value V_μ. Voltage standard deviation V_σ is due to circuit noise.

Fig. 2 which requires 24 amplitude DACs and 4 detectors (DET). The DACs are assembled as tiles in an array (fixed height and variable length based on the number of DACs) due to their high aspect ratio. Each additional QD in QCORE requires one DAC and a horizontal spacing of 3.5 μm. The RF clock buffer is located adjacent to the high-speed PG block. The flip-chip IC package on the PCB is shown in Fig. 5(left).

The IC is placed inside a cryo-cooler operating at 3.5 K. The external FPGA programs the on-chip pattern generator with the quantum experiment sequence shown in Figs. 6 and 7 (labels are consistent with Fig. 3) while a 2-GHz source is used as a system clock. The Coulomb blockade operation of SEID can be best understood by the energy level profile shown in Fig. 6. For an electron to be injected into QD1 from QPC$_L$ two conditions have to be satisfied. First, at least one discrete energy level E_N in QD1 has to align with the Fermi level E_F. Second, the barrier level U_B has to be near or lower than E_N. In Fig. 6(left), V_{I0} is too low and none of the aforementioned conditions are satisfied. Consequently, the two snapshots of QPC$_L$ are the same, i.e., $V_{\mathrm{DET}} = 0$ with high probability. In Fig. 6(middle), E_N and E_F are aligned; however, the barrier is high resulting in 50% probability of electron transfer. In Fig. 6(right), U_B is lowered to a point where the probability of electron transfer is >90%.

The time domain waveforms of the scenario detailed in Fig. 6(right) are shown in Fig. 7. The first step is to enable the precharge device while the DACs wired to nodes I_0, R_G, and R_D are precharged to V_{I0PRE}, V_{RGPRE}, and V_{RDPRE}, respectively. This operation ensures that the voltage at node QPC$_L$ is set to V_{RDPRE}. The precharge is subsequently turned off and V_{QPCL} (amplified version) is sampled and stored by the detector chain. Next, the imposer gate I_0 is stepped up by a fixed voltage by the DAC. A ~30-mV step at I_0 translates to ~3-mV step at the tunnel junction and, consequently, U_B is lowered by ~3 meV, which is enough to tunnel one electron from QPC$_L$ to QD1. The resulting change in voltage at QPC$_L$ is $(1e/C_{\mathrm{QPCL}})$. V_{QPCL} is sampled and stored again shortly after the electron transfer. The amplified difference between samples is V_{DET} that has a mean V_μ and standard deviation V_σ.

The experimental verification of Rabi oscillation between intermediate QDs is outside the scope of this letter. The focus here is to verify the single-electron injection operation through M_{ieL} only. The boundary condition for the precharge operation needs to be established before the SEID is engaged. For that purpose, the experiment illustrated in Figs. 6(right) and 7 is repeated over a thousand times for each setting of V_{RGPRE} and V_{RDPRE}. The resulting V_μ is plotted as a heatmap in Fig. 8. When the electron successfully tunnels

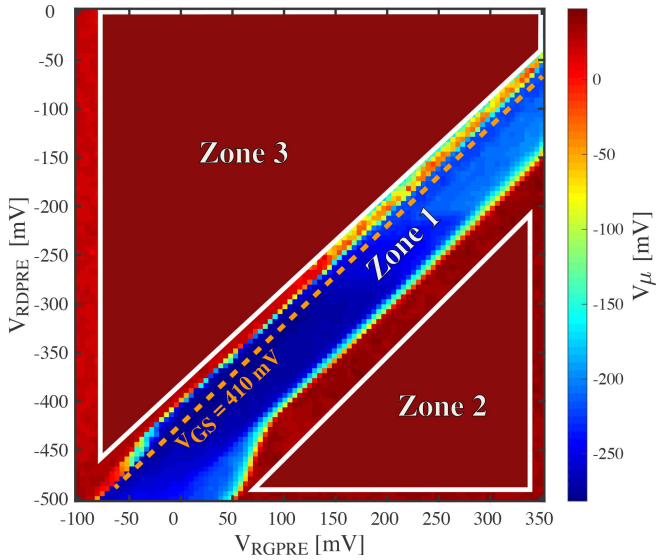

Fig. 8. Measured heatmap of V_μ as a function of R_G and R_D precharge levels (V_{RGPRE} and V_{RDPRE}). The blue region "Zone 1" represents transfer of one electron and the red region "Zone 2" represents no transfer of electrons.

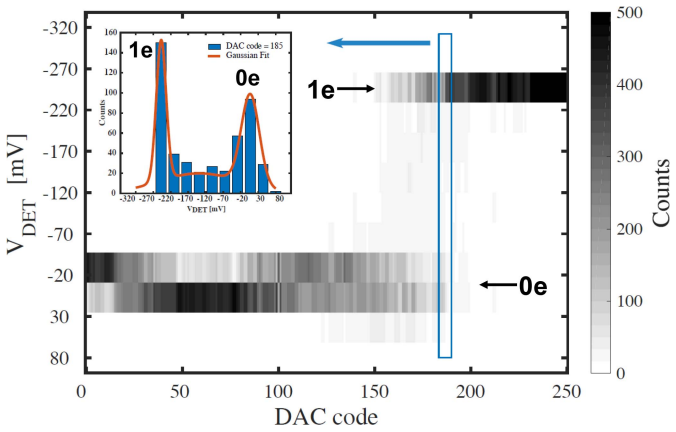

Fig. 9. Measured data of single electron transfer. The single electron transfer takes place around DAC code of 160 when V_{DET} transitions from a low to a high magnitude.

through M_{ieL} into QD1, the V_μ magnitude is higher and is depicted in the plot by the blue color region (Zone 1). In the red colored region (Zone 2), V_μ magnitude is near zero implying no electron transfer. This is due to the elevated V_{gs} of M_{preL} after the precharge phase and hence any information associated with the electron transfer is lost. The data above the 410 mV V_{gs} boundary (V_{RGPRE}–V_{RDPRE}) ("Zone 3") results in improper precharge operation and hence is not of interest.

The digital (0.8 V) and analog (1.5 V) supply current during this operation with all the control circuitry and a single detector (measuring QPC_L) is 3.5 mA and 0.7 mA, respectively. Therefore, the overall power consumption of the quantum operation cell is ~4 mW; orders of magnitude lower than the thermal budget of 1.5 Watt of the cryo-cooler. The precharge boundary condition of $V_{gs} = 410$ mV is used in the next experiment where the objective is to verify the single-electron transfer operation. The DAC voltage driving I_0 (corresponding to the parameter V_{DAC1} in Fig. 7) is varied while the histogram of V_{DET} for each setting of the DAC is collated into a heat map shown in Fig. 9. The electron transfer from QPC_L to QD1 is around the code of 160.

V. Conclusion

We have demonstrated a proper operation of the single-electron injection device (SEID) in the proposed 0.28-μm^2 quantum gate structure in 22-nm CMOS. The SEID requires appropriate biasing of the precharge device, which is verified by rigorous characterization. The compact quantum structure is integrated with all necessary control circuitry operating a very low power of 4 mW.

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