

A Hybrid-PLL (ADPLL/Charge-Pump PLL) Using Phase Realignment With 0.6- μ s Settling, 0.619-ps Integrated Jitter, and -240.5 -dB FoM in 7-nm FinFET

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Abstract—All-digital PLLs (ADPLLs) based on a ring-oscillator (RO) provide very fast settling, but they suffer from quantization noise due to discrete tuning of their digitally controlled oscillator (DCO). Although RO charge-pump PLLs (CP-PLLs) do not exhibit quantization noise thanks to their continuous VCO tuning, they are quite slow and require huge VCO gain to cover frequency drift due to temperature variations. Further, in CP-PLLs, the reset pulse of phase detector (PD) must be wide for proper PLL functioning, but this sets a lower limit on reference spurs. We propose a hybrid-PLL in a 7-nm FinFET CMOS that combines the best advantages of ADPLL and CP-PLL. We introduce periodical phase realignment by the reference clock, and ultrashort pulse for resetting the PD. The hybrid PLL covers 0.2–4 GHz and settles in 0.6 μ s. It emits low -52 dB reference spurs in the conventional mode, and 1.05 ps and 0.62 ps integrated jitter in the conventional and realignment modes, respectively.

Index Terms—All-digital PLL (ADPLL), charge-pump PLL (CP-PLL), fast settling, hybrid PLL, realignment and injection locking, reference spur.

I. INTRODUCTION

The wide-tuning-range ring-oscillator (RO)-based PLLs are widely used in the applications of DDR, SoC, and SerDes. The modern products push for lower power consumption, smaller die size, and higher operated frequency. However, those requirements can be satisfied by advanced process technology [1] because it can provide lower supply voltage, larger device driving current, and smaller device than does the mature technology. Although conventional RO-based ADPLLs have numerous advantages over their analog charge-pump (CP) counterparts in advanced technology [2], [3], they still have some limitations as below. Step-size resolution of a digitally controlled oscillator (DCO) must be very fine, which is quite challenging to meet; otherwise, its quantization noise will degrade the ADPLL's jitter performance. Further, the ADPLLs employ a deterministic sequencer to switch from the frequency acquisition to phase tracking [2], [3]. However, if the allocated acquisition interval happens to be insufficient, then the PLL might run out of range during the phase tracking. Hence, the conventional ADPLLs need hundreds of reference cycles to complete the frequency acquisition. Although the RO-type CP-PLLs avoid quantization noise thanks to the continuous tuning of a VCO, they suffer from two issues.

- 1) The effective voltage tuning range of VCO becomes very narrow (<0.3 V) because of lower supply voltage that causes huge VCO gain (K_{VCO}). In general, 4-GHz frequency tuning

range generates more than 13 GHz/V K_{VCO} in 0.3-V voltage range. Huge VCO gain degrades the performance of jitter and reference spur when PLL suffers from noisy supply or ground.

- 2) Long acquisition times are caused by a limited PLL bandwidth (BW).

In order to meet the stability requirements, the PLL-BW must be smaller than one-tenth of reference clock (FREF). However, traditional ADPLLs [2], [3] can provide shortest frequency acquisition times because the output difference of reference accumulator and variable accumulator (called phase error, PHE) is huge at the beginning to provide huge frequency jump. When the RO frequency is close to target, the PHE becomes smooth, meaning frequency jump becomes small. In general, the modern products call for the locking time of PLL to be <3 μ s [4]. Furthermore, in traditional CP-PLLs, the wide reset pulse of phase detector (PD) is adopted to guarantee a proper PLL function but a current mismatch between the CP's head and tail current sources causes an increase in reference spurs. A digital self-calibration algorithm of the VCO center frequency was presented in [5] to reduce the VCO gain. It uses binary search to find the target band, but it needs a lot of reference cycles to complete the calibration. Furthermore, the digital coarse tuning of VCO is composed of a voltage-to-current converter (V2I), current multiplier, and an ICO. Hence, the VCO gain (K_{VCO}) varies with the tuning word, thus creating a problem of excessively varying the PLL bandwidth over the wide tuning range.

In this letter, we propose a hybrid PLL architecture that *dynamically* combines the digital manner of frequency acquisition in ADPLLs with the fine continuous-phase tracking in CP-PLLs to provide an overall better performance, faster locking time, better power supply rejection, lower oscillator's sensitivity to noise, and digital relocking in case of running out of tracking range, while avoiding the oscillator's quantization noise. In this PLL, a digital control loop of a counter-based ADPLL is used for the fast frequency acquisition, whereas a CP-PLL is then *seamlessly* turned in for the fine phase tracking (see Fig. 1). Hence, it combines the advantages of ADPLL and CP-PLL to reach fast tracking time (<40 reference cycles) while being free from the DCO quantization noise. This PLL also builds a block called tracking-trend-detector. It can automatically transit digital phase acquisition to analog phase tracking at the earliest possible opportunity when the instantaneous oscillating frequency fluctuates around the desired target (see Fig. 2). The switchover to digital coarse tuning is also done automatically in case of running out of tracking range. Benefiting the hybrid architecture of this PLL, the proposed hybrid RO (see Fig. 3) uses collaborative digital and analog tuning controls. It obtains over an octave tuning range with low analog RO gain (K_{RO}) of merely 3 GHz/V. However, low K_{RO} means the device of "voltage to current" can adopt smaller size to reduce gate leakage current and improve reference spur as well.

The proposed PLL is realized in a 7-nm FinFET, whose devices exhibit excellent g_m and I_{ON} [1], thus allowing to be clocked at a much higher reference frequency (FREF) while consuming less power and producing shorter inverter delay. The reference spurs are improved by means of ultrashort reset pulse in the PD and faster switching devices in the charge pump. However, the low frequency device noise becomes worse with process technology migration [6].

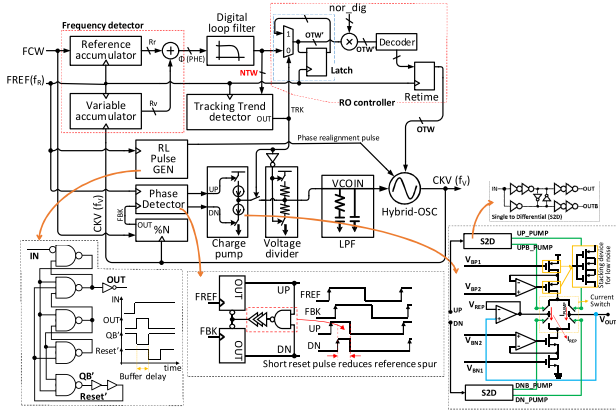
Manuscript received May 18, 2020; revised July 1, 2020; accepted July 13, 2020. Date of publication July 20, 2020; date of current version August 4, 2020. This article was approved by Associate Editor Shuo-Wei (Mike) Chen. The work of Tsung-Hsien Tsai was supported in part by the Science Foundation Ireland under Grant 14/RP/I2921. (*Corresponding author: Tsung-Hsien Tsai.*)

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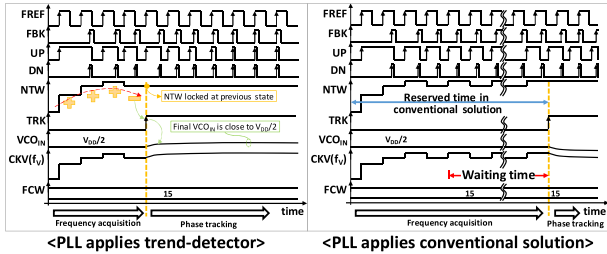
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Digital Object Identifier 10.1109/LSSC.2020.3010278



(a)



(b)

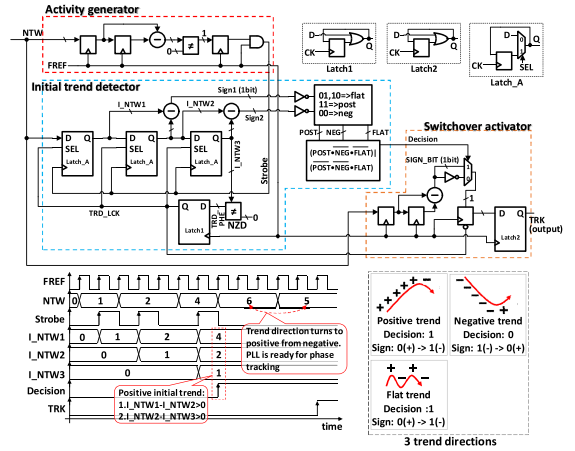
(c)

Fig. 1. Hybrid PLL. (a) Block diagram. (b) Tracking behavior with the trend-detector. (c) Tracking behavior using the conventional solution.

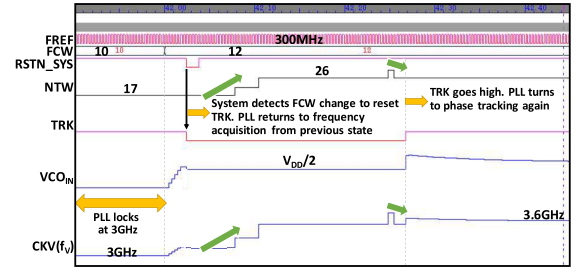
The realignment technique is induced into this PLL for suppressing the in-band noise of PLL and improving jitter performance.

II. ARCHITECTURE AND CIRCUIT DESIGN

Fig. 1(a) shows the overall hybrid-PLL architecture. It consists of the digitally controlled frequency acquisition path and analog-controlled phase-tracking path, jointly tuning the hybrid RO. The former includes a supply voltage divider. The latter comprises a PD, a CP, an RC loop filter (RC-LF), a feedback divider ($\%N$), and a short pulse generator (RL-Pulse-GEN) for the phase realignment. During the frequency acquisition ($TRK = 0$), the voltage divider feeds the VCO_{IN} input to hybrid RO at $1/2 V_{DD}$ while the analog controlled loop is disabled by breaking the connection between CP and RC-LF. The digital frequency detector compares the phases of $FREF$ and CKV and produces PHE. It is then filtered and normalized as NTW . The RO controller with gain normalization converts NTW to a thermometer code for frequency tuning with the precisely controlled bandwidth ($= \alpha * FREF / 2\pi$, $\alpha = 2^{-3} \sim 1$) [3]. The *optimum* switchover is decided by the tracking trend detector. The PD and feedback divider are operating throughout for quickly responding to the acquisition/tracking switchover. At the moment of switchover, the $FREF$ and FBK clocks are roughly phase aligned, as shown in Fig. 1(b). During the phase tracking, $TRK = 1$ turns off the voltage divider and enables the analog controlled loop (the path of CP to RC-LF) for producing the continuous tuning voltage (VCO_{IN}). At the same time, the latch of RO controller is opaque, allowing to disconnect the digital loop while maintaining the NTW state. The overall locking time, including the frequency acquisition and phase tracking, is only 0.6 μ s. Benefiting from this architecture, the frequency tuning range of VCO in phase tracking mode can become narrow and thus the V2I device receiving VCO_{IN} can be chosen small to reduce leakage current. However, in order to reduce efficiently the leakage current of VCO_{IN} path, the capacitor of RC-LF is implemented with MOM capacitors. The device channel length is smaller than 1 μ m in advanced technology [7], the stacking gate device is



(a)



(b)

Fig. 2. Tracking trend detector: (a) schematic and timing diagram (all flip-flops are reset on power-up). (b) Behavior simulation with FCW change.

used to increase the output resistance. However, in order to achieve fast switching times with high output resistance in CP, the regulated wide-swing current mirror with current switching is used in the CP of this PLL. Benefiting from the 7-nm FinFET, I_{REP} can fast switch to I_{PUMP} with the incoming UP/DN. However, the short channel device of 7-nm FinFET provides shorter delay time [7] that can produce the narrow reset pulse for PD. Hence, the combination of narrow reset pulse in PD and fast switching current in PUMP can reduce the mismatch current injected from CP to RC-LF for improving the reference spur. The RL pulse is generated by RL-Pulse-GEN, which is composed of a latch and a few buffer cells which are also used in the PD, thus ensuring precise timing between the two functions.

The conventional ADPLLs employ a *deterministic* sequencer to switch from the frequency acquisition to phase tracking [2], [3]. However, if the allocated acquisition interval happens to be insufficient, then the PLL might run out of range during the phase tracking. Due to PVT uncertainties and wide range of the generated frequencies, the conventional ADPLLs take hundreds of reference cycles to complete the frequency acquisition just to avoid any failure caused by prematurely entering the phase tracking. We propose a *behavioral* sequencer, the tracking trend detector in Fig. 2, which automatically finds the earliest safe switchover point by observing the oscillator tuning word (NTW). The tracking behavior of the conventional and proposed PLL arrangements are shown in Fig. 1(c) and (b), respectively. The proposed circuitry comprises the activity generator producing a strobe only when the NTW changes, the initial trend detector “clocked” by the strobe, and the switchover activator to assert the switchover control, TRK . At first, the registers of $I_NTW1 \sim 3$ are reset and the nonzero-detector (NZD) outputs logic low to latch1. Three different NTW samples are captured by the strobe clock. Latch1 will lock the three initial NTW samples as soon as NZD detects nonzero in register I_NTW3 . Then, the following logic circuitry decides on the initial trend direction from $sign1$ and

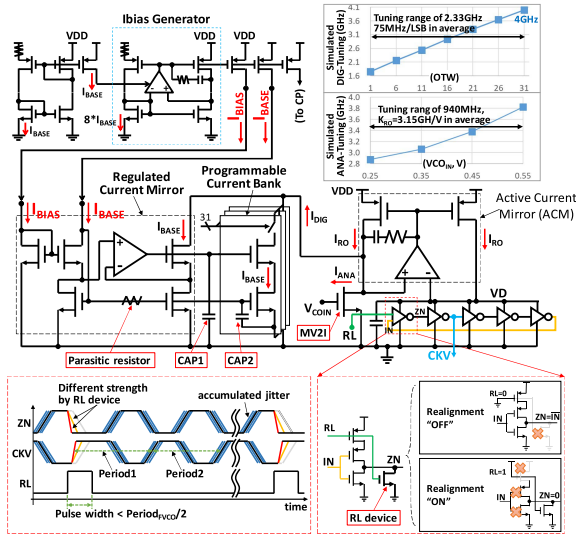


Fig. 3. Ideal schematic of the hybrid RO, highlighting the tuning range coverage and phase realignment schemes.

sign2. (sign2/sign1: 2'b00 for negative trend, 2'b11 for positive trend, and 2'b01/10 for flat trend). In the switchover activator, a reversal of the trend direction can be detected by comparing two consecutive samples and the switchover command (TRK) is locked by latch2. Hence, the proposed hybrid PLL with the behavioral sequencer takes only dozens of reference cycles to complete the frequency acquisition. If FCW is changed, the hybrid PLL will retune the frequency acquisition from phase tracking by tying VCO_{IN} to $V_{DD}/2$ (enabling the voltage divider again). Furthermore, the frequency acquisition resumes from the last NTW state, rather than the middle reset state, as shown in Fig. 2(b).

Fig. 3 shows a circuit diagram of the hybrid RO. The proposed technique combines the digital I_{DIG} and analog I_{ANA} tuning currents to generate the RO supply current, I_{RO} , while using an active current mirror to increase robustness to supply variations. The RO is implemented with ultralow V_T devices such that its supply voltage (V_D) can be as low as 0.45 V. A voltage margin of 200 mV can maintain the pMOS device of active current mirror in saturation. That sets the supply voltage of hybrid PLL to 0.65 V. The digital tuning path comprises a regulated current mirror and programmable current bank with 31 thermometer-coded tuning steps that produce a combined current ($I_{DIG} = I_{BASE} + I_{BASE} * \text{stages}$). The structure of regulated current mirror can provide enough output resistance against the ground noise and it can reduce the mismatching current between current banks in advance technology. This manner of current control is chosen over the conventional capacitance control as it is more precise for tuning with less phase noise variability. The unit current, I_{BASE} , of 20 μA generates an average frequency step of 75 MHz and its quantization error (residue) is passed to the analog tuning path during the phase tracking. This handoff feature is distinct from conventional “hybrid” solutions and is instrumental in achieving the ultrafast settling. The total digital tuning range is 2.33 GHz. The analog path comprises an nMOS device (called MV2I) for translation of tuning voltage (VCO_{IN}) to current I_{ANA} for the phase tracking. The RO drift due to temperature is ~ 430 MHz from -40°C to 125°C (i.e., 2.6 MHz/ $^\circ\text{C}$). The analog tuning range of 940 MHz can cover $2\times$ of the RO frequency drift and so it results in average K_{RO} of 3.15 GHz/V in the 0.3-V tuning range, which is $3.6\times$ gain reduction improvement versus the conventional CP-PLLs. However, the MV2I can use small device size because of small K_{RO} and thus it can reduce the leakage current on the path of CP to hybrid-RO. Furthermore, the I_{DIG} current is tuned by the oscillator tuning word in thermometer code (OTW) that is independent of I_{ANA} . Hence, it can provide uniform frequency

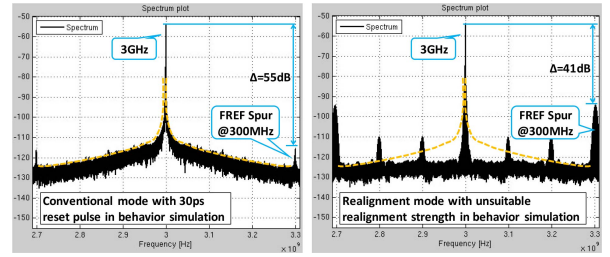


Fig. 4. Behavioral simulations in the conventional mode with 30-ps reset pulse (left) and the realignment mode with *unsuitable* RL strength (right).

steps and its K_{RO} does not vary with tuning words thus providing a stable PLL bandwidth (unlike in [5]). The I_{BIAS} current is generated by a current generator with active-current-mirror (ACM) to provide high power noise rejection for maintaining the clock quality. The capacitor1 (CAP1) is used to compensate the stability of regulated current mirror. The combination of capacitor2 (CAP2) in current banks and parasitic resistor is used to filter the current noise; its bandwidth is set around 10 MHz because the noise of hybrid-RO in closed-loop can be suppressed by PLL-BW. In the realignment mode, a very narrow pulse (RL) triggered by the rising edge of FREF is injected into the RO. The first RO cell functions as a loop inverter when $RL = 0$ and RL device is turned off. During a brief moment when $RL = 1$, the RO loop is broken and the net of ZN is pulled to ground, CKV gets edge-aligned with FREF. However, the RO’s accumulated jitter is refreshed [8], [9].

The strength of realignment (RL) dominates the performance of period jitter and reference spur. Although a sufficient strength can reset the accumulated jitter of oscillator to reduce the in-band noise of PLL, this strength distorts the ZN waveform for phase alignment to cause transient period difference on period1 and period2 that degrades the period jitter. However, if the latency of FREF to RL is different than the latency of FREF to UP/DN, the locked phase of CP-loop is broken by this RL strength. The phase difference of UP and DN generated by the PFD appears as the voltage variation of VCO_{IN} to adjust the RO’s phase that degrades the reference spur, as shown in Fig. 4. Therefore, the suitable RL strength can efficiently reduce the in-band noise of PLL and does not degrade the reference spur and period jitter. Fig. 4 shows the behavioral simulations between the conventional mode with a 30-ps reset pulse and the realignment mode with unsuitable realigned strength; the reference clock is applied at 300 MHz for reducing simulation time and it also shows the reference spur at 300 MHz offset; the target frequency is set at 3 GHz for both simulations. In the conventional mode, the reference spur shows 55dB and the border of spectrum is drawn with a yellow dot line. In the realignment mode, the unsuitable realigned strength (strong one) is applied. The in-band spectrum is efficiently suppressed (compared to the yellow dot line) but the reference spur is degraded to 41 dB. The RL-Pulse-GEN is integrated into the PFD and implemented by auto-place-and-route (APR), while the RL device is implemented by customized layout. Unfortunately, the latencies of FREF to RL and FREF to UP/DN are not constrained in APR and there are no adjustable options built into this prototype. The RL device uses the same W/L as the ring-cell and did not incorporate any adjustable options. It means, this prototype has enough capability to reduce the in-band noise of PLL but the performance of reference spur and period jitter are degraded by the unconstrained realigned strength.

III. MEASUREMENT RESULTS AND CONCLUSION

The proposed hybrid-PLL is implemented in TSMC 7-nm FinFET CMOS. Fig. 5 shows the measured settling behavior. The overall settling time is only 0.6 μs at 200-MHz FREF (0.8 μs at 100-MHz FREF) and includes 0.12 μs with $\alpha = 2^{-2}$ and 0.48 μs for the frequency and phase acquisition, respectively.

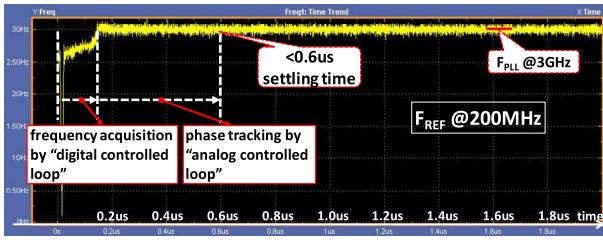


Fig. 5. Measured settling behavior at 200-MHz FREF.

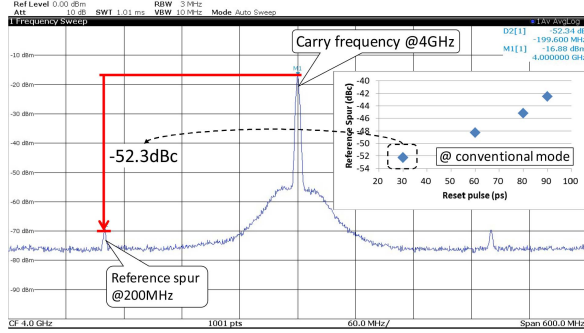


Fig. 6. Measured spectrum at 4-GHz FPLL at 200-MHz FREF and comparison of reset pulse of PD and performance of reference spur.

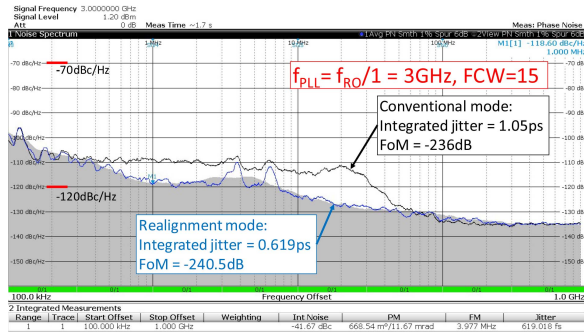


Fig. 7. Measured phase noise of conventional mode and realignment mode at 3-GHz PLL output with 200-MHz FREF.

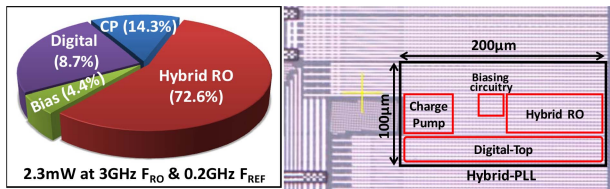


Fig. 8. Power consumption allocation among various blocks and die photograph of the 7-nm FinFET hybrid PLL.

Fig. 6 shows the measured spectrum at 4-GHz PLL output with 200-MHz FREF. The measured reference spur is -52.3 dBc when in the conventional mode with an ultrashort PD reset pulse of 30 ps (verified to degrade to -41 dBc if the width of reset pulse would increase to 90 ps). In Fig. 7, the measured integrated phase jitter at 3 GHz PLL output with 200-MHz FREF is 0.619 ps in the realignment mode and 1.05 ps in the conventional mode. In the conventional mode, -110 dBc/Hz in-band PN is limited by the CP noise. Benefited from the advantage of realignment, the in-band noise can be eliminated effectively to achieve -120 dBc/Hz, which is merely bounded by the FREF noise with $20\log(\text{FCW})$. The spurs at 4 MHz and 6 MHz exist in both conventional and realignment modes and are caused by the testing environment. Fig. 8 shows the power consumption

 TABLE I
 PERFORMANCE SUMMARY AND COMPARISON TO STATE-OF-THE-ART

Reference	This Work	ISSCC'16[3]	JSSC'13[10]	ISSCC'16[11]	
Architecture	Hybrid PLL	Charge Pump PLL	MDLL	DMDLL	
Technology	7 nm	14 nm	0.13 μ m	28 nm	
Supply	0.65 V	0.95 V	1.1 V	NA	
Reference	200 MHz	100 MHz	375 MHz	75 MHz	
Output	0.2 G-4 GHz	0.15 G-5 GHz	1.5 GHz	2.4 GHz	
Settling time @ F_{PLL}	0.6 μ s @3 GHz	2.96 μ s @1.2 GHz	NA	NA	
Area (mm^2)	0.012	0.022	0.25	0.024	
F_{RO} for jitter/power measurements	3 GHz@RL ²	3 GHz@Con ³	4 GHz	1.5 GHz	2.4 GHz
Integrated jitter (ps)	0.619	1.05	1.26	0.4	0.7
Power (mW)	2.3	2.56	0.9	1.51	
FoM ¹ (dB)	-240.5	-236	-233.9	-248.4	-241

¹FoM = $10 \cdot \log[(\sigma_{\text{jitter}}^2) \cdot (P_{\text{DC}}/1\text{mW})]$, ²RL: realignment mode, ³Con: conventional mode

allocation among various blocks and the die micrograph. The core area is 0.012 mm^2 plus 0.008 mm^2 for decoupling capacitors dedicated to filter out heavy digital noise from the host supply. The total power at 3-GHz PLL output with 200-MHz FREF is 2.3 mW @0.65 V (1.67 mW for hybrid RO, 0.33 mW for CP, 0.2 mW for digital logic, and 0.1 mW for bias circuit), leading to the record-high FoM of -240.5 dB in realignment mode and -236 dB in the conventional mode.

Table I compares the proposed hybrid PLL with the state-of-the-art RO PLLs. It achieves the fastest settling of 0.6 μ s, and the best integrated jitter and FoM of 0.619 ps and -240.5 dB, respectively.

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