An Adaptive-Resolution Quasi-Level-Crossing-Sampling ADC Based on Residue Quantization in 28-nm CMOS

Hongying Wang, *Student Member, IEEE*, Filippo Schembari, *Member, IEEE*, Marek Miśkowicz, *Senior Member, IEEE*, and Robert Bogdan Staszewski, *Fellow, IEEE*

***Abstract*—We present a digitally intensive adaptive-resolution (AR) quasi-level-crossing-sampling (quasi-LCS) analog-to-digital converter (ADC) for Internet-of-Things wireless networks, where the power consumed in data transmission, processing, and storage can be significantly reduced by minimizing the ADC's gross output bit-rate. The AR quasi-LCS ADC is implemented as a delta-modulator and adopts a 4-bit asynchronous SAR ADC to quantize the residue voltage signal, thus allowing a straightforward implementation of LCS and AR algorithms in the digital domain, as well as yielding a digital-friendly architecture. Fabricated in 28-nm CMOS, this ADC achieves an SNDR of 53 dB over 1.42 MHz signal bandwidth while consuming 205 μW and an active area of 0.0126 mm^2.**

***Index Terms*—Adaptive resolution (AR), analog-to-digital converter (ADC), asynchronous SAR ADC, compressed sensing, event-based signal processing, level-crossing sampling (LCS).**

I. Introduction

Wireless sensor devices underpin the broad ecosystem of Internet-of-Things. Battery-powered wireless sensor nodes benefit from adopting the nanoscale CMOS technology to promote inexpensive large-scale integration with good power efficiency. The latter should be pursued not only at the analog front-end and analog-to-digital converter (ADC) stages, but also at the RF transmitter (TX) and digital signal processor (DSP), given the ever-increasing amount of data to be transmitted, processed, and stored. Indeed, the power budget of a wireless sensor node is almost always dominated by the DSP and RF TX. A possible way of increasing the system power efficiency is to reduce average gross output bit rate. Such paradigm was exploited in [1] for biopotential signal acquisition, leveraging on an adaptive sampling mechanism which adjusts the ADC sampling frequency f_s based on the input signals slew rate. The adjustment of sampling frequency is however between only two f_s values, limiting the efficiency of the technique. In [2], a compressed-sensing analog front-end was implemented by pipelining the compressed-sensing channels which include Nyquist-rate programable switched-capacitor (sw-cap) multiplying digital-to-analog converter/integrators and sub-Nyquist rate ADCs, so as to reduce the gross output bit rate. That technique, however, requires complex hardware in the front-end, and results in a complex and more power-hungry signal recovery at the receiver side.

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H. Wang, F. Schembari, and R. B. Staszewski are with the School of Electrical and Electronic Engineering, University College Dublin, Dublin 4, D04 V1W8 Ireland (e-mail: hongying.wang@ucdconnect.ie).

M. Miśkowicz is with the Department of Measurement and Electronics, AGH University of Science and Technology, 30-059 Kraków, Poland.

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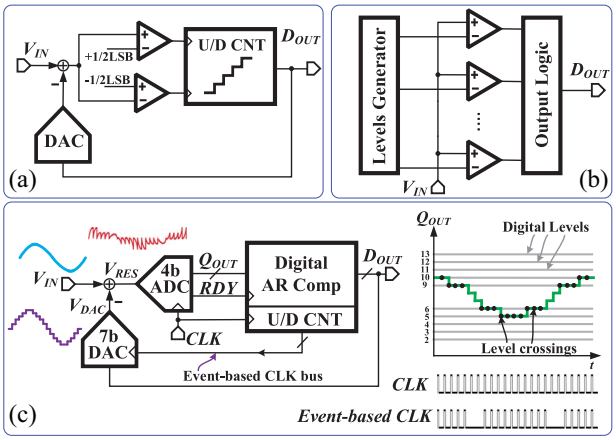

Fig. 1. LCS ADC topologies. (a) Delta-modulator. (b) Flash. (c) Proposed.

An attractive alternative to the aforementioned techniques is level-crossing sampling (LCS), in which the signal is sampled and converted only when it crosses specific threshold levels. LCS also brings information about where the input signal lies (i.e., between which neighboring levels), which becomes more important as the temporal distance between two consecutive level-crossings (Δt_{zc}) increases, and it is of particular interest when Δt_{zc} is locally larger than the Nyquist period, since it allows to represent the input at sub-Nyquist level-crossing rate. Two common LCS ADC topologies are the delta modulator [Fig. 1(a)] [3], [4] and the flash [Fig. 1(b)] [5]. Both of them typically make use of *high-performance* comparators to detect threshold crossings, which are rather challenging in nanoscale CMOS given the low intrinsic gain of transistors and, more importantly, considering that the regeneration time depends on the input signal derivative, which ultimately impairs the ADC linearity. It is also worth noting that a purely continuous-time (CT) approach cannot directly interface to conventional discrete-time (DT) DSPs, demanding an interposed synchronization logic. The gross output bit-rate of an LCS ADC can be further reduced by adaptively tuning the ADC resolution (LSB) depending on the input signal derivative (adaptive-resolution LCS, AR LCS [6]).

In this letter, we propose a digitally intensive AR quasi-CT LCS delta-modulator [Fig. 1(c)] which quantizes its voltage residue V_{RES} by means of a low-resolution but heavily oversampled sub-ADC (*residue quantizer*). This mimics the CT LCS operation and allows a straightforward implementation of LCS and AR algorithms in the digital domain, which can be realized as a readily synthesizable logic. This is achieved using an asynchronous 4-bit SAR ADC as the residue quantizer, whose *ready* output signal (*RDY*) is used as a clock of a multithreshold comparator (*AR Comp*) within the following synthesized digital logic, thus enabling adaptive resolution quantization (up to 5 LSBs in this design). The latter also integrates an up/down

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counter (*U/D CNT*) clocked by *CLK* which generates the binary digital inputs for the feedback DAC. Implemented in TSMC 28-nm LP CMOS, this ADC achieves 53-dB SNDR over a 1.42-MHz bandwidth with a maximum power consumption of 205 μW, and it can directly interface with the DT DSPs.

II. Proposed Residue-Quantizing Quasi-LCS ADC

In LCS ADCs, the conversion errors arise from uncertainty in the position of threshold levels (amplitude error) and from finite time resolution of the time quantizer (timing error) [7]. Neglecting amplitude errors, the ADC SNR, as a function of time quantization, is expressed as in [8]

$$\mathrm{SNR_{dB}} = 20\log_{10}(R) - 14.2 \tag{1}$$

where R is the timing resolution ratio, equal to $(f_{\mathrm{in}} \cdot \Delta t_e)^{-1}$, in which f_{in} is the input signal frequency and Δt_e is the absolute timing error (i.e., here, the delta-modulator loop delay variation, Δt_L). In asynchronous LCS ADCs, Δt_L is mainly due to the propagation-delay dispersion of comparators.

We propose here a new method to perform the LCS and to reduce the effects of absolute timing error, in which the input sampling clock of the ADC is gated off based on level crossing triggers. The signal BW in this system is bounded to the maximum voltage shift $\Delta_{\max}$ that the feedback DAC is able to provide in the clock period $(1/f_s)$. By equalizing this slew rate $f_s\Delta_{\max}$ to the maximum derivative of a -3 dBFS input sinewave signal (amplitude indicated as $A_{-3\mathrm{dB}}$), it is calculated as

$$\Delta_{\max} \cdot f_s = \max\{\frac{\delta}{\delta t}[A_{-3\mathrm{dB}} \cdot \sin(2\pi \cdot \mathrm{BW} \cdot t)]\} \tag{2}$$

and therefore $\mathrm{BW} = (\Delta_{\max} \cdot f_s)/(2\pi \cdot A_{-3\mathrm{dB}})$. Adaptive resolution up to 5 LSBs can extend the BW by 5 times.

The main purpose of this letter is to promote shifting the functionality of an LCS ADC toward the digital domain (hence, the adopted terminology quasi-LCS), with the additional benefits of mitigating the negative impact of analog comparators on performance. Our objective is to digitize the delta-modulator residue signal V_{RES} using a low-resolution sub-ADC such that the AR-LCS algorithm can now be mostly carried out in digital logic. Therefore, the realization of adaptive resolution is nearly costless in terms of hardware resources. The *AR Comp* compares the digitized V_{RES} with multiple digital threshold levels (up to 10 here). It is worth noting that quantizing the voltage residue weakens, in principle, the theoretical advantages of a purely CT approach, i.e., negligible influence of amplitude errors on the SNR. However, timing errors of CT LCS ADCs also have a significant impact on performance, and often demand sophisticated compensation techniques [3]. Moreover, although the power consumption of the proposed ADC is less scalable versus input frequency compared to the CT counterpart in [3], it is still more flexible than in uniform-sampling ADCs and conventional LCS ADCs. An additional advantage is its DT output, which makes it suited to directly interface with the conventional DT DSPs.

III. Circuit Implementation

Fig. 2 shows the block diagram of the proposed ADC. The delta modulator loop consists of an analog part, which comprises the sw-cap feedback DAC, subtractor and 4-bit residue quantizer; and a digital part, comprising both the synthesized logic operating as AR comparator and U/D counter, as well as a custom control logic responsible for generating the event-based synchronous gating triggers used to control the DAC and subtractor. After the subtraction node, two cascaded low-gain amplifiers with passive load are

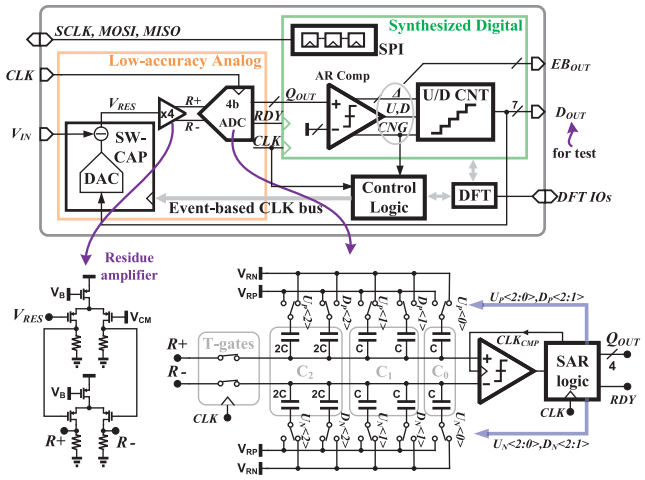

Fig. 2. Block diagram of the proposed AR quasi-LCS ADC architecture.

used to amplify by 4× the residue and to drive the 4-bit residue quantizer while isolating it from the "glitchy" sw-cap subtractor. Moreover, the residue amplifiers loaded by the input capacitance of the residue quantizer act as a 2nd-order anti-aliasing LPF with a cut-off frequency ~10 MHz. They also determine the quantization noise transfer function of the ADC, as well as the out-of-band peak magnitude of the signal transfer function at around 10 MHz, which is up to 10 dB; an ADC prefilter might therefore be needed in some cases to suppress potential input interferers around $f_{\mathrm{CLK}} \pm 10$ MHz, where $f_{\mathrm{CLK}} = 80$ MHz. Since uniform sampling only occurs at the residue quantizer, and considering the anti-aliasing filtering by the residue amplifier, residue aliases are sufficiently attenuated and do not impair the in-band performance of the residue quantizer. Therefore, the in-band performance of the proposed ADC will not be affected by residue aliases. Design for testability circuitry (DFT in Fig. 2) consists of an LVDS TX to probe digital signals and two test output operational amplifiers which probe the amplified residue voltages.

The 4-bit residue quantizer is implemented as a top-plate sampling asynchronous SAR ADC with split binary-weighted capacitive DAC (apart from the LSB capacitors C_0, which are not split). The unit capacitor is a 4.5-fF MOM-cap from the PDK, while the sampling switches are transmission gates and not bootstrapped, given the low amplitude of the amplified residue signal (below half the ADC full-scale). The comparator is implemented as a simple latch stage, while the SAR logic consists of only TSPC flip-flops and logic gates. The *CLK* is used only at this point of the system and the U/D counter, while the AR comparator in the synthesized digital logic is "clocked" by *RDY*. Two digital output formats can be transmitted off-chip: 1) the binary-coded input of the feedback DAC, D_{OUT} and 2) the event-based output (EB_{OUT}). The latter comprises the trigger *CNG*, which goes high if a level is crossed, with *U* and *D* indicating whether V_{IN} is increasing or decreasing, and Δ indicating the magnitude of the shift that D_{OUT} experienced during the *CLK* period.

The schematic of the sw-cap feedback DAC and subtractor, whose topology was inspired by [3], is shown in Fig. 3. The digital control signals involved are *clk*1, *clk*2, *s*0, and *s*1, all derived from the level-crossing trigger *CNG* and system clock *CLK*. There are two main operational phases: *track* and *update*. When a digital threshold level in the digital AR comparator is crossed, the signal *CNG* will be set to one, thus generating *clk*1 as a gated version of *CLK*. *clk*2 is likewise a nonoverlapping inverted replica of *clk*1. The update phase of the DAC is asserted by the rising edge of *clk*1. During this phase, bottom plates of the DAC capacitors are connected to V_{REFP} or V_{REFN}, depending

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART IN ADCS FOR COMPRESSED SENSING APPLICATIONS

	[3]	[4]	[5]	[9]	[10]	**This Work**
Topology	AR LCS	AR LCS	LCS	LCS	LCS	**AR LCS**
Need CT Comparator	Yes	Yes	Yes	Yes	Yes	**No**
Process (nm)	130	180	65	500	65	**28**
Area (mm^2)	0.3575	0.96	0.0036	0.06	0.3	**0.0126**
Power	9 μW	25 μW	2.3 mW	106 μW	30 mW	**205 μW**
BW	20 kHz	1 kHz	2.4 GHz	5 kHz	20 MHz	**1.42 MHz**
SNDR (dB)	47-54	52.2	25.3	31	59.9	**53.46**
FoM$_{W,peak}$(fJ/c-s)	549	37,600	32	365,700	929	**187**

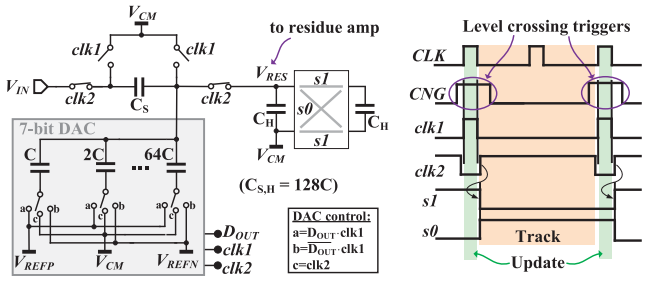

Fig. 3. Binary-weighted 7-bit DAC with sw-cap subtractor (left) and timing of control signals (right).

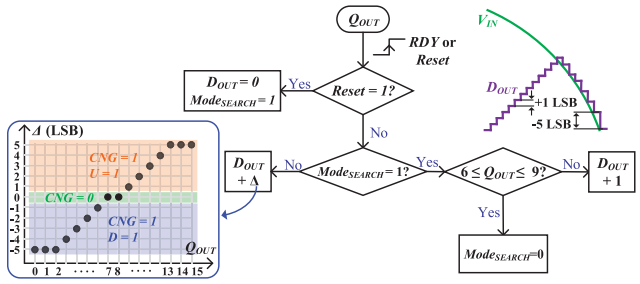

Fig. 4. Logic flow of the synthesized digital block.

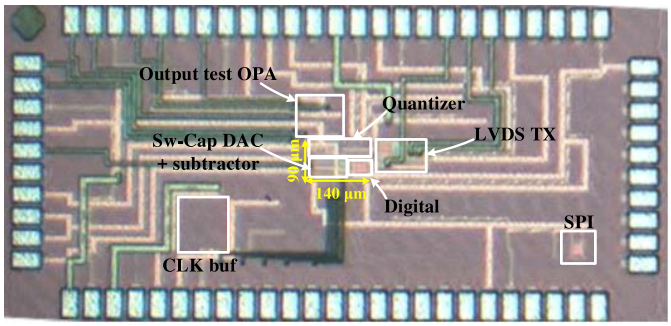

Fig. 5. Chip micrograph of the proposed AR quasi-LCS ADC.

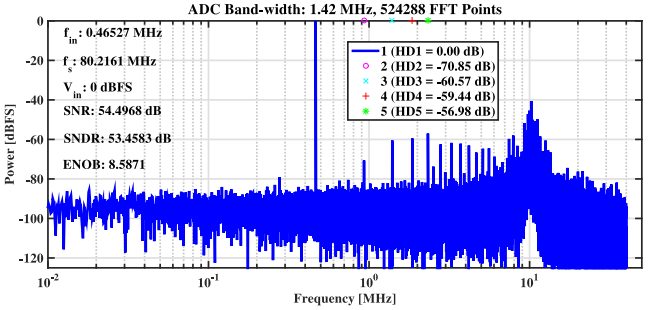

Fig. 6. Measured spectrum with a 465-kHz full-scale sinusoidal input.

on D_{OUT}, while the input capacitor C_s is disconnected from the input (V_{IN}) and V_{RES}, and shorted to V_{CM}. Moreover, the hold capacitor C_H maintains the value that V_{RES} node captured right before the end of the previous track phase. The sizes of the switches and unit capacitor are a tradeoff between the ADC low-frequency noise power and the DAC settling time behavior. The subtraction between V_{IN} and the sw-cap DAC output V_{DAC} is performed at the rising edge of *clk*2, which marks the beginning of the track phase. Synchronously to this, the control signals *s*0 and *s*1 also change state, inducing the flipping of the right-most C_H capacitor, thus removing the memory charge. During the track phase, V_{RES} is a CT signal and is equal to

$$V_{\mathrm{RES}}(t) = G_s \cdot [V_{\mathrm{IN}}(t) - V_{\mathrm{DAC}}] + V_{\mathrm{CM}} \tag{3}$$

where V_{DAC} is equal to $\mathrm{LSB}_{\mathrm{DAC}} \cdot \sum_{i=0}^{6}(D_{\mathrm{OUT}}[i] \cdot 2^i)$, with $\mathrm{LSB}_{\mathrm{DAC}}$ being the LSB amplitude of the 7-bit DAC. G_S is the gain of the subtractor, equal to 1/4. Considering a cascade of the subtractor, low-gain residue amplifier and 4-bit SAR quantizer as a standalone block (SAQ), we can express its LSB as

$$\mathrm{LSB}_{\mathrm{SAQ}} = \frac{V_{\mathrm{REF,ADC}}}{16 \cdot G_S \cdot G_A} \tag{4}$$

where $V_{\mathrm{REF,ADC}} = V_{\mathrm{RP}} - V_{\mathrm{RN}}$ (see Fig. 2) and G_A is the residue amplifier gain, nominally 4. Proper system operation demands $\mathrm{LSB}_{\mathrm{SAQ}}$ to be a good approximation of $\mathrm{LSB}_{\mathrm{DAC}}$. Given the ADC targeted specs, the challenge is the sw-cap DAC and subtractor, whose layout parasitics must have negligible impact on the converter nonlinearity.

The logic flow diagram of the synthesized digital block, including the AR comparator and U/D counter is depicted in Fig. 4. After the system reset (e.g., power-on reset, *Reset*), a *power-on* search mode is asserted ($\mathrm{Mode}_{\mathrm{SEARCH}} = 1$), and the U/D counter will continuously increment by 1 at the rising edge of each *CLK* pulse until Q_{OUT} reaches mid-scale (7 or 8), meaning that the feedback DAC output is within 1 LSB away from V_{IN}. This ends the *power-on* search mode and asserts the normal AR conversion mode ($\mathrm{Mode}_{\mathrm{SEARCH}} = 0$). In this operational mode, at the rising edge of *RDY*, the residue quantizer output Q_{OUT} is compared with the ten digital thresholds (9, ... 13 and 2, ... 6) of the AR comparator, which are the digital equivalent of the "levels" of an LCS ADC. Depending on where Q_{OUT} lies, the U/D counter output D_{OUT} is updated accordingly. The adaptive resolution range is from -5 LSB to 5 LSB. With the AR algorithm, the gross output bit rate can be reduced 3× at the edge of signal band with no appreciable SQNR degradation.

IV. MEASUREMENT RESULTS

The chip micrograph is presented in Fig. 5, showing the core ADC (sw-cap subtractor, residue amplifier, residue quantizer, and synthesized logic), occupying an area of 0.0126 mm^2 (140×90 μm^2),

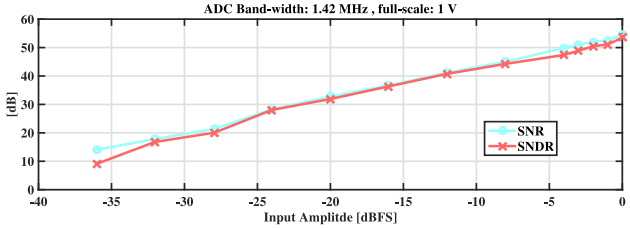

Fig. 7. Measured SNR and SNDR versus input amplitude of a 465-kHz sinusoidal input.

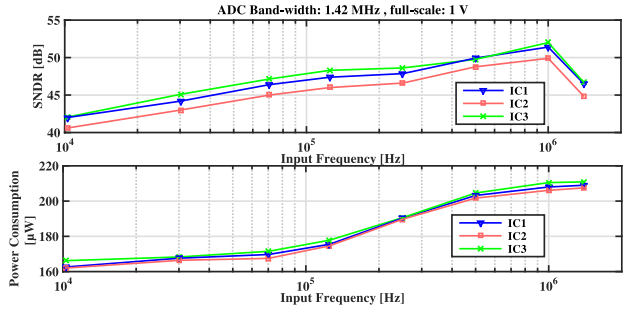

Fig. 8. Measured SNDR and power consumption of three ICs versus frequency of a −3-dBFS sinusoidal input.

as well as clock buffer and DFT. Fig. 6 shows the measured ADC output spectrum, achieving an SNDR of 53 dB with a full-scale input sinewave at 465 kHz. The noise power is dominated by the residue quantizer's quantization noise, which is oversampled by $f_{\mathrm{CLK}} = 80\,\mathrm{MHz}$ and shaped by the loop up to 10 MHz, allowing to exceed the 7-bit nominal resolution of the feedback DAC by 1.5 bits. The harmonics around 10 MHz are amplified by the loop gain up to 10 dB (but they do not get aliased!). Fig. 7 presents the measured SNR and SNDR versus input sinewave amplitude, while the characterization of SNR, SNDR, and power consumption versus frequency for a −3-dBFS sinewave is instead presented in Fig. 8, showing an overall good agreement among the three measured ICs. The gradual drop of SNDR at low frequencies is due to the fact that more harmonics, mainly arising from the feedback DAC's residual nonlinearity, fall into the signal band. It is also caused by the current leakage of switches at node V_{RES}, especially happening at <100-kHz input frequencies due to the long lack of activities between two consecutive level-crossing events. Despite the use of the clock, the proposed ADC still offers comparable power consumption and power scalability versus input frequency compared to most CT LCS ADCs and superior to uniform-sampling ADCs. Finally, Table I compares the proposed work with the state-of-the-art in ADCs for compressed sensing applications.

V. Conclusion

An AR quasi-LCS delta-modulator ADC which exploits voltage residue quantization using a 4-bit asynchronous SAR ADC was presented. The residue quantization allows a straightforward implementation of adaptive resolution level-crossing algorithm in the digital domain. By avoiding the use of high-performance analog comparators, timing errors no longer contribute to the ADC SNR, while amplitude quantization does not impair the performance. Its synchronous DT digital output makes it suitable to be directly interfaced to conventional DT DSPs.

VI. Acknowledgment

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