A Fully Synthesizable Fractional-*N* MDLL With Energy-Efficient Ring-Oscillator-Based DTC of Large Tuning Range

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***Abstract*—This letter describes a fully synthesizable fractional-*N* multiplexing delay-locked loop (MDLL) with a ring-oscillator-based digital-to-time converter (RO-DTC). The proposed RO-DTC can generate a wide range of time delays with only a relatively smaller number of delay cells. Since its structure is periodical, the corresponding predistortion look-up table (LUT)'s size could also be reduced. The proposed MDLL is implemented in a 65-nm CMOS process. The measured results show that the RO-DTC's power normalized by operating frequency and tuning range is the lowest among other state-of-the-art works. The proposed MDLL achieves FoMs of −242.3 and −218.6 dB in integer-*N* and fractional-*N* operation modes at RF frequencies 1.04 and 1.0465 GHz. The core area is 0.0892 mm^2.**

***Index Terms*—Analog mixed-signal system, digital-to-time converter (DTC), frequency synthesis, fully synthesizable circuit, multiplexing delay-locked loop (MDLL).**

I. Introduction

In fractional-*N* all-digital frequency synthesizers, digital-to-time converters (DTCs) are usually adopted to mitigate quantization errors from the modulation of dividers. The nonlinearity effect in DTCs is a major source of spurious signals. One method to solve the problem of DTC nonlinearity is to reduce the delay range requirement of DTC [1], [2], [3], [4]. However, these techniques introduce mismatches between interpolated/selected phases, and circuit structures are limited by fully synthesizable design's intrinsic limitations, like minimum-length devices' mismatch, asymmetric P&R, etc [5]. Another method is to modulate the divider and/or DTC's control words to randomize nonlinear errors and to reshape noise [6], [7], [8]. These techniques will either extend the required tuning range of DTCs, worsening their linearity, or require to make matched implementations of DTCs. To eliminate the nonlinearity of long tuning range, the designers would apply digital predistortion [9], [10]. However, predistortion of longer-range DTCs requires larger look-up tables (LUTs) with precise results or smaller LUTs but with errors of polynomial fitting. Although long-range DTCs generally have worse-jitter-power tradeoffs, they are applicable if suitable for suppressing nonlinearity.

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This letter proposes a fully synthesizable fractional-*N* multiplexing delay-locked loop (MDLL) with a ring-oscillator-based DTC (RO-DTC). The RO-DTC's structure intrinsically supports very long delay length, while the predistortion scheme is only required to maintain a small set of nonlinearity sources.

II. Proposed Mechanism

Conventional fully synthesizable delay-line-based DTCs utilize a series of delay cells with a selectable mechanism (e.g., a symmetric multiplexer (MUX) or path-selection switches) to generate desired time delays. An example is shown in Fig. 1(a). In comparison, the proposed RO-DTC uses a ring oscillator (RO) as a "folded" delay line, as shown in Fig. 1(b). The counter counts the number of RO's output cycles and makes comparisons to the cycle control word D_{C}. When the number of cycles reaches D_{C}, the symmetric MUX is enabled, and the RO units' outputs are selected by the unit control word D_{U} to generate the desired time delay. The overall time delay can be ideally calculated as $T_{\mathrm{total}} = T_{\mathrm{u}}(N_{\mathrm{RO}}D_{\mathrm{C}} + D_{\mathrm{U}})$, where T_{u} is the unit delay of the RO, and N_{RO} is the number of RO stages. The maximum tuning range of the RO-DTC could be then expressed as $T_{\mathrm{TR}} = T_{\mathrm{u}}(N_{\mathrm{RO}}N_{\mathrm{CNT}} - 1)$, where N_{CNT} is the maximum available number of the counter.

The design of the proposed circuit minimizes elements that contribute to nonlinearity. It achieves this by decreasing delay stages, inherently reducing mismatches between them. Additionally, it lessens the complexity of designing the symmetric MUX or the highly matched switch series. A corresponding calibration scheme, which utilizes the reduced number of mismatch sources, is also discussed.

III. Circuit Implementation

A. MDLL System Architecture

Fig. 1(c) shows the overall MDLL system architecture. An FLL path is also implemented and controls the DCO's coarse bank, although not shown in the figure. The output frequency is between 900 MHz and 1.2 GHz with a reference signal of 104 MHz.

The MDLL uses a 7-unit RO-DTC as the coarse DTC. A conventional digital control module of DTC generates a 7-bit control word. Then a decoder designed for the proposed RO-DTC converts it to D_{C}'s inversed thermal-coded form $D'_{\mathrm{C,th}}$ and D_{U}'s one-hot-coded form $D_{\mathrm{U,oh}}$ with maximum values of 18 and 6, respectively, $(19 \times 7 > 2^7)$. A shift comparator is designed as a counter and a comparator. A 7-bit thermal-coded fine DTC is designed for fine-tuning the time delay and applying predistortion for the RO-DTC.

The `INJ_EDGE` and the `DCO_FB` signals are connected to the DCO's MUX and the SS-BBPD. To minimize the timing offset between the MUX and the SS-BBPD, they are synthesized to be close to each other with P&R constraints of symmetry.

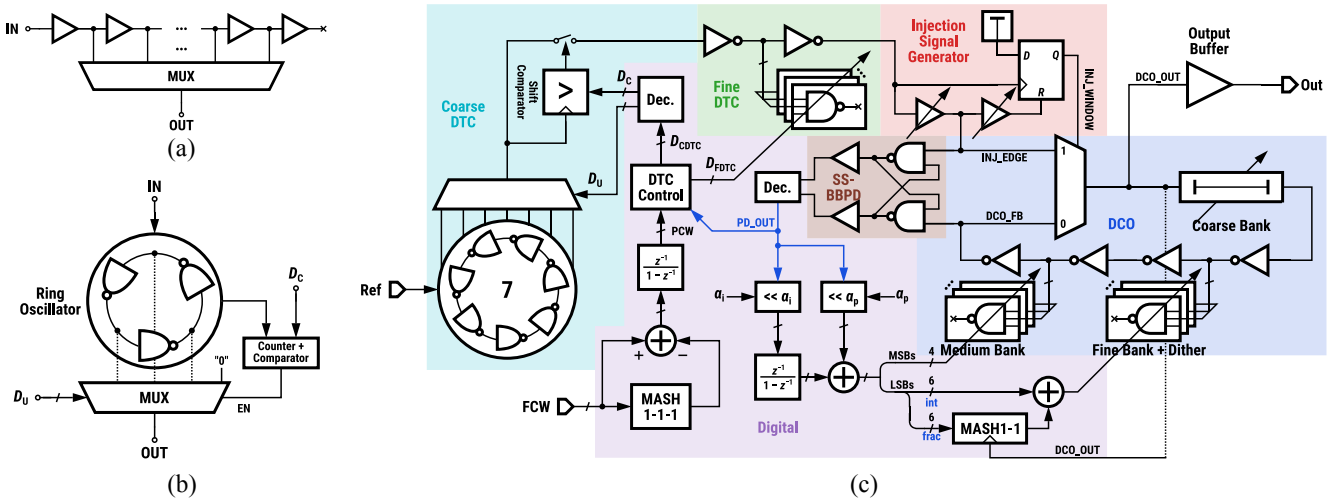

Fig. 1. (a) Example of fully synthesizable delay-line-based DTC. (b) Conceptual diagram of the proposed RO-DTC. (c) System architecture of the proposed MDLL. The thermal-coded banks' decoders and the FLL path are omitted from the diagram.

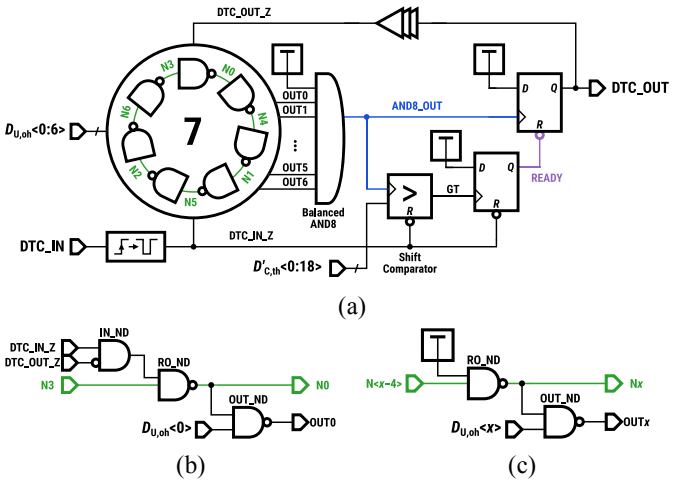

Fig. 2. (a) Circuit implementation of the proposed RO-DTC, with schematic of the (b) zeroth node and the (c) xth nodes, where $1 \le x \le 6$, $x \in \mathbb{Z}$.

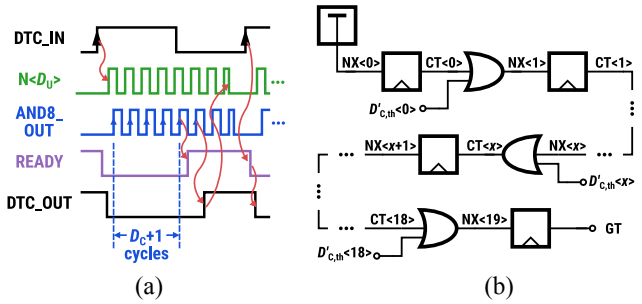

Fig. 3. (a) Waveform of the RO-DTC. (b) Schematic of the shift comparator. The clock and reset signals in each DFF are omitted.

B. RO-DTC

Fig. 2(a) shows the structure of the RO-DTC. Fig. 2(b) depicts the 0th node, and Fig. 2(c) depicts the xth node, where $1 \le x \le 6$, $x \in \mathbb{Z}$. Those are nodes inside the RO. Each node contains a NAND3 gate named RO_ND as the gate in the RO loop, an output gate named OUT_ND as the output node, and an input gate, which is IN_ND in the 0th node and a TIE_HIGH gate in the xth node. The output gate OUT_ND and the balanced AND8 gate function together as the balanced MUX. The input gate IN_ND ties the node N0 to high and consequently, other Nx nodes to low or high, respectively, when idle. When the DTC receives a rising edge from DTC_IN, it turns to a negative impulse in DTC_IN_Z and it "loosens" the nodes N0 to N6 and the RO starts oscillation. Note that, to make the next rising edge of Nx to be in N$\langle x+1 \rangle$, the naming order of the RO loop nodes is not in the schematical order.

The waveform of the RO-DTC is shown in Fig. 3(a). AND8_OUT, which is the output signal of the balanced MUX (again, which is combined with the output gates OUT_ND and the balanced AND8) drives a shift comparator. When the shift comparator completes shifting of D_C times, the signal GT rises and sets the signal READY to high through a D flip-flop (DFF). When the next rising edge of AND8_OUT comes, the output signal DTC_OUT is triggered through the next DFF. To cut down power consumption of the RO, when the signal DTC_OUT rises, the RO also locks by setting N0 to high until the next rising edge of DTC_IN comes.

The structure of the shift comparator is shown in Fig. 3(b) with the clock and reset signals omitted. When the shift comparator starts working, the comparator propagates "1"s toward the node GT. So we can set the thermal-coded signal $D'_{C,th}$ to be $\overbrace{00\ldots00}^{D_C\text{"0"}s}\ \overbrace{11\ldots11}^{(18-D_C)\text{"1"}s}{}_2$ to let the shift comparator shifts "1"s to the left by D_C clock cycles and then trigger GT. If a longer tuning range of DTC is required, the length of the shift comparator can be vastly extended thanks to its extensible structure, with the only limitation in constructing its clock tree.

By selecting the RO stage number to 7, the oscillator frequency becomes 4.65 GHz in simulation with post-layout NAND3 models. With this frequency, the logic gates and the DFFs in the RO-DTC can work correctly. Also, keeping the RO stage number to 7 makes the RO-DTC's structure and predistortion LUT compact and simplifies the implementation of the digital decoder and the balanced MUX. Note that because of the parasitics on the supply network and ground, the RO-DTC's resolution may have fluctuations in the first few cycles. Stronger supply networks and larger on-chip decoupling capacitance are required in the layout. During the physical synthesis of the RO-DTC, the RO elements, balanced AND8 elements, and the last stage of the input buffers were calculated to be as symmetric as possible

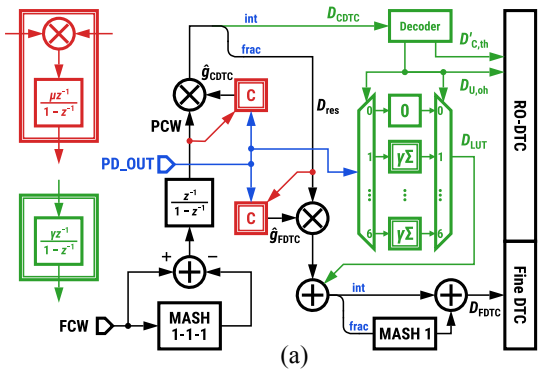

Fig. 4. (a) Diagram of fractional-N operation control and calibration. The structures of its accumulator and correlator are shown on the left. Time delays are omitted. (b) Simulated convergency transient of DTC calibration. Values are multiplied by factors for better visualization.

and were placed in a 19×19 grid in the script of relative placement (RP).

C. Digital Processing for Fractional-N Operation

Nonlinearity of the DTC caused by mismatches still exists because of round-off errors during placement, irregular routing, and mismatches of manufacturing. We propose a DTC control and calibration scheme, which is depicted in Fig. 4(a). The frequency control word FCW is fed to the MASH 1-1-1 modulator for fractional-N operations. The residue then accumulates to phase control word PCW. By multiplying the estimated coarse DTC gain $\hat{g}_{CDTC}$, the raw coarse DTC control word D_{CDTC} and residue D_{res} is calculated. On the coarse DTC control and predistortion path, which is colored green in Fig. 4, the decoder decodes D_{CDTC} into $D'_{C,th}$ and $D_{U,oh}$ and sends the results to the RO-DTC. $D_{U,oh}$ is also sent to the predistortion LUT, which records the deterministic jitter of the RO-DTC depending on D_U. The LUT values are selected by the current time step's D_U as its output D_{LUT}. On the other path, the fine-DTC-gained residue $\hat{g}_{FDTC}D_{res}$ is added to LUT's output D_{LUT}. After a MASH 1 modulator, the resulting fine DTC control word D_{FDTC} is output to its analog counterpart. All the digital calibrations start after phase lock. Because the correlated signals of the calibrations are different and uncorrelated to each other, the calibration loops do not conflict. Fig. 4(b) shows the simulated convergency transient. The injection starts after the calibration finishes. Note that the MUX and the SS-BBPD asymmetry might introduce an offset to the calibration scheme. A solution to mitigate this offset is shown in [10].

IV. Measurement

The chip is manufactured in TSMC 65-nm CMOS technology. All the active circuits, except I/O buffers and ESD modules, are implemented with a commercial 65-nm digital standard cell library.

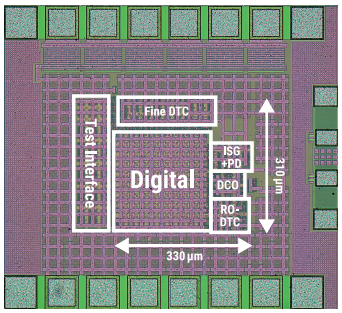

Fig. 5. Die photograph.

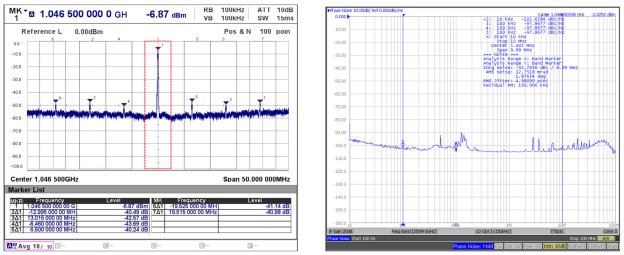

Fig. 6. (a) Measured spectrum and (b) measured phase noise in fractional-N mode with RF frequency of 1.0465 GHz.

TABLE I
Comparison Table of State-of-the-Art Fractional-N Fully Synthesizable PLLs

Journal/ Conference	**This Work**	[11] JSSC'23 K. Kwon	[12] JSSC'21 S. Kundu	[13] SSC-L'20 B. Liu
Process	**65 nm**	12 nm	22 nm	5 nm
Injection?	**Yes**	Yes	Yes	Yes
Reference Frequency (MHz)	**104**	40	80	40
Integrated Jitter (ps)	**4.98**	4.7	2.74	2.99
Output Frequency (GHz)	**1.0465**	2.4006	3.6175	1
FoM (dB)	**−218.6**	−220.6	−226.2	−232.6
Reference Spur (dBc)	**−35.1**	−45.6	−60	−37.1
Worst Fractional Spur (dBc)	**−40.2**	−30	−47	−43.8
Power (mW)	**5.52**	3.91	3.19	0.615
Supply (V)	**1**	0.8	N/A	0.75
Active Area (mm^2)	**0.0892**	0.063	0.00525	0.0036

The chip photograph is shown in Fig. 5. The total core active area is 0.0892 mm^2 except for the SPI test interface and the output buffer.

The chip is measured in 1.0-V supply voltage. The reference frequency is 104 MHz, eight times the commonly used crystal oscillator's frequency of 13 MHz. In the measurement of integer-N mode at 1.04-GHz output frequency, the MDLL has 435 fs output jitter and −33.1 dBc reference spur, with a power consumption of 3.08 mW. The large reference spur is mainly caused by weak isolation between the RO-DTC and digital modules. In the fractional-N mode at 1.0465-GHz output frequency, the system performs 4.98 ps output jitter and −40.2 dBc fractional spur, with a power consumption of 5.52 mW, in which the RO-DTC consumes 1.44 mW. The large jitter in the fractional-N mode might mainly caused by power supply fluctuations, which leads to malfunctioning of digital predistortion of the period of 7. The measured fractional-N spectrum and phase noise is shown in Fig. 6. The comparison table of the proposed MDLL in fractional-N and other synthesizable MDLLs is shown in Table I.

The measured resolution of the RO-DTC is 37.64 ps, with a full tuning range of 4817.9 ps, which could cover more than 4 DCO cycles

TABLE II
COMPARISON TABLE OF STATE-OF-THE-ART (COARSE) DTCS

Journal/ Conference	**This Work**	[15] ISSCC'18 H. Liu	[10] TCAS-I'21 B. Liu	[2] JSSC'19 A. Santiccioli
Technology	**65 nm**	65 nm	65 nm	65 nm
Synthesizable?	**Yes**	No	Yes	No
Reference Frequency (MHz)	**104**	52	100	100
Supply (V)	**1**	1	1.2	1.2
DC Power (mW)	**1.44**	0.098	0.817	0.5
Bit Width	**7**	10	6	N/A
Resolution (ps)	**37.64**	0.58	33.20	N/A
Tuning Range (ps)	**4817.9**	610	2125*	303
Jitter (fs)	**287.4**	630	N/A	230
Normalized Power (mW)**	**2.9**	3.1	3.8	16.5

* The denoted tuning range is calculated from its resolution and bit width described in the papers.
** Normalized power $P_{\mathrm{norm}} = P_{\mathrm{DC}}/(f_{\mathrm{ref}} \cdot T_{\mathrm{TR}})$, where f_{ref} is reference frequency and T_{TR} is the maximum tuning range.

and could work with MASH 1-1-1 modulation. The comparison table of the proposed RO-DTC and other DTCs, whether synthesizable or not, is shown in Table II. Since the power consumption of the DTCs has linear dependencies with both the reference frequency and the tuning range [14], we can calculate the normalized power consumption as $P_{\mathrm{norm}} = P_{\mathrm{DC}}/(f_{\mathrm{ref}} \cdot T_{\mathrm{TR}})$, where f_{ref} is reference frequency and T_{TR} is the tuning range. The comparison table shows that the proposed RO-DTC, which has a normalized power consumption of only 2.9 mW, is more energy-efficient than the other DTCs.

V. CONCLUSION

In this letter, we developed a fully synthesizable MDLL with a long-tuning-range RO-DTC. The proposed RO-DTC, with its corresponding digital processor, has a compact structure. The proposed MDLL achieves FoMs of -242.3 and -218.6 dB in integer-*N* and fractional-*N* operation modes at RF frequencies 1.04 and 1.0465 GHz. The RO-DTC achieves a normalized power consumption of 2.9 mW, the lowest among other state-of-the-art works.

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