A BiCMOS Active Quencher Using an Inverter-Based Differential Amplifier in the Comparator

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***Abstract*—For fast switching off of a firing single-photon avalanche diode (SPAD), an active quenching circuit in 0.35-μm BiCMOS technology with a very fast quenching slew rate is introduced. Quenching transients measured at an integrated small prober pad are shown. An NPN transistor as quenching switch leads to an active quenching time of 250 ps and a quenching slew rate of 21.1 V/ns. A self-biased two-inverter differential amplifier used in the comparator makes this fast quenching possible. By the implementation of cascoding, the excess bias voltage of the integrated SPAD can be doubled to 6.6 V with respect to the nominal supply voltage of 3.3 V of the BiCMOS process used. Active resetting of the SPAD is achieved in 725 ps. The power consumption of the BiCMOS quenching circuit is 16.3 mW at 40 Mcounts/s and 3 mW in the idle state.**

***Index Terms*—Active quenching, BiCMOS, comparator, integrated photodiode, self-biasing, single-photon avalanche diode (SPAD).**

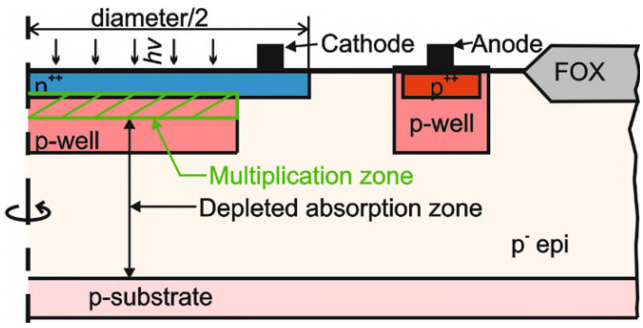

Fig. 1. Cross section of SPAD with thick absorption zone.

I. Introduction

Single-photon avalanche diodes (SPADs) are very important for sensors, which have to work at very low-light levels down to the detection of single photons. However, they are affected by dark counts and afterpulsing, i.e., to show photon detections where no photon was absorbed [1]. The photon detection probability (PDP) increases with the excess voltage, however, at also higher-dark count rate (DCR) and larger afterpulsing probability (APP). APP can be reduced with longer dead time, however, limiting the detection rate. Both, dark counts and afterpulses limit the sensitivity of SPAD-based receivers [2]. However, it is well known that fast active quenching reduces the avalanche charge flowing through the SPAD and therefore decreases the APP [3], [4], [5]. In [4], with an ultrafast quenching circuit in 28 nm fully depleted SOI CMOS, a reduction of the APP by 50% was reported.

Many active quenching circuits (AQCs) in CMOS technology were described in literature [4], [5], [6], [7], [8], [9]. A 50-μm diameter p^+/n-well SPAD was quenched from an excess bias of 9 V within 1 ns by an AQC in 0.18-μm high-voltage CMOS [6]. The APP of a so-called RE-SPAD was larger than 10% at a dead time of 12.5 ns [6]. For a 10-μm diameter SPAD at an excess bias of 3.5 V, a quenching time of 0.7 ns was reported with an AQC in standard 0.18 μm CMOS [7].

A cascoded AQC in 0.35-μm CMOS applying 5-V transistors showed simulated reaction and subsequent quenching times of 0.8 ns and 0.61 ns (total quenching time of 1.4 ns) for a 40-μm diameter SPAD and an excess bias of 9.9 V [8]. The measured total quenching time was 1.7 ns and the quenching slew rate was 7 GV/s [8]. A dead time of 30 ns was necessary for an APP of 2.1%. For a p^+/n-well SPAD with an active area of 90 μm^2 and an excess voltage of 0.5 V the simulated quenching time was 0.1 ns with an AQC in 65 nm CMOS [9]. The simulated quenching time of a p-well/n-well SPAD with an active diameter of 13 μm from an excess bias voltage of 1.8 V was about 0.4 ns in 0.18-μm CMOS [10].

The motivation for the development of BiCMOS processes was the superiority of bipolar analog circuits due to a higher transconductance and a better-driver capability of bipolar junction transistors (BJTs) compared to MOSFETs [11]. Bipolar transistors therefore will speed up AQCs. Discrete BJTs [3], [12] and bipolar standard components [13] were used in AQCs. AQCs with bipolar transistors in BiCMOS quenching circuits were exploited in [14] and [15]. A 25-μm diameter off-chip InGaAs SPAD was actively quenched from an over-voltage of 5.5 V in 920 ps according to post-layout simulation with a BiCMOS AQC dissipating 30 mW [15]. A 55 nm Bipolar-CMOS-DMOS (BCD) process was only used for the implementation of an SPAD using a pure CMOS AQC [16]. We used bipolar transistors in the comparator of an AQC in 0.35-μm BiCMOS to reduce the reaction time [17]. In this letter, we replace the bipolar differential amplifier of [17] by an inverter-based differential amplifier and apply a bipolar transistor as quenching transistor. The SPAD is shortly introduced in Section II. Section III describes the AQC, Section IV depicts measured results, and Section V concludes this letter.

II. Structure of SPAD

The integrated SPAD (see Fig. 1) is fabricated on a wafer carrying an about 12 μm thick epitaxial layer with a boron concentration of about 2×10^{13} cm^{-3}. This epitaxial layer is exploited as thick absorption zone. The bulk of the wafer (p-substrate, see Fig. 1) is highly boron doped. The circular SPAD has an active (p-well) diameter of 29 μm. A 1.5 μm wide virtual guard ring. (The n^+ diameter is 32 μm.) prevents premature edge breakdown. No process modifications were needed.

The reach-through SPAD was described in detail in [18] and [19]. Only 19 V are needed to deplete the thick absorption zone fully [18].

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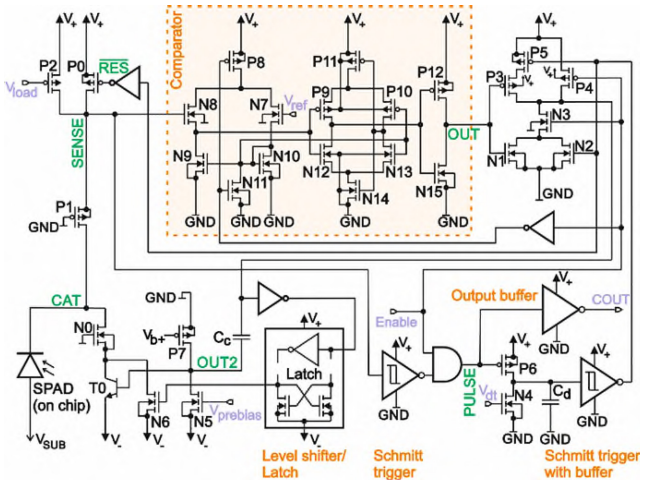

Fig. 2. Circuit of AQC.

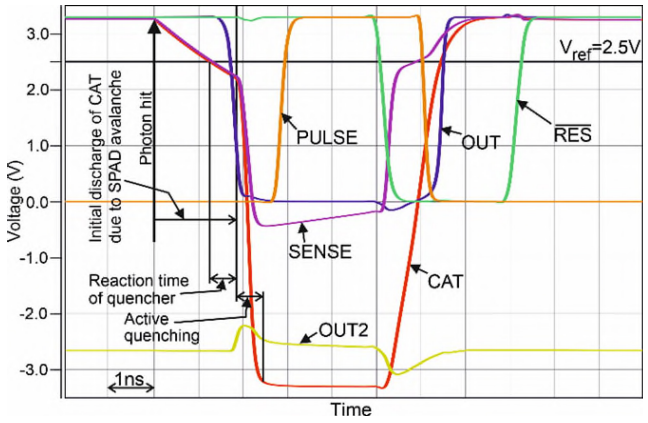

Fig. 3. Simulated waveforms at important nodes. $V_{\mathrm{ref}} = 2.5$ V was chosen for a better visibility of waveforms.

The capacitance of the SPAD used here is 15 fF according to device simulations with ATLAS [20]. The PDP of the SPAD achieves its maximum (35%) at a wavelength of 635 nm with an excess voltage of 6.6 V [19].

III. Quenching Circuit

Fig. 2 shows the schematic diagram of the BiCMOS active-quenching, active-resetting circuit. The circuit uses $V_+ = +3.3$ V and $V_- = -3.3$ V. T0 is a bipolar NPN transistor serving as quenching switch. Because of the uncomplicated usage of MOSFETs as cascode transistors, the N0 cascodes T0 to enable an excess bias of 6.6 V although the bipolar and MOS transistors were developed for a supply voltage of only 3.3 V. The resetting switch P0 is cascoded with P1 accordingly. The cascode configuration of the T0/N0 quenching and P0/P1 reset-ting switches ensures that these four transistors never leave the safe operation ranges although the voltage swing of the cathode node (CAT) and therefore the excess bias V_{ex} of the SPAD can be 6.6 V. To operate the SPAD in the Geiger mode with the maximum $V_{ex} = 6.6$ V, its anode, i.e., the substrate of the chip V_{SUB}, has to be connected to $-V_{\mathrm{BD}} - |V_-| = -V_{\mathrm{BD}} - 3.3$ V. Then it still can be quenched to the breakdown voltage V_{BD}. All transistors are located inside a deep n-well for isolation from V_{SUB}.

The comparator consists of a level-shifting stage (P8, N7–N10), a special differential amplifier (P9–P11, N12–N14) and the inverter formed by P12 and N15 acting as a driver stage. In the level-shifter, N7 and N8 are source followers to transfer the cathode potential (e.g., 3.25 V) to $\approx V_+/2$, where the decision threshold of the differential amplifier is located. Current mirror N9/N10 adjusts the currents in N7 and N8 automatically, i.e., saving constant current sources. Switches P8 and N11 enable/disable the level shifter and thereby photon detection.

This differential amplifier is simplified compared to [21] and uses two matched inverters (P9/N12 and P10/N13), which are (self-)biased via a negative feedback with P11 and N14. P11 and N14 work deep in the ohmic region in order not to reduce the output swing of the inverters [22]. This improves the performance with respect to PVT. This amplifier was called complementary self-biased differential amplifier (CSDA). Since the gain of this CSDA is nearly equal to that of an inverter, we prefer to call it "self-biased two-inverter differential amplifier (STIDA)." Its main advantages for the application in the AQC besides self-biasing are its high gain and its almost rail-to-rail swing. The simulated input-referred noise voltage of the comparator is 1.58 $\mathrm{mV_{rms}}$. Inverters P12/N15 and P3/N1 effectively drive the base of the quenching transistor T0 with pulses, which are generated due to coupling via capacitor C_C.

After quenching and the hold-off time, the cathode of the SPAD (CAT node) is charged to V_+ with P0. Subsequently, P0 is turned off to wait for a photon. If a photon triggers an avalanche, the avalanche current grows. Since P1 and P2 are conducting (P2 is set by V_{load} as an active resistor), the voltage drop across P2 increases (P0 is off) during this passive quenching phase and the voltage at the sense node undercuts the detection threshold V_{ref} of the comparator. The output (OUT, see Fig. 3) of the comparator, which uses the STIDA (see Fig. 2) instead of BJTs to save electrical power compared to [17], then switches to "low" and turns on P3. The rising slope at the drain of P3 is coupled via C_c to the base of T0 and turns it on. Active quenching starts and the CAT node is drawn down to V_-.

Prebiasing the base of T0 with P7 and N5 reduces the charging time of node OUT2 and reduces the reaction time of the AQC. Via an inverter and the Level shifter/Latch (see Fig. 2), a nMOS transistor (N6) with a width of 1μm and minimum length is switched on somewhat delayed. N6 pulls node CAT to a defined potential near V$_-$ when T0 is turned off again a short time after quenching. Due to dynamically coupling, the potential at OUT2 returns to its steady-state value, which is defined by P7/N5. Thus, the power consumption for active quenching is reduced. The dead time is mostly defined by C_d and can be controlled by V_{dt} setting the current in N4. The dead time is minimum (7.1 ns) for $V_{dt} = 3.3$ V. When P5 is switched off (N2 is turned on) by the Schmitt trigger connected to C_d, the CAT node starts to be charged again to V_+ by P0 for a new photon detection. T0 is kept off. After a certain delay P0 is switched off and the SPAD can detect the next photon. The minimum duration of the whole cycle is 7.1 ns.

The simulated power dissipation of the proposed AQC, including output driver is 16.3 mW for 40 MCounts/s, which is by a factor of 3.56 less than that of the AQC exploiting a bipolar differential amplifier in the comparator [17]. In the idle state, enabled and waiting for a photon, the AQC consumes 3 mW.

The AQC with integrated SPAD (see Fig. 4) was fabricated in XFAB 0.35 μm PIN-photodiode CMOS with appended NPN process module. The AQC has an active area of 27900 $\mu\mathrm{m}^2$ without SPAD, prober pad of 1764 $\mu\mathrm{m}^2$ and output driver.

IV. Measured Results

The prober pad (see Fig. 4) with a capacitance of $\approx$30 fF was contacted with a Picoprobe Model 35 having an input capacitance of 50 fF. The total capacitance T0 had to discharge during the

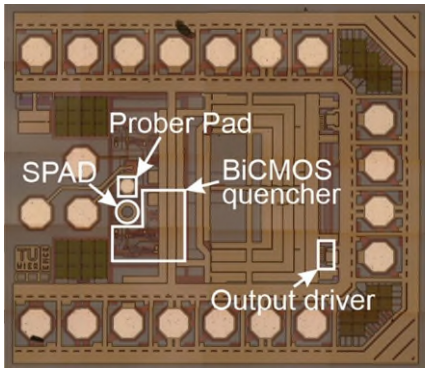

Fig. 4. Chip micro-photograph of the proposed active quenching chip.

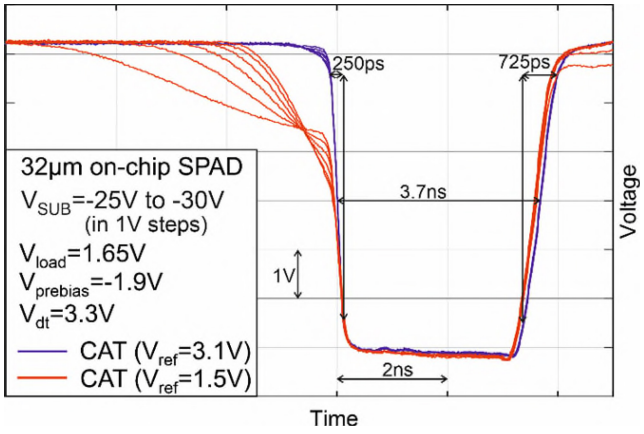

Fig. 5. Measured transient response at the CAT node.

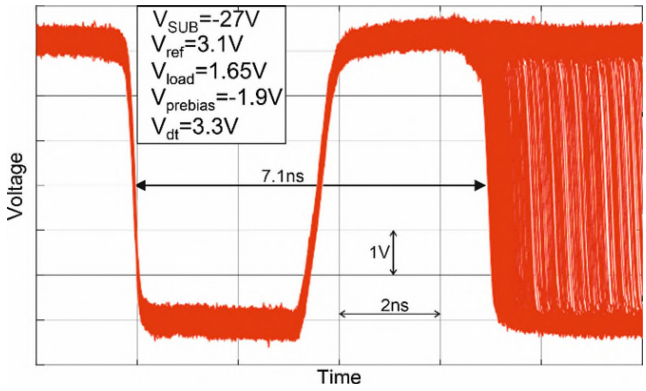

Fig. 6. Overlayed measured transients at the CAT node for random interphoton arrival times.

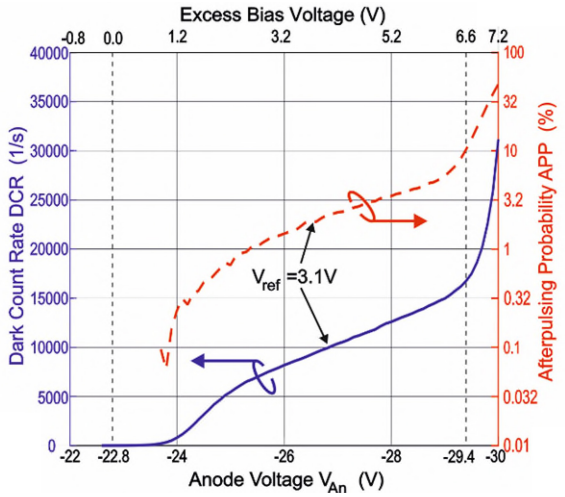

Fig. 7. Measured DCR and APP.

measurements of the transients was 130 fF, including SPAD, prober pad, picoprobe, and parasitic capacitances of the circuit. A keysight oscilloscope MSOV204A recorded the measured transients. Dark counts (and their after-pulses) were used with the device under test inside of a dark box. A Peltier element held the temperature of the chip constant at 25 °C during the measurements. Fig. 5 presents the measured transients for V_{SUB} from -25 to -30 V, i.e., for excess voltages from 2.2 to 7.2 V for $V_{\mathrm{BD}} \approx 26.1$ V. The measurements were done for the lowest-possible detection threshold of 0.2 V, i.e., for the reference voltage $V_{\mathrm{ref}} = 3.1$ V, because there the passive quenching time (from photon absorption to the transient crossing V_{ref}) is shortest. The 90%–10% fall time during active quenching is 250 ps as marked in Fig. 5. This value is by 230 ps shorter than that of 480 ps of a pure CMOS AQC in the same 0.35-μm technology with an 80-μm diameter SPAD having a capacitance of 80 fF [23]. It has to be mentioned that these 480 ps were simulated (due to the lack of a prober pad in [23]) and therefore may be too optimistic. Compared to the BiCMOS AQC of [17] with a wide NMOS quenching transistor and a quenching time of 550 ps, the bipolar transistor T0 reduces the quenching time by 300 ps. The slew rate of the AQC suggested here during active quenching is 21.1 V/ns. Active resetting takes place within 725 ps. After 7.1 ns the next photon can be detected enabling a maximum count rate of 140 Mcounts/s (see Fig. 6, no shorter photon interarrival times were observed). After a quench duration of 3.7 ns (see Fig. 5) the logic needs additionally approx. 2.7 ns (defined by the current in N4 and C_d) to be ready for a new photon detection. This delay of 2.7 ns is unnecessarily long from a circuit point of view and could be reduced by 2.5 ns. Adding the passive quenching and the reaction time of the comparator sums up to 7.1ns in Fig. 6.

The measured DCR and after-pulsing probability are depicted in Fig. 7 with V_{ex} in steps of 0.1V and for a measurement time of 10 s at each V_{ex}. The APP was obtained using the method of photon interarrival time [24]. At $V_{ex} = 6.6$ V, the APP is 10.3% for a dead time of 7.1 ns.

V. Comparison and Conclusion

The implementation of a bipolar transistor as quenching switch speeds up active quenching considerably compared to pure CMOS AQCs. An active quenching time of 250 ps and a quenching slew-rate of 21.1 V/ns are observed thanks to the bipolar quenching switch and to the STIDA. Compared to an AQC exploiting a bipolar differential amplifier, which needed source followers for level shifting, as comparator in the same 0.35-μm BiCMOS technology [17], the power dissipation is reduced by a factor of 3.56. The quenching time of the active quencher in 0.35-μm BiCMOS is 2.8 times shorter than that of an AQC in 0.18-μm CMOS from [7], whereby the BiCMOS AQC handles an excess bias of 6.6 V compared to 3.5 V. The lower price of 0.35-μm BiCMOS compared to 0.18-μm or nanometer CMOS, particularly in low-volume ASIC fabrication due to a large difference in the mask costs, should also be mentioned. The AQC is expected to improve APP and bit error ratio of SPAD-based receivers.

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