A Fetal-Movement Circuit Harvesting High-Energy Plasma During Fabrication, Concept, and Its Application to Self-Programming PUF

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***Abstract*—This letter presents a concept of a circuit harvesting high-energy plasma and operating during its semiconductor fabrication process, namely, fetal-movement circuit (FMC). The plasma current collection antenna is designed to be a comb shape for area saving. This enables the FMC related circuits to be placed within a dicing street for suppressing its area penalty to be almost zero. A self-programming oxide-breakdown physically unclonable function (PUF) has been implemented as one of the FMC applications. The successful PUF programming operation during fabrication has been demonstrated.**

***Index Terms*—Energy harvesting, fetal movement, plasma, self-programming physically unclonable function (PUF), semiconductor fabrication.**

I. Introduction and Concept Proposal

A physical computer shape is mainly restricted by its energy source. A desktop computer is a large rectangular tower shape and fixed in a room because it is powered by a 100–200 V at 50/60-Hz wall-mounted AC outlet and a high-voltage high-power bulky AC-to-DC converter is required as a power supply unit. By utilizing a high-capacity compact battery as the energy source, the computer could be implemented in a notebook, a pad, a watch, and even a ring shape. A wireless power delivery scheme utilizing on-chip coil can even realize a powder-shaped computer [1]. If an existing high-energy source yet unexploited by the computer is found, a new computer shape and functionality could emerge.

As the unexploited existing high-energy field, this letter discovered high-energy plasma in a semiconductor fabrication process (Fig. 1). Plasma-based reactive ion etching (RIE) is one mainstream etching instrument in the semiconductor fabrication. The high-energy plasma ions are used to process silicon and metal layers but, as well-known as an antenna effect, the ion charging current during the metal layer etching process is strong enough to breakdown a transistor gate oxide. By harvesting stable power from this high-energy etching plasma, a computing circuit operating during its fabrication process can be realized, namely, fetal-movement circuit (FMC).

This letter is an extended version of the ISSCC conference paper [2]. In the next Section II, FMC antenna and circuit design details will be described. The antenna layout optimization and the antenna/circuit placement strategy will be introduced for FMC area penalty saving. As one of the FMC demonstrators, self-programming oxide-breakdown physically unclonable function (PUF) circuit will be proposed. Section III will present measurement results of preliminary PUF core characterization and FMC-based self-programming operation. Finally, concluding remarks will be drawn in Section IV.

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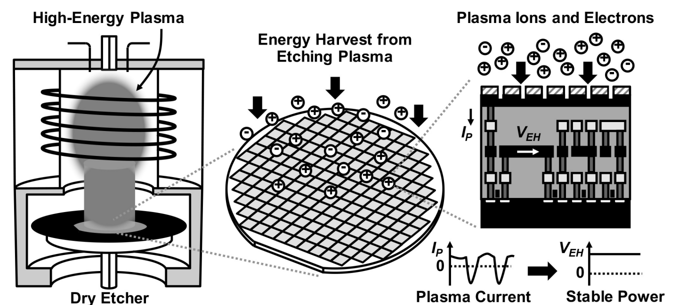

Fig. 1. Conceptual sketch of FMC.

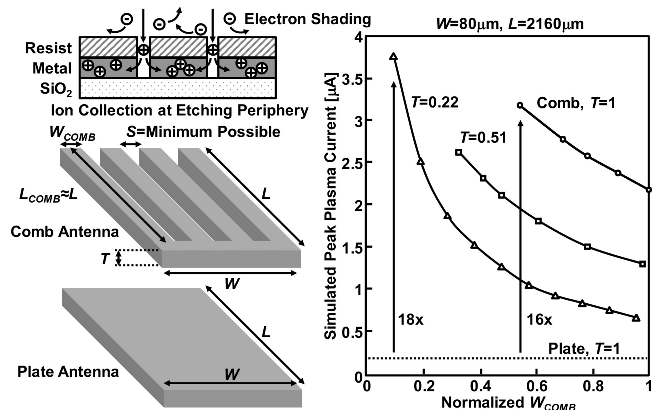

Fig. 2. Antenna layout and simulated plasma ion injection current. W_{COMB} and T_{NORM} are normalized with the maximum metal thickness available in the process.

II. Antenna and Circuit Design

A. Antenna Layout Optimization

A metal layer during the plasma etching process collects plasma ions and acts as an energy harvesting antenna. In this plasma-current collection antenna, the plasma ions are injected through at the etching periphery of the metal layer. A comb-shaped antenna would be the best-design choice for maximizing the etching peripheral area and hence the plasma ion injection current (Fig. 2). The etching peripheral area of the comb antenna A is given by

$$A = 2(nL + W)T \tag{1}$$

where L is the antenna length, W is the total antenna width, T is the antenna metal thickness, and n is the number of the comb teeth. n is expressed as

$$n = \frac{S + W}{S + W_{\text{COMB}}} \tag{2}$$

where W_{COMB} is the comb teeth width, and S is the space between the comb tooth. In order to maximize A under limited L and W

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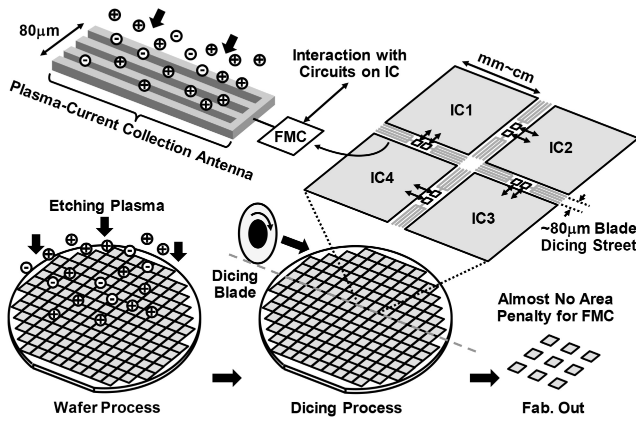

Fig. 3. FMC layout strategy utilizing dicing street.

layout area resources, n should be maximized. Both S and W_{COMB} should be then minimized to increase n, however the minimum S and W_{COMB} available in the fabrication process is restricted by the process parameter T. Under a given condition allowed in a design rule, proper choice of metal layer thickness is therefore needed to maximize n and hence A. Based on a classic etching plasma current model [3], the peak plasma current collected by the comb antenna was simulated in Fig. 2. In a particular fabrication process used in this letter, the best-metal layer thickness option was found to be 22% of the maximum metal thickness available in the process. In this best-metal options in the process used in this letter, the minimum S and W_{COMB} both approach $T/2$. The maximum etching peripheral area is approximated by

$$A = 2\left(\frac{\frac{T}{2}+W}{T}L + W\right)T \approx L(T+2W). \tag{3}$$

With the given area of 80 μm × 2160 μm for the antenna, >3-μA current can be collected which is >18× larger, compared to a simple plate-shaped metal antenna with the same layout footprint.

B. FMC Layout Strategy

For silicon layout area penalty saving, the plasma-current collection antenna with FMC circuit is placed within a dicing street of a silicon wafer (Fig. 3). The dicing street width is typically around 80 μm in the current mainstream blade dicing. The antenna and circuit exclusive for FMC can be placed within the blade dicing street and hence almost no silicon layout area penalty is burdened for FMC fabricated with the blade dicing process. Through the interaction with FMC during fabrication, circuits that exhibit valuable functionality are generated and left in the diced ICs after the fabrication. This letter mainly considers the blade dicing as it is the current low-cost mainstream dicing scheme. In other advanced laser or chemical dicing schemes, the dicing street width could be narrower down to around 20 μm. The antenna aspect ratio design should be updated depending on the dicing scheme used in the target process.

C. Self-Programming PUF With FMC

In this letter, the proposed FMC circuit is utilized to fabricate a highly stable self-programming oxide-breakdown PUF with small area penalty. Compared to other-type of silicon-based PUFs [4], [5], [6], the inherently explicit stochastic oxide-breakdown behavior can be utilized as stable PUF entropy source. Fig. 4 depicts the circuit schematic and its simulated waveforms. Except for transistors subject to oxide-breakdown, 5-V thick-oxide IO devices are used.

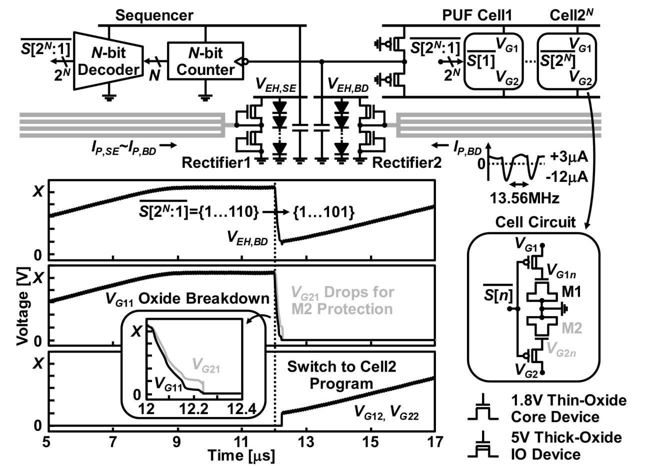

Fig. 4. Circuit schematic and simulated waveforms of FMC-based self-programming PUF.

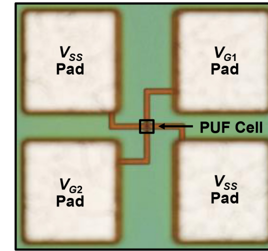

Fig. 5. Die photograph of PUF cell core.

A pair of FMC-based circuits are employed for stable PUF ID programming: one for generating the transistor oxide-breakdown voltage at $V_{EH,BD}$ and the other for generating the stable power supply at $V_{EH,SE}$ for the proper PUF programming sequencer operation. The sequencer consists of an edge-triggered N-bit counter followed by a decoder to generate sequential PUF programming control signal during fabrication based on the collected plasma ion energy. Each PUF cell programming completion can be self-detected. The counter in the sequencer increments the address by detecting the sudden drop of $V_{EH,BD}$ due to immediate reduction of oxide impedance at the oxide-broken node in the PUF cell. To prevent the sequencer supply voltage from dropping down due to the crowbar current at PUF cell switching, the sequencer input buffer consist with long channel devices. Also this $V_{EH,BD}$ voltage drop can be utilized to protect from additional oxide-breakdown at another unbroken node in the PUF cell. Compared to the oxide-breakdown PUF reported in [7], a bulky high-voltage generator for oxide breakdown could be omitted in this self-programming PUF scheme with FMC implementation.

III. Experimental Results

For a preliminary PUF cell electrical characterization, a test chip was fabricated in 180-nm CMOS with a set of the oxide-breakdown PUFs (Fig. 5). In total 1920 PUF cells operations were evaluated by applying a ramp voltage to both PUF core gate voltages V_{G1} and V_{G2} pads simultaneously from a common power supply to measure stable oxide-breakdown PUF operations and associated electrical characteristics changes. Simultaneous breakdown at both nodes is prevented by the same mechanism as PUF programming with FMC. Fig. 6 presents the distribution of gate oxide-breakdown voltages of 1920 PUF cells. The breakdown voltage variations range over 0.5 V, indicating a wide variation of oxide durability. Due to this durability

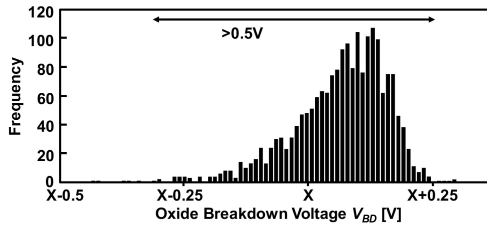

Fig. 6. Measured gate oxide-breakdown voltage distribution.

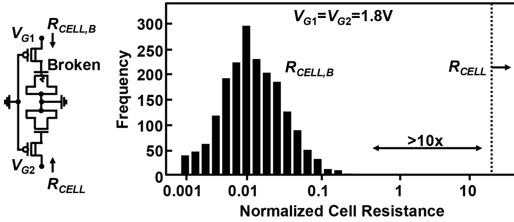

Fig. 7. Measured gate impedance after oxide breakdown.

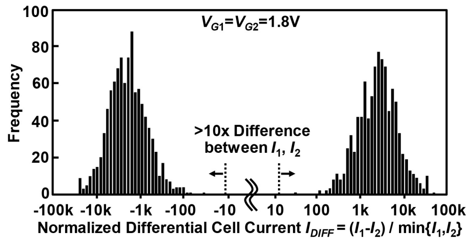

Fig. 8. Measured distribution of differential current in 1920 PUF cells.

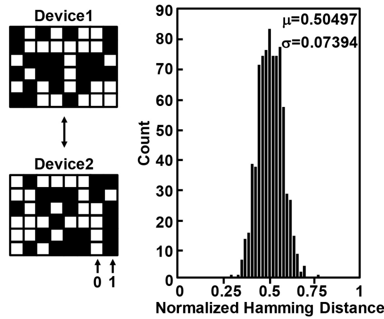

Fig. 9. Measured Hamming distance between 40 devices of 48-bit PUF code.

variation, no simultaneous breakdown for both nodes of PUF cell was observed, and the gate impedance distribution is clearly separated with and without breakdown (Fig. 7). The resistance changes between broken and unbroken oxide were all measured to be more than 10× for stable PUF cell operation against dynamic voltage and temperature (VT) environment fluctuations. The difference produced by the oxide-breakdown also can be observed from the differential current I_{DIFF} in the PUF cell. It could be measured to be >10× difference for all the 1920 PUF cells (Fig. 8). Fig. 9 demonstrates the performance of the generated bit sequence as PUF, based on the Hamming-distance (HD) value (μ/σ = 0.50497/0.07394) among 40 devices of 48-bit PUF code.

The FMC circuit incorporating the oxide-breakdown PUF cell was fabricated in 180-nm standard CMOS [Fig. 10(a)]. Measured 230 PUF cells successfully exhibit PUF functionality with the aid of FMC during fabrication. The differential current I_{DIFF} between the paired PUF cell was measured to be >2× difference for all the 230 cells and spread evenly between positive and negative values (Fig. 11). In

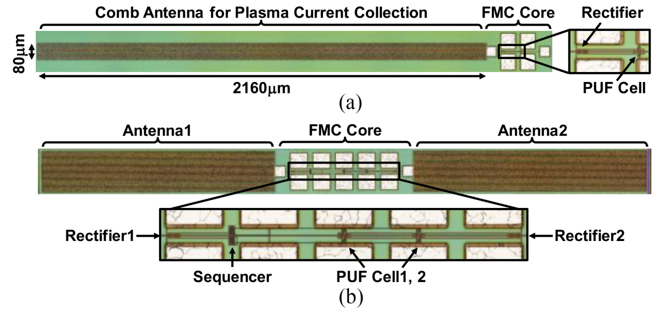

Fig. 10. Micrographs of PUF cell test chip with FMC: (a) single PUF cell with FMC and (b) 2-bit PUF cell array with FMC.

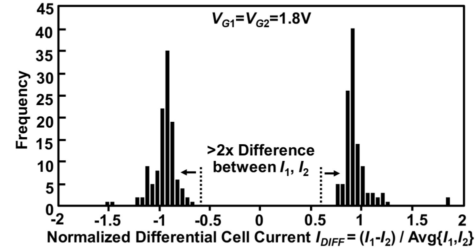

Fig. 11. Distribution of differential current in 230 single PUF cells with FMC.

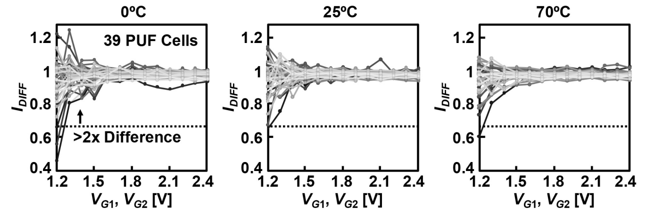

Fig. 12. PUF cell response to variations in temperature and supply voltage.

this circuit configuration, I_1, I_2 difference is reduced from >10× to >2× due to current flow through always-on transistor pseudo-resistors between V_{G1} and V_{G2} for PUF response readout. For practical PUF with FMC, by cutting the wire connecting V_{G1} and V_{G2} in the dicing process, >10× difference could be obtained. Based on the 230 PUF cells response, its entropy was measured to be 0.9998. In addition, this explicit entropy difference can be maintained over wide temperature and supply voltage ranges over 0 °C–70 °C and 1.3–2.4 V (Fig. 12). Even in the PUF cell implementation with 5-V IO devices, low-voltage PUF operation can be possible because of the huge impedance changes after the oxide- breakdown phenomena.

Finally, oxide-breakdown PUF array programming with the FMC sequencer was evaluated [Fig. 10(b)]. It has two antennas for oxide-breakdown voltage and power supply to the sequencer. 23 pairs of PUF cell response bits was measured. Similar to the single PUF cell measurement with FMC, the cell current difference I_{DIFF} for every PUF cells under the sequencer control also exhibited >2× difference for the stable PUF response read-out (Fig. 13). Based on the 23 pairs of PUF cells response, its entropy was measured to be 0.9986.

For the Hamming weight (HW) and HD characterizations, 8-bit PUF codes of single PUF cells measured over 20 devices were analyzed. The normalized average HW was calculated to be 0.512 and the HD distribution was calculated to be 0.514 in average (μ) and 0.1766 in deviation (σ). This HD deviation is almost identical to the one according to the 8-bit binary distribution, indicating reasonable randomness. By applying autocorrelation function (ACF) to

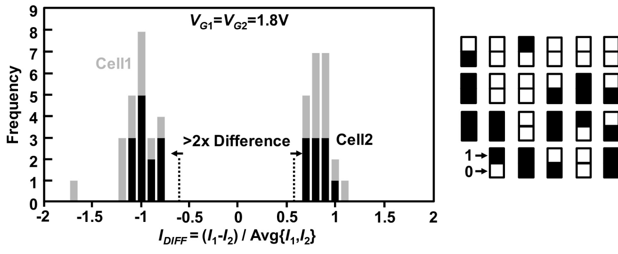

Fig. 13. Differential current distribution and response bits of 23 pairs of PUF cell with FMC.

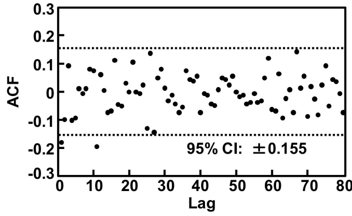

Fig. 14. Autocorrelation plot of the 160-bit PUF data.

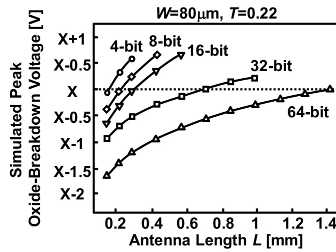

Fig. 15. Simulated $V_{EH,BD}$ dependence on antenna length.

TABLE I
PERFORMANCE COMPARISON BETWEEN OXIDE-BREAKDOWN PUFs

	VLSI'10 [8]	ISSCC'18 [7]	SSCL'19 [9]	This Work
Technology	65nm	55nm	40nm	180nm
Bit Cell Area [μm²] (Normalized Area)	3 (0.38)	0.66 (0.12)	3 (1)	11.3 (0.19)
Post Procseeing BD	Yes	Yes	Yes	No
Inter HD	0.499	0.5	0.496	0.486
BER [%]	0	0	0	0 (39-bit)
VDD [V]	1.0-1.2	0.81-1.32	0.9-1.5	1.3-2.4
Temperature [°C]	0-85	-40-150	-20-120	0-70

the 160-bit PUF data, no ACF peaks were observed, and no spatial correlation was identified (Fig. 14). A comparison with other oxide-breakdown PUFs is shown in Table I. Although there are issues about PUF code shortness and detailed BER evaluation at current stage, our PUF has the advantage of completing self-programming by oxide-breakdown during fabrication with FMC, thus there is no need for on-chip high-voltage generator and no post-processing for programming.

The maximum PUF code length programable by FMC is determined by the available plasma current in the process and the antenna size. Fig. 15 presents the harvested oxide-breakdown voltage $V_{EH,BD}$ dependence on the antenna length. Assuming typical plasma current density of 10 pA/μm^2, 64–128-bit PUF array would be the practically available solution programable by the FMC placed in the 80-μm width narrow dicing street. In addition, plasma etching time becomes shorter as the metal wire thickness thinner, but the typical etching time ranges from a few minutes to several tens of minutes order, which is sufficiently long compared to the time needed for one PUF cell programming. Based on typical total charge to breakdown of $<$10 C/cm^2 and gate area of $<$0.1 μm^2 for a 1.8-V IO device, one PUF cell programming is completed within around 10 ms. Therefore, even thickness $T_{\text{NORM}} = 0.22$ is sufficient to program a large-sized PUF during fabrication.

IV. CONCLUSION

The silicon prototype successfully demonstrated feasibility of FMC. This letter presents the concept of FMC harvesting energy from plasma and operating during its fabrication etching process. The comb-shaped antenna efficiently collect plasma ion injection current by maximizing the etching peripheral area of the antenna. This compact antenna implementation allows the FMC to be placed within the dicing street for further silicon layout area saving. As one of the FMC demonstrators, the self-programming oxide-breakdown PUF is presented. The silicon prototype successfully demonstrated feasibility of circuit fetal-movement.

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