A High-speed Low Voltage CMOS Schmitt Trigger With Adjustable Hysteresis

Zhe Chen
National University of Defense Technology
Microelectronics and Solid-state Electronics
Chang Sha, China
1328882015@qq.com

Shuming Chen
National University of Defense Technology
Microelectronics and Solid-state Electronics
Chang Sha, China
smchen@163.com

***Abstract*—This paper presents a brief overview of Schmitt Triggers and proposes a low voltage adjustable CMOS Schmitt trigger using body biasing technique. The voltage-feedback inverter with body control is employed to speed up the switching process, and control the intensity of the feedback. The proposed Schmitt trigger makes it particularly attractive for low-voltage high-speed applications. The CMOS Schmitt Trigger circuit has been designed using 40nm 1V CMOS technology and simulated using HSPICE with BSIM4 device models. Simulation results are presented.**

Keywords—Schmitt trigger; voltage-feedback; body biasing technique; adjustable hysteresis

I. INTRODUCTION

It is well known that CMOS Schmitt triggers widely used in both analog and digital applications. It can convert irregular shaped waveform or sine wave or triangular wave into a perfect shape square wave or pulse to solve noise problem[1]. The important applications of Schmitt trigger circuit has been widely used in the input buffers to increase noise immunity[2], sub threshold SRAM[3], sensor[4], and pulse with modulation circuits[5].

Schmitt trigger circuits are acting as signal restoring circuits[6]. They are widely used because of filtering any type of noise and exhibits a plain digital signal. The Schmitt trigger is a comparator that includes two different transition threshold voltage. When the input is higher than a certain chosen threshold, the output is switched; when the input is lower than another chosen threshold, the output is also switched; when the input is between the two, the output retains its is DC transfer characteristics. Schmitt trigger has different switching thresholds for positive-going and negative-going input signals, while the comparator shows only one switching threshold. This type of characteristics is called hysteresis. The hysteresis of Schmitt trigger provides better noise margin and noise stable operation than the comparator.

The conventional Schmitt trigger is consist of operational amplifiers and resistor feedback. This type of Schmitt trigger is not suitable for the integration in CMOS technology, primarily because of the area of operational amplifiers and resistors in the chip[7]. Compare to the conventional Schmitt trigger circuits, CMOS Schmitt trigger has these advantages: high noise immunity, well suited for low voltage applications[8], and thresholds present less variations with respect to the temperature alterations[9]. The CMOS Schmitt trigger was introduced by Stayert and Sansen[10]. It has high input impedance, balanced input and output characteristics. However, the speed of this circuit is limited to the slew rate of the internal node of the circuit. Perhaps the most widely cited single-ended Schmitt trigger is initially proposed by Dokic[11]. Dokic's design stacks four transistors between power and ground rails and is therefore not particularly attractive for application where supply voltages are low. A very simple CMOS Schmitt trigger circuit is composed of two regular CMOS inverters and two output transistors, well suited for low-voltage and high-speed applications[12]. Cong-Kha Pham introduces a CMOS Schmitt trigger circuit with controllable hysteresis using logical threshold voltage control circuit[13]. The Schmitt trigger proposed by R.Sapwi et al. is based on conventional

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the width-length ratio[14]. The hysteresis width is clear and less sensitive to the variation of load capacitance and source voltages. Fei Yuan[15] generates the Schmitt trigger using regenerative current feedback and can be adjusted by varying the current of the regenerative feedback network. Ambothu Suresh [16] proposes the CMOS Schmitt Trigger circuit with self-bias transistor (SBT) technique which was used to reduce power.

In this paper, we propose a new Schmitt trigger with adjustable hysteresis. The hysteresis of the Schmitt trigger can be adjusted by body biasing technique. Positive voltage-feedback is employed to speed up the switching process compared to the Schmitt trigger in [11]. The remaining part of the paper is mentioned as: the proposed Schmitt trigger is described in sec.2. Sec.3 presents the simulation results in TSMC-40nm CMOS technology. The final paper is concluded in sec.4

II. CIRCUIT DESCRIPTIONS

The CMOS Schmitt trigger is consist of three NMOS transistors (N1, N2, and N3), and three PMOS transistors (P1, P2, and P3) in Fig.1a. It shows the basic CMOS Schmitt trigger circuit design according to [11] in the Fig.1a.

The proposed Schmitt trigger is shown in the Fig.1b and is categorized into two parts which is Part 1 and Part 2. Part 1 is consist of two transistors of N1 and P1. Part2 is consist of two inverters (N2, P2, N2, P3), while the inverters serve three purposes. First, the switching threshold of the inverter is depended on the aspect ratio of PMOS and NMOS (k_P and k_N). Part 2 employs the different ratio of the transistors to change the switching threshold of the inverter. Second, the part 2 CMOS inverters are connected in a positive feedback configuration, thus speeding up the switching process. Third, the control voltages of the CMOS inverter in part 2 controls the intensity of the feedback signal, thus the switching threshold voltage of the Schmitt trigger.

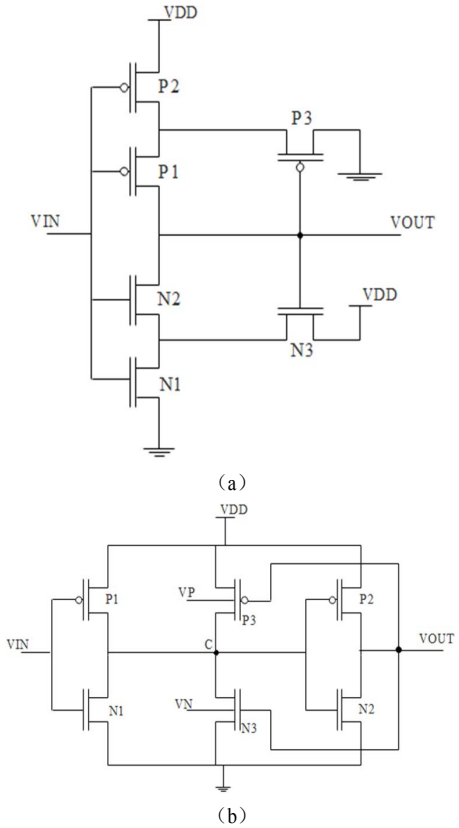


Fig.1 (a) Traditional Schmitt trigger (b) Proposed circuit

The proposed Schmitt trigger is shown in the Fig.1b and is categorized into two parts which is Part 1 and Part 2. Part 1 is consist of two transistors of N1 and P1. Part2 is consist of two inverters (N2, P2, N2, P3), while the inverters serve three purposes. First, the switching threshold of the inverter is depended on the aspect ratio of PMOS and NMOS (k_P and k_N). Part 2 employs the different ratio of the transistors to change the switching threshold of the inverter. Second, the part 2 CMOS inverters are connected in a positive feedback configuration, thus speeding up the switching process. Third, the control voltages of the CMOS inverter in part 2 controls the intensity of the feedback signal, thus the switching threshold voltage of the Schmitt trigger.

The operation of the circuit can be explained as follows. Let assume initially that the input signal V_{IN} is low. And the output signal V_{OUT} is low too. So transistors of N1, N3 is in the cut off regions and P1, P3 is in the saturation regions. To switch the V_{IN} from low to high, the transistor of N1 turns on gradually, the voltage of node C decrease, while the V_{OUT} gradually increase. When the

the equal resistor of C node to ground decrease, pulling down the voltage of node C further, which improve the rate of the switch in the V_{OUT}. Since the control voltage Vp can be used to set the threshold voltage of P3, and thus the amount of an extra current source of P3, the switching threshold voltage from low to high (V_{LH}) can be adjusted via the controlling voltage Vp. Limited by $|2\phi_F|$, the maximum V_{LH} is obviously obtained when Vp approximately reaches 0 Volt.

When the N1 is actually in the saturation regions, current in the N1 is equal to the sum of P1 and P3. So we can find:

$$\frac{u_pC_{ox}W_{P1}}{2L_{P1}}(V_{DD}-V_{LH}-|V_{TH0,\,P1}|)^2+\frac{u_pC_{ox}W_{P3}}{2L_{P3}}$$

$$(V_{DD}-V_{LH}-|V_{TH,P3}|)^2=\frac{u_nC_{ox}W_{N1}}{2L_{N1}}(V_{LH}-V_{TH0,N1})^2 \quad (1)$$

Where $V_{TH0,\,N1}$ and $V_{TH0,\,P1}$ is the zero body-bias threshold voltage of N1 and P1, $V_{TH,\,P3}=V_{T0}-\gamma(\sqrt{|2\phi_F|+V_P-V_{DD}}-\sqrt{|2\phi_F|})$. As the result, we can get:

$$V_{LH}=\frac{m(V_{DD}-|V_{TH0,P1}|)+n(V_{DD}-|V_{TH,P3}|)-V_{TH0,N1}+d}{m+n+1} \quad (2)$$

Where

$$d=\sqrt{\begin{matrix}n(V_{DD}+V_{TH0,N1}-|V_{TH0,P1}|)^2+m\\(V_{DD}-V_{TH0,N1}-|V_{TH,P3}|)^2+mn(|V_{TH0,P1}|-|V_{TH,P3}|)^2\end{matrix}}$$

$m=\frac{K_{p1}}{K_{N1}}$, $n=\frac{K_{p3}}{K_{N1}}$, K_N and K_p are given by $\frac{uC_{ox}W}{2L}$.

Similarly, when the input voltage is high, the output voltage is also high. So the transistors of P1, P3 is in the cut off regions and N1, N3 is in the saturation regions. To switch the V_{IN} from high to low, the transistor of P1 turns on gradually, the voltage of node C increase, while the V_{OUT} gradually decrease. When the voltage of node C is higher than the switching voltage of the inverter (P2 and N2), N3 turns off and P3 turns on gradually. As the result, the equal resistor of C node to VDD decrease, pulling up the voltage of node C further, which improve the rate of the switch in the V_{OUT}. Since the control voltage V_N can be used to set the threshold voltage of N3, and thus the amount of an extra current sink of N3, the switching threshold voltage from high to low (V_{HL}) can be adjusted via the controlling voltage V_N. Limited by$|2\phi_F|$, the minimum V_{HL} occurs when V_N reaches approximately V_{DD}.

When the P1 is actually in the saturation, current in the P1 is equal to the sum of N1 and N3. So we can find:

$$\frac{u_nC_{ox}W_{N1}}{2L_{N1}}(V_{HL}-V_{TH0,N1})^2+\frac{u_nC_{ox}W_{N3}}{2L_{N3}}$$

$$(V_{HL}-V_{TH,N3})^2=\frac{u_pC_{ox}W_{P1}}{2L_{P1}}(V_{DD}-V_{HL}-|V_{TH0,P1}|)^2 \quad (3)$$

Where $V_{TH0,\,N1}$ and $V_{TH0,\,P1}$ is the zero body-bias threshold voltage of N1 and P1, $V_{TH,\,N3}=V_{T0}+\gamma(\sqrt{|2\phi_F|-V_N}-\sqrt{|2\phi_F|}$. As the result, we can get:

$$V_{HL}=\frac{pV_{TH0,N1}+qV_{TH,N3}-V_{DD}+|V_{TH0,P1}|+e}{q+p+1} \quad (4)$$

Where

$$e=\sqrt{\begin{matrix}q(V_{DD}-V_{TH,N3}-|V_{TH0,P1}|)^2+p\\(V_{DD}-V_{TH0,N1}-|V_{TH0,P1}|)^2+pq(V_{TH0,N1}-V_{TH,N3})^2\end{matrix}}$$

$p=\frac{K_{N1}}{K_{P1}}$, $q=\frac{K_{N3}}{K_{N1}}$, K_N and K_p are given by $\frac{uC_{0x}W}{2L}$.

From Equation (2) and (4), it is clearly shown that V_{LH} depends on V_P, while V_{HL} depends on V_N. As a result, V_{LH} and V_{HL} are tuned via V_P and V_N. The width of the hysteresis (V_{HW}) is calculated and given by $V_{HW}=V_{LH}-V_{HL}$.

III. SIMULATION RESULT

To verify the circuit performance, HSPICE with BSIM4 is used to simulate the conventional and proposed circuit using a 40nm CMOS process under 1V supply.

TABLE I shows the transistor dimensions for conventional circuit according to [11] and proposed circuit. As shown in Fig.2a, the propagation delay will increase when the load capacitance increase. The delay times of these circuits are measured as the average of the response time for positive and negative output transition for a square input waveform at 1GHz. We can clearly find that in Fig.1b the propagation delay of proposed circuit is less compared to the traditional Schmitt trigger because of the positive

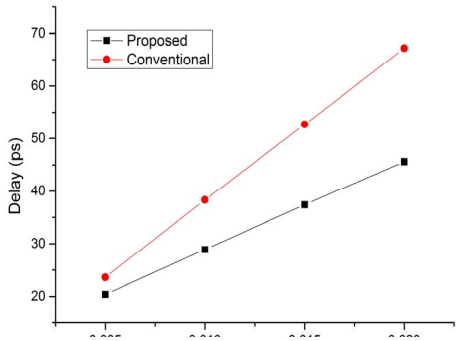
feedback feature. A speed comparison between the proposed circuit and traditional circuit, with the same capacitive load (0.1pF), is present in Fig.2b, where the superiority of the new circuit is apparent.

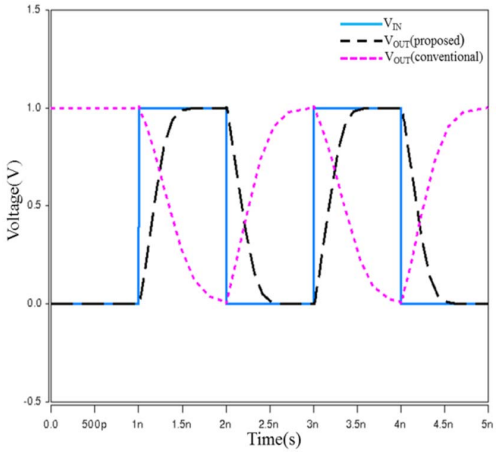
Fig.3 shows the output signal when the input signal is applied with a triangular waveform (1Vpp, 1 GHz). We can find the switching threshold voltages from the crossing points between the input and output signal. The Fig.4 shows the DC voltage transfer characteristics for different values of V_P and V_N. We can easily see that the switching threshold voltages of the proposed circuit can be independently adjusted. For example, V_{LH} depends on the control voltage V_P and V_{HL} depends on the control voltage V_N.

Finally, the Fig.5 shows the switching threshold voltage V_{LH} versus V_P and V_{HL} versus V_N. As seen, switching threshold voltages V_{LH} and V_{HL} can be adjusted from 0.69V to 0.89V and from 0.19 to 0.30V. The margin of switching threshold voltages V_{LH} is approximately 20% of the supply voltage, which V_{HL} is approximately 10%.

TABLE I. Transistor Dimensions

Length=40nm	**Conventional circuit**	**Proposed circuit**
	Width(nm)	Width(nm)
P1	800	800
P2	800	800
P3	1040	400
N1	400	400
N2	400	400
N3	900	200





(b)

Fig.2 (a) Propagation delay at CL=0.005pF、0.01pF、0.015pF、0.02pF (b) Speed comparison between the proposed circuit and traditional circuit

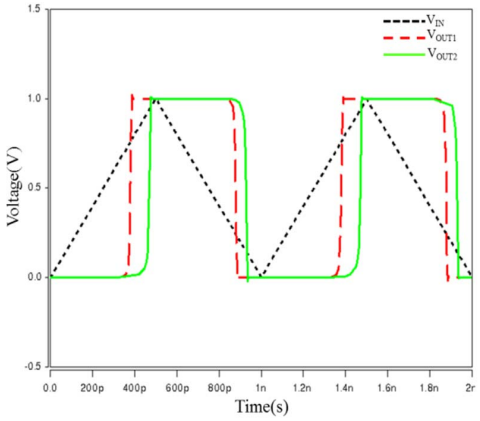


Fig.3 Input and output waveforms

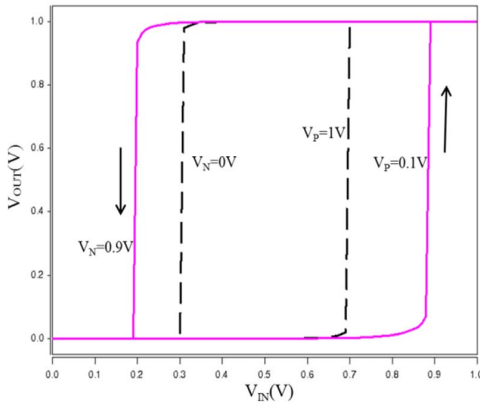
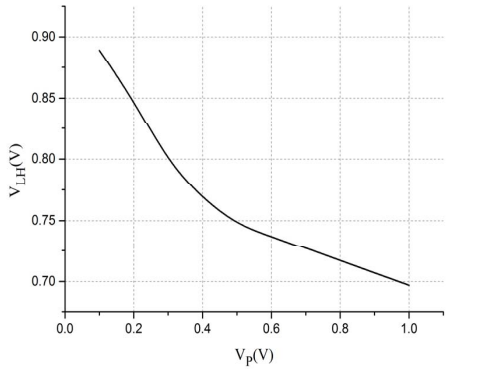
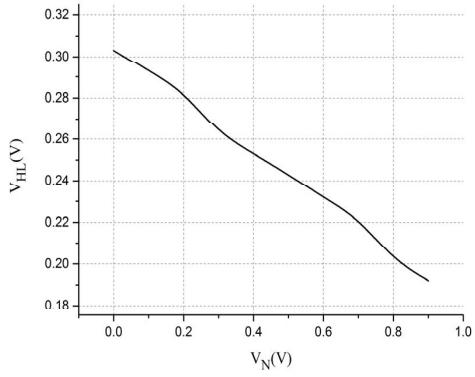


Fig.4 DC voltage transfer characteristics



(a)



(b)

Fig.5 (a) Switching threshold V_{LH} versus V_P and (b) V_{HL} versus V_N

IV. CONCLUSIONS

A new proposed CMOS Schmitt Trigger using body biasing technique has been presented. The hysteresis of the Schmitt trigger can be adjusted by controlling voltages V_P and V_N. The voltage-feedback characteristics of the Schmitt trigger makes it particularly attractive for low-voltage high-speed applications. Simulation results demonstrate that the proposed circuit is giving less propagation delay compare to conventional circuit. The circuit can operate under 1V and the switching threshold voltages can be independently adjustable via controlling voltages V_P and V_N.

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